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Politécnica - La Almunia
Centro adscrito
Universidad Zaragoza

ESCUELA UNIVERSITARIA POLITÉCNICA
DE LA ALMUNIA DE DOÑA GODINA (ZARAGOZA)

ANEXOS

Sistema “Copidron”

DISEÑO DE UN SISTEMA DE SEGUIMIENTO DE RUTA PARA UN DRON

424.16.33

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Director: Javier Esteban Escaño

Fecha: 08/11/2017

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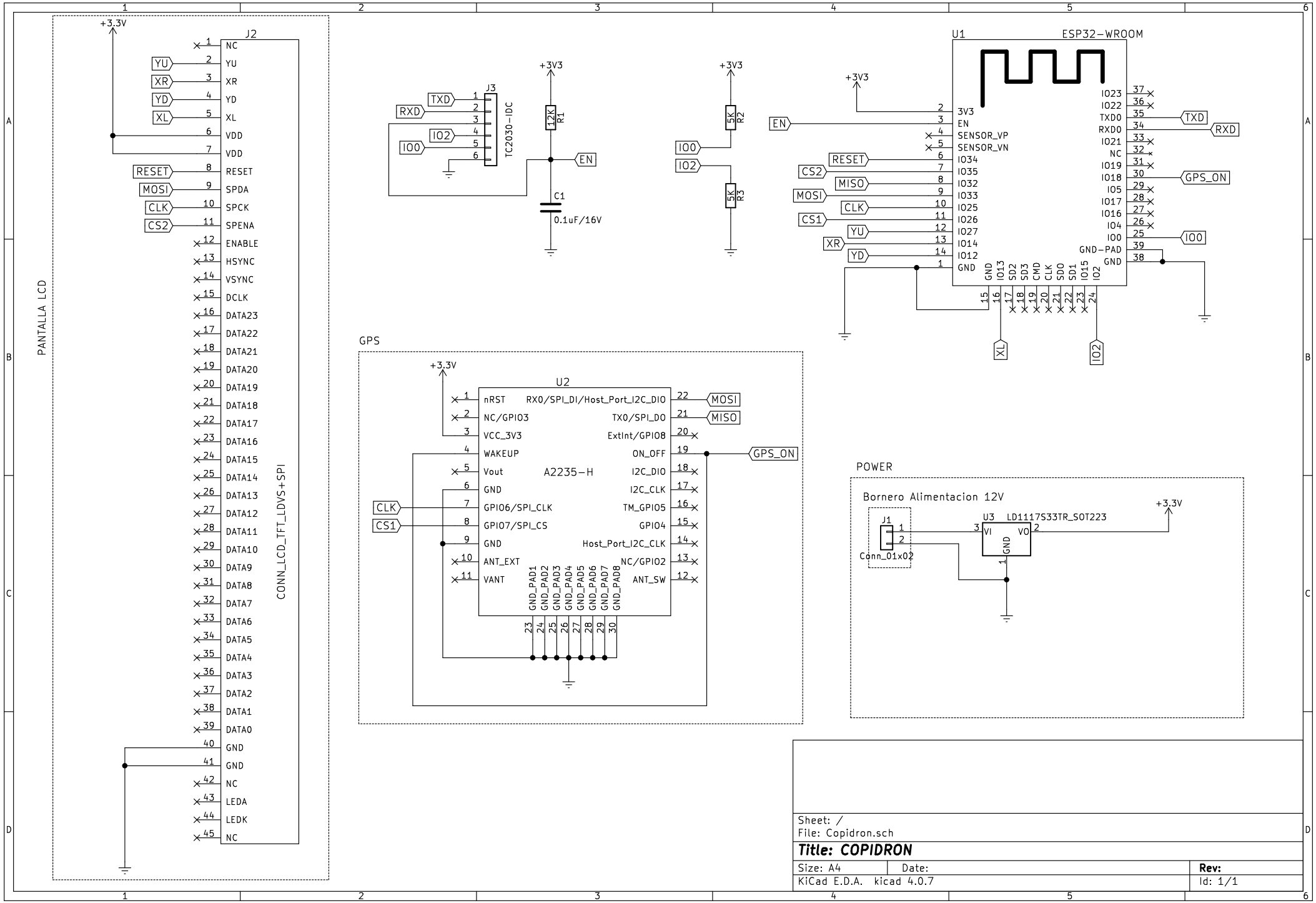
1.1. PLANO 1: ESQUEMA ELECTRÓNICO DE LA PANTALLA PARA EL COCHE.



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Title: COPIDRON

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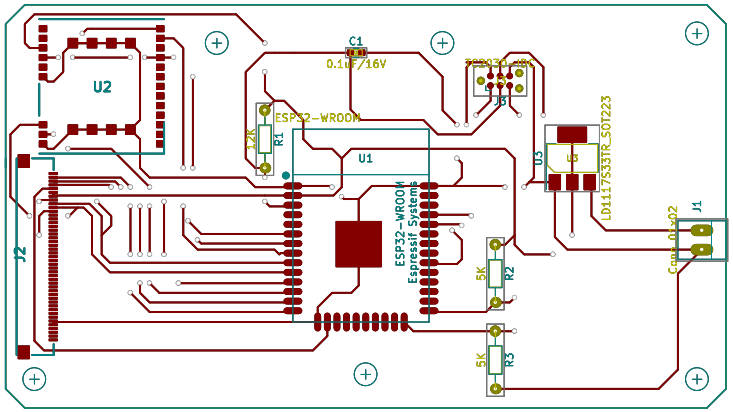
KiCad E.D.A. kicad 4.0.7		Id: 1/1

1.2. PLANO 2: ESQUEMA FRONTAL DE LA PCB DE LA PANTALLA.



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Size: A4	Date:	**Rev:**
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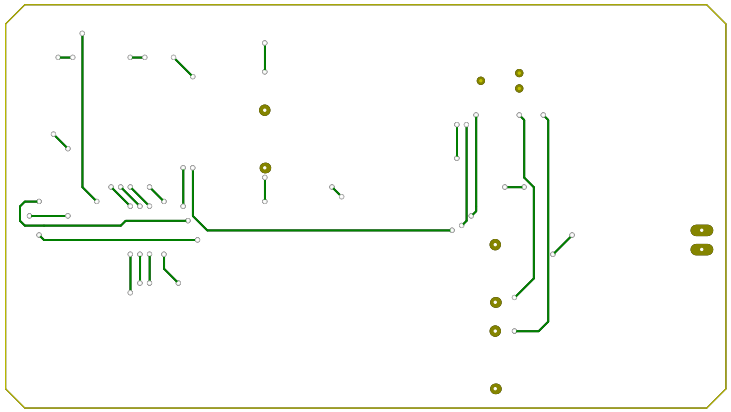
1.3. PLANO 3: ESQUEMA TRASERO DE LA PCB DE LA PANTALLA.



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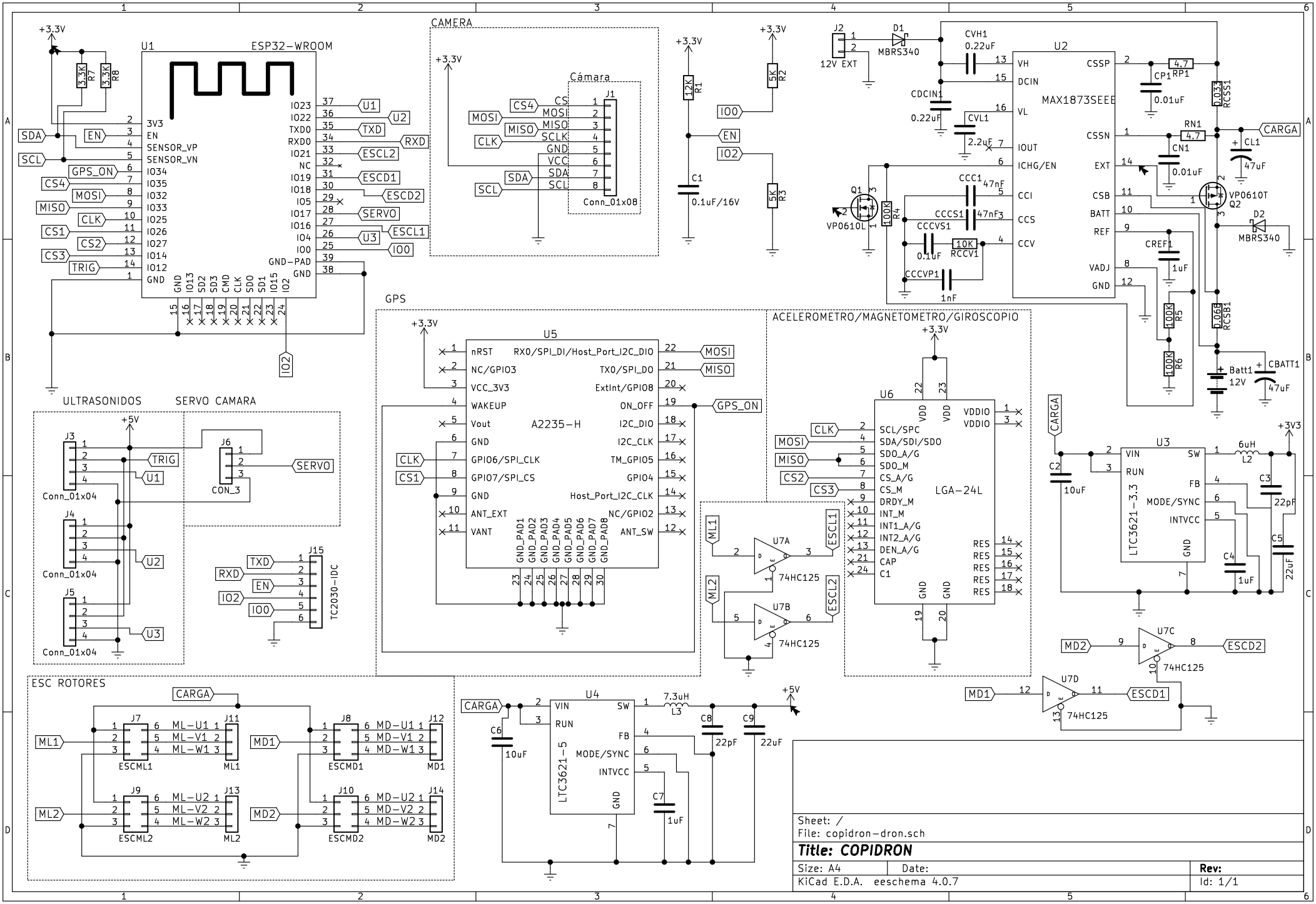
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 4.0.7		Id: 1/1

1.4. PLANO 4: ESQUEMA ELECTRÓNICO DEL DRON.


U1
ESP32-WROOM
CAMERA
Cámara
J1
Conn_01x08
GPS
U5
A2235-H
ACELEROMETRO/MAGNETOMETRO/GIROSCOPIO
U6
LGA-24L
U2
MAX1873SEEE
ULTRASONIDOS
SERVO CAMARA
ESC ROTORES
U3
LTC3621-3.3
U4
LTC3621-5
U7A
U7B
U7C
U7D
74HC125
Q1
VP0610L
Q2
VP0610T
D1
MBRS340
D2
MBRS340
J2
12V EXT
Batt1
12V
CARGA
+3.3V
+5V
+3V3
SDA
SCL
EN
GPS_ON
CS4
MOSI
MISO
CLK
CS1
CS2
CS3
TRIG
SERVO
TXD
RXD
IO2
IO0
ML1
ML2
MD1
MD2
ESCL1
ESCL2
ESCD1
ESCD2
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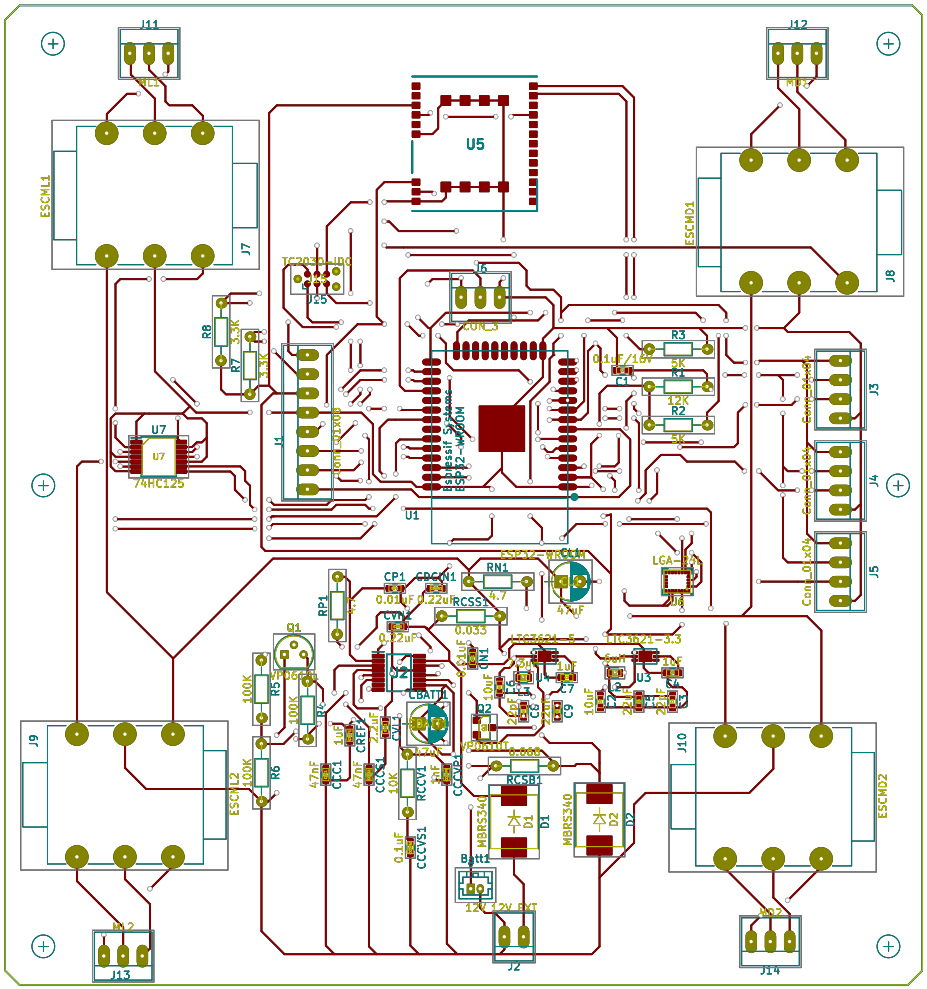
Id: 1/1

1.5. PLANO 5: ESQUEMA FRONTAL DE LA PCB DEL DRON.



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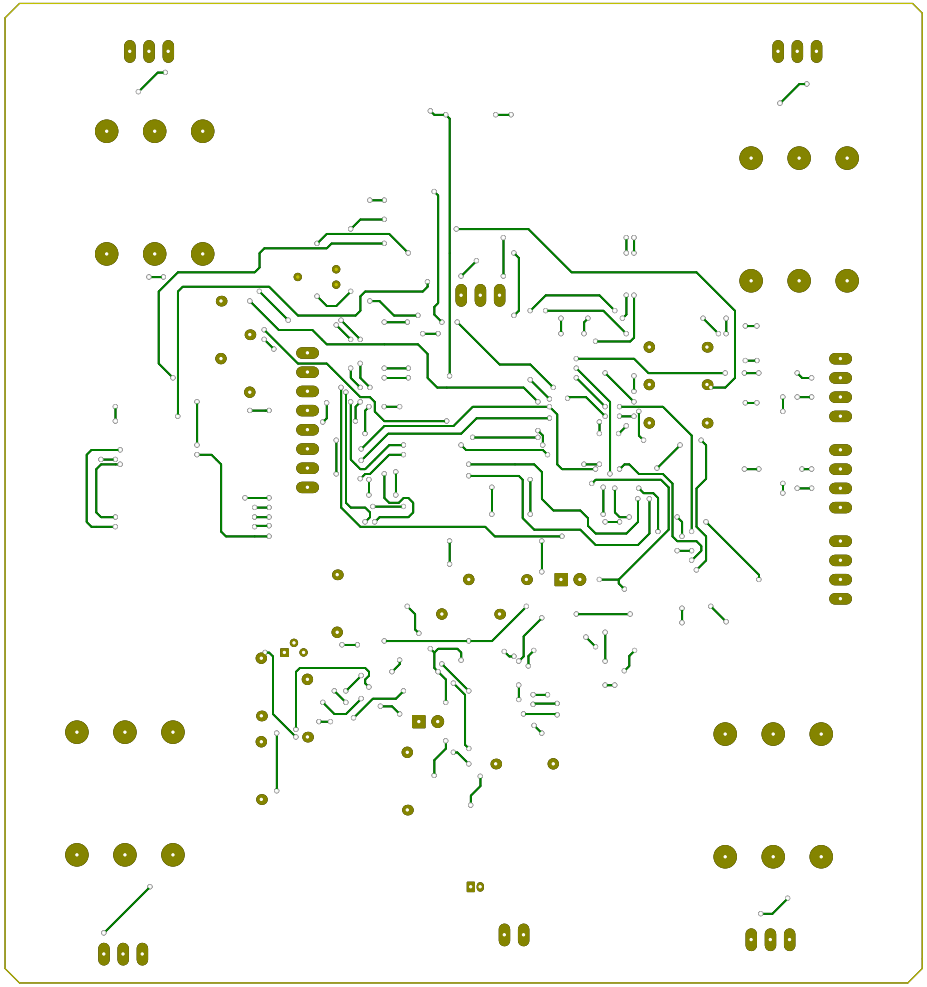
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. pcbnew 4.0.7		Id: 1/1

1.6. PLANO 6: ESQUEMA TRASERO DE LA PCB DEL DRON.



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File: copidron-dron.kicad_pcb		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. pcbnew 4.0.7		Id: 1/1

ANEXO 2. (COMPONENTES Y PROGRAMACIÓN)

2.1. TABLA DE COMPONENTES

	Elemento	Referencia	Fabricante	Peso (total en g)	Web
Componentes Coche	Pantalla LCD 9,8''	CLAA098EP01	CPT	-	http://onubaonline.es/es/9-8-pulgadas/CPT_CLAA098EP01_9.8_pulgadas-datasheet
	GPS	A2235-H	Maestro	-	http://www.farnell.com/datasheets/1833178.pdf
	Regulador de Tension	LD1117S33TR-SOT223	STMicroelectronics	-	http://pdf1.alldatasheet.com/datasheet-pdf/view/94465/STMICROELECTRONICS/LD1117S33TR.html
	Controlador	ESP-WROOM-32	Espressif Systems	-	http://espressif.com/sites/default/files/documentation/esp-wroom-32_datasheet_en.pdf
	Resistencias de distintos Valores (3 u.)	SFR16S	Vishay	-	http://www.vishay.com/docs/28722/sfr16s25.pdf
	Condensador 0,1µF	0603YC104KAT4A	AVX	-	http://es.farnell.com/avx/0603yc104kat4a/ceramic-capacitor-0-1uf-16v-x7r/dp/2691202
Componentes Dron	Controlador	ESP-WROOM-32	Espressif Systems		http://espressif.com/sites/default/files/documentation/esp-wroom-32_datasheet_en.pdf
	4 Rotores	A2212/13	Suppo	208	http://www.suppomodel.com/motor/A2212.html
	4 ESC	ESC 30A	Genericas	100	
	4 Aspas	GWS HD 10x6	GWS	364	https://hobbyking.com/en_us/hobbykingtm-propeller-10x6-black-cw-ccw-6pcs.html
	Servo	MG90S	Tower Pro	9g	http://descargas.cetronic.es/MG90S.pdf
	Cámara	ArduCAM Mini 5MP	arducam	20g	http://www.arducam.com/downloads/shields/ArduCAM_Mini_5MP_Camera_Shield_DS.pdf
	Sensores Ultrasonidos	HC-SR04	Cetronic	30g	http://descargas.cetronic.es/HCSR04.pdf
	Chip cargador de baterias	MAX1873SEEE	MAXIM	0,288	https://datasheets.maximintegrated.com/en/ds/MAX1873.pdf
	Fuente Conmutada	LTC3621-3.3 / LTC3621-5	Linear Tecnology	2g	https://www.iodparts.com/part/linear-technology/ltc3621hms8e-23-3-pbf#datasheet
	GPS	A2235-H	Maestro	4g	http://www.farnell.com/datasheets/1833178.pdf
	Acelerómetro, Magnetómetro, Giroscopio.	LSM9DS1	STMicroelectronics	4g	http://www.farnell.com/datasheets/2028150.pdf?_ga=2.156422846.421548647.1501143593-590481626.1501143593
	Resistencias de distintos Valores (13 u.)	SFR16S	Vishay	0,286	http://www.vishay.com/docs/28722/sfr16s25.pdf
	Diodo Schottky (2 u.)	SS34	MULTICOMP	0,434	http://es.farnell.com/multicomp/ss34/schottky-diode-3a-40v-smc-full/dp/1843499
	Transistores Mosfet (2 u.)			0,2	
	Condensadores de distintos valores (21 u.)	0603YCXXX	AVX	3,4	http://es.farnell.com/avx/0603yc104kat4a/ceramic-capacitor-0-1uf-16v-x7r/dp/2691202
	Amplificador para ESC	74HC125T14		2	https://www.diodes.com/assets/Datasheets/74HC125.pdf
	Inductores (2 u.)	GLFR1608T100M-LR	TDK	0,34	http://es.farnell.com/tdk/glfr1608t100m-lr/power-line-ind-10uh-400ma-20-full/dp/2372219
	Bateria	Multistar 5200mAh 4S 10C	Multistar	433	https://hobbyking.com/en_us/multistar-high-capacity-4s-5200mah-multi-rotor-lipo-pack.html

2.2. DATASHEET COMPONENTES

2.2.1. Pantalla

Volver a: 9.8 pulgadas

CLAA098EP01

DATASHEET | STOCKS

Fabricante:CPT

Última actualización :: 13-05-2015 11:13:54

Compare

CPT CLAA098EP01 Información básica

Fabricante ::	CPT
Modelo ::	CLAA098EP01
Tipo de panel ::	a-Si TFT-LCD , Panel
Temperatura de trabajo ::	0 ~ 50 °C
Temperatura de almacenaje ::	-25 ~ 65 °C
RoHS ::	Conformidad RoHS
Caracteristicas específicas ::	Superficie Antirreflectante, Amplio ángulo de visión, Retroiluminación de LED blanco, Tipo Horizontal, With LED Driver

CPT CLAA098EP01 Características mecánicas

Tamaño del panel ::	9.8 pulgadas
Resolución ::	1280(RGB)×960 (Quad-VGA)
Configuracion del pixel ::	RGB Raya Vertical
Densidad de pixeles ::	162 PPI
Relación de aspecto ::	4:3 (H:V)
Forma del panel ::	Plana rectangular
Tamaño del pixel ::	0.156×0.156 mm (H×V)
Peso ::	140g (Typ.)
Superficie ::	Antireflejante (Neblina 13%)
Área activa ::	199.68×149.76 mm (H×V)
Dimension del contorno ::	211.8×163.5 mm (H×V)
Profundidad del contorno ::	2.5/4.45 (Typ./Max.) mm
Soportes (Brackets) ::	agujeros de montaje (5 pcs) on up, left y right side brackets
Horizontal o vertical ::	Tipo Horizontal
Panel tactil ::	Sin

CPT CLAA098EP01 Caracteristicas ópticas

Modo de Visualización ::	VA, Normalmente Negro, Transmisivo
Brillo ::	400 cd/m2 (Typ.)
Relación de contraste ::	VA, Normalmente Negro, Transmisivo
Visualización de color ::	16.7M (6-bit + Hi-FRC)
Gama de colores ::	50% NTSC (CIE1931)
Tiempo de respuesta ::	30 (Typ.)(Tr+Td)
Ángulo de visión ::	80/80/80/80 (Min.)(CR≥10) (L/R/U/D)
Dirección de la vista ::	Simétrica
Cromacidad blanca ::	Wx:0.314; Wy:0.335

CPT CLAA098EP01 Características electrónicas

Frecuencia vertical ::	60Hz
Exploración inversa ::	No

CPT CLAA098EP01 Sistema de retro-iluminación

Posición de la lámpara ::	Borde
Tipo de lámpara ::	WLED
Vida útil de la lámpara ::	15K(Min.) (horas)
tipo de interfaz ::	Incluida en la señal de interface del panel
Placa controladora de lámpara (Tipo) ::	Borde
Corriente de la lámpara ::	20±0.5mA

CPT CLAA098EP01 Conector de señal

Tipo de señal ::	LVDS
Clase de la señal ::	LVDS (1 ch, 8-bit) + SPI
Voltaje de entrada ::	3.3V (Typ.)
Corriente de entrada ::	TBD
Tipo de interfaz ::	Conector
Intefaz (Marca) ::	Panasonic
Intefaz (Modelo) ::	AXT340124
Intefaz (Tamaño pin) ::	0.4 mm
Intefaz (Pins) ::	40 pins
Intefaz (Cantidad) ::	1 pcs

CPT CLAA098EP01 Producción

Estado de la producción :: No continuado

Productos relacionados

EG4801S-AR

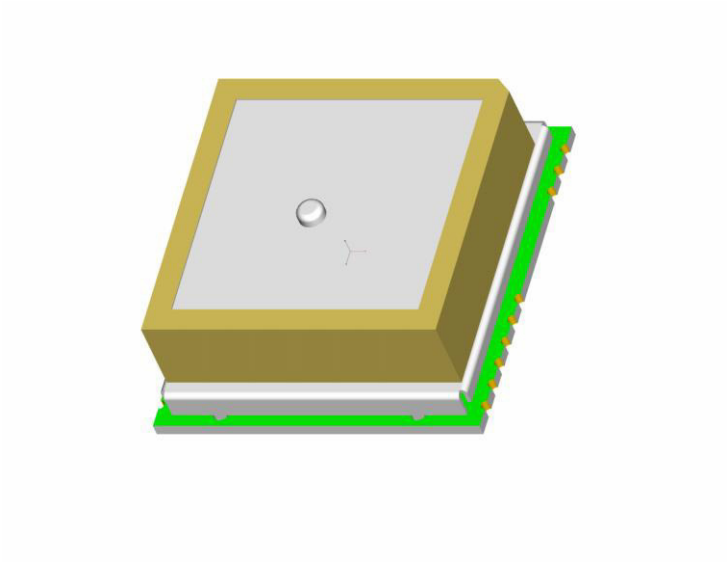
2.2.2. Receptor GPS

GPS Receiver A2235-H

A Description of Maestro's
GPS Antenna Receiver Module A2235-H

User's Manual

Version 1.3



Revision History

Rev.	Date	Description
0.1	08-15-12	First release
0.2	04-19-13	1.Update I2C interface description 2.Update Pin information 3.Add self-start description 4.Add External Antenna description
0.9	05-08-13	1.Version updated 2.Add section 6.1 remark
1.0	08-15-13	Update Pin information and Table 6 current consumption data
1.1	10-16-13	Update Pin information and Mechanical outline solder side A2235-H
1.2	11-12-13	Add a Note 5 under section 3
1.3	03-04-14	Updates 1PPS Picture
	mm-dd-yy	

	Name	Date	Signature
Written by	Happy wen	03-04-14	H W
Checked by	Sam Law, Matthieu	03-04-14	S L,M
Approval by	Frank Tang, Calvin Yau	03-04-14	F T,C Y

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Table of Contents

1 Introduction

A2235-H is an antenna module with SiRF Star IV ROM based chip and an on-board patch antenna (15mm x 15mm x 4mm). It is cost down version of A2035-H with reduced size and stacked up antenna architecture. RF switch was implemented (but NOT on engineering samples) so as to support external active antenna for performance enhancement if required. In order to have an easier migration for existing customers using A2035-H, we decided to keep same pin assignment as that of A2035-H. Additional pins for supporting external antenna won't affect this drop-in replacement property. Since there is an RF feed point underneath the module, special PCB design is required on user's application. Receiver part of A2235-H is fully identical to A2200-A with latest CSR Premier ROM 9333 and enabling I2C host port, Host Port I2C_CLK (Pin 14) was added for this new function.

The A2235-H is a module designed for a 3.3V environment.

1.1 Feature Overview

The A2235-H is a new module with the following outstanding features.

- Fast, responsive location experience
  - High-sensitive navigation engine with tracking down to -163dBm
  - 48 track verification channels
  - SBAS (WAAS, EGNOS, MSAS, GAGAN)
- Breakthrough micro power technology
  - Requires only 50 – 500µA to maintain hot start capability
- Active jammer remover
  - Removes in-band jammers up to 80dB/Hz
  - Tracks up to eight CW (continuous wave) jammers
- Size: 17.8mm (L) x 16.5mm (W) x 6.7mm (H)
- Operating voltage: 3V3
- No internal EEPROM but support external EEPROM through I2C interface
- Extremely low power consumption by using DC/DC converter
- No back-up battery required
- MEMS supports
- TCXO is used for providing stable 16.369MHz system clock
- CSR Premier ROM 9333 is used which is equivalent to Release 2.2 (i.e. F/W 4.1.2)
- Support external active antenna
- Build-in LNA with close to 20dB gain

1.2 Characteristics Overview

The module's most important characteristics are:

Operable at 3.3V / 22mA @ 1fix per second

- UART interface at CMOS level
- Small form factor of 17.78 x 16.51 mm² (0.7" x 0.65")
- Supported temperature range: -40°C to +85°C
- Single-sided SMT component, for reflow soldering
- RoHS compliant, lead-free
- Tape & reel packaging
- Excellent antenna support
    - On-module patch antenna
    - Antenna input for direct connection of external active antenna
    - RF switch to select between antennas

The antenna receiver module is available as an off-the-shelf component, 100% tested and shipped in tape-and-reel packaging.

1.3 RoHS and Lead-Free Information

Maestro's products marked with the lead-free symbol either on the module or the packaging comply with the "Directive 2002/95/EC of the European Parliament and the Council on the Restriction of Use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

All Maestro GPS receiver modules, GPS antenna receiver module and telematics units are RoHS compliant.

1.4 Label

The A2235-H label (size: 12.0x 4.0 mm²) contains the following information:

Figure 1: A2235-H label

The label is placed on the side of the GPS antenna. The data matrix code holds the product type, part number, software release, hardware release, factory code, year & week of assembly and a 6-digit serial number. Due to limited space on module label, only product type, year & week of assembly and 6-digit serial number will be printed on it.

Representing	**Factory location**	**Product Number**	**Part Number**	**Software Release**	**Hardware Release**	**Assembly Year/Week**	**Serial Number**
Number of digits (16)	XX	XXXXXXX	XXXX	XX	XX	XXXX	XXXXXX
	2	6	4	2	2	4	6
Example	TF	A2235H	9333	01	01	1211	000005
Meaning	TF	Given	Given	Given	Given	Year=12 Week=11	Increment from 000001 up to 999999

Example of MID#: TFA2235H933301011211000005

1.5 Characteristics

The module is characterized by the following parameters.

1.5.1 GPS Characteristics

Channels		48, parallel tracking
Correlators		~400,000
Frequency		L1 (= 1,575 MHz)
Tracking Sensitivity On-module antenna		-163 dBm
Horizontal Position Accuracy	Stand alone	< 2.5 m CEP (SA off)
Time To First Fix – TTFF (theoretical minimum values; values in real world may differ)	Obscuration recovery (1)	0.1 s
	Hot start (2)	< 1 s
	Warm (3)	< 35 s
	Cold (4)	< 38 s

Table 1: A2235-H GPS characteristics

(1) The calibrated clock of the receiver has not stopped, thus it knows precise time (to the µs level).
(2) The receiver has estimates of time/date/position and valid almanac and ephemeris data.
(3) The receiver has estimates of time/date/position and recent almanac.
(4) The receiver has no estimate of time/date/position, and no recent almanac.

Note: Performance (sensitivity and TTFF) might slightly decrease below -30°C.

1.5.2 Mechanical Characteristics

A2235-H Mechanical dimensions	Length Width Height	17.78±0.20 mm, 0.7±0.008” 16.51±0.20 mm, 0.65±0.008” 7.11 mm, 0.28”(Max)
A2235-H Weight		4.0 g, 0.14 oz

Table 2: A2235-H dimensions and weight

1.6 Handling Precautions

The GPS receiver module A2235-H is sensitive to electrostatic discharge (ESD). Please handle with appropriate care.

2 Ordering Information

2.1 GPS Receiver A2235-H

The order number is built as follows:

- **A2235-Hxxxx**

A2235-H is the model name. The “xxxx” refers to the current part number on the module.

2.2 Packing

The A2235-H GPS modules come in a tape and reel package suitable for pick and place machines.

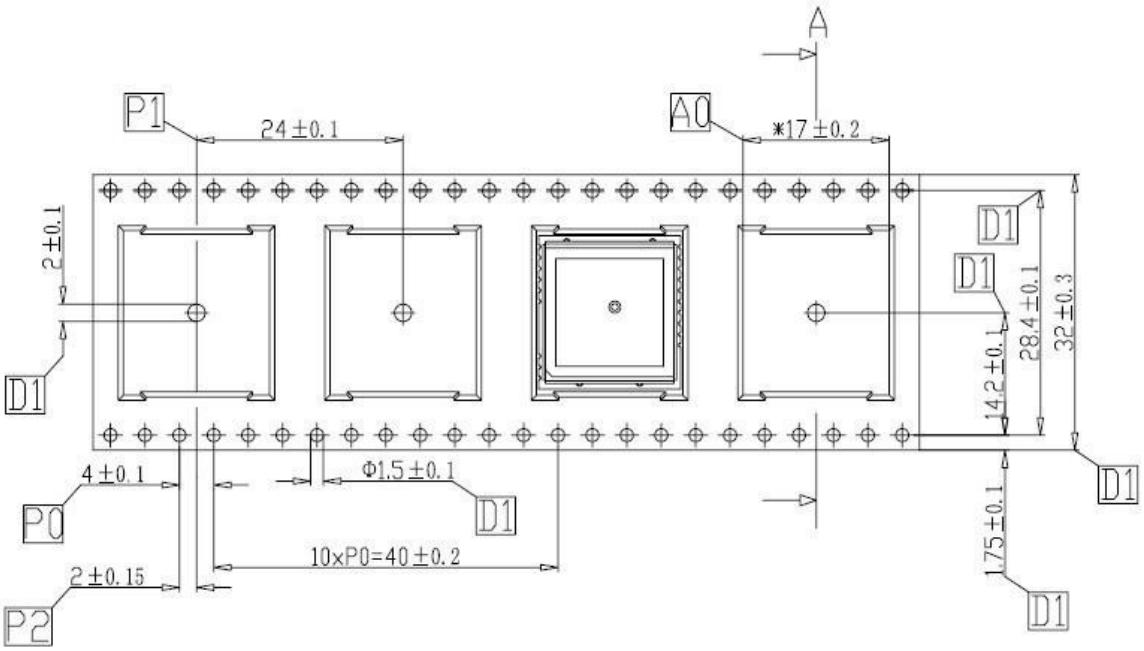


Figure 2: A2235-H tape specifications (1)

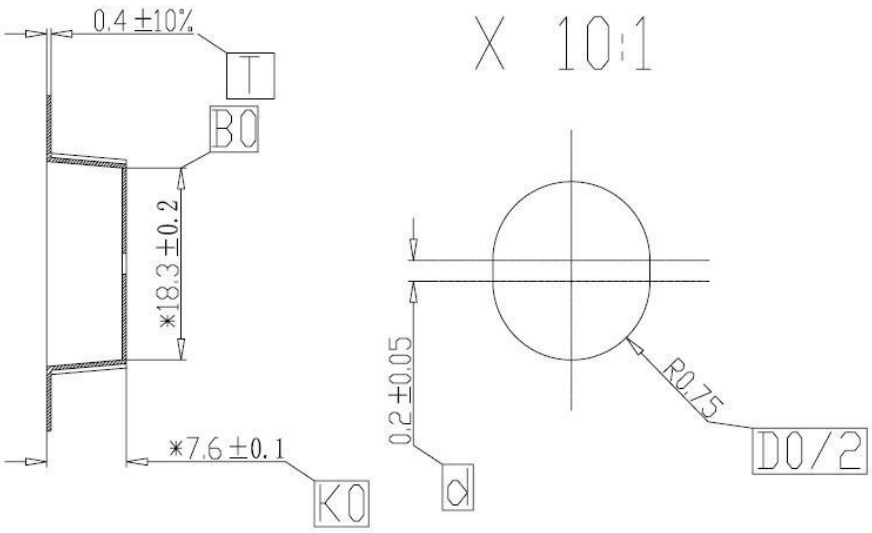


Figure 3: A2235-H tape specifications (2)

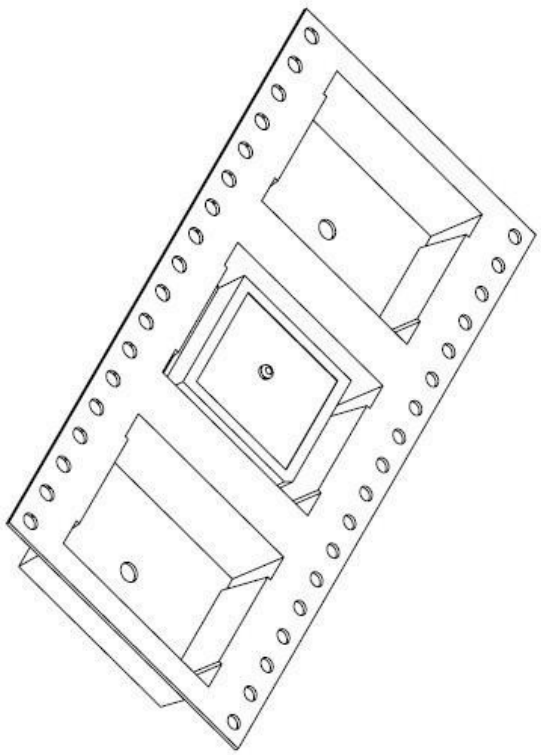


Figure 4: A2235-H tape specifications (3)

One complete reel holds 500 A2235-H modules.

There is 1 kinds of packaging for shipment:

One box holds 1 reel
Reel diameter: 38 cm
Outer Box dimensions: 38.8 (W) x 38.8 (L) x 5.7 (H) cm
Gross weight: 5.06 Kg
Net weight: 4.13 Kg

2.3 Additional Equipment

EVA2235-H	Evaluation Kit (including one module A2235-H)

Table 3: Additional equipment

A detailed description of the EVA2235-H Evaluation Kit can be found in the appropriate manual.

3 Quick Start

In order to allow an easy and quick start with the A2235-H module, this chapter provides a short overview on the important steps to be taken to receive NMEA messages with position information on a serial port (UART).

NOTE 1: The A2235-H needs an external pull-up resistor to be configured for UART operation. Please consider the pull-up resistor in your design or pull the GPIO up right after reset by other means.

NOTE 2: The ON_OFF input of the A2235-H needs to be connected to a push-pull output of a microprocessor. For a wake-up, including the initial one after power on, a LOW-HIGH transmission is mandatory.

NOTE 3: It is recommended to connect the nRST pin of the A2235-H to an open collector / open drain output of a microprocessor!

NOTE 4: The A2235-H needs two external pull-up resistors to be configured for the Baud rate 4800. Please consider the pull-up resistor in your design.

NOTE 5: In order to let existing A2035-H customers to drop-in replace original design with A2235-H, they have to send an OSP command to switch the protocol and baud rate to NMEA 4,800.

A0 A2 00 18 81 00 01 01 00 01 01 01 05 01 01 01 00 01 00 01 00 01 00 01 00 00 12 C0 01 64 B0 B3

If there are provisions to mount 2.2K pull up resistors on GPIO[0] and GPIO[1] (please refer to Table 4) on existing design, customers can configure the protocol and baud rate through hardware instead of sending OSP command above.

3.1 Minimum Configuration

The following picture shows the minimum configuration for NMEA or binary outputs received and commands sent via an RS232 interface based on the GPS module A2235-H.

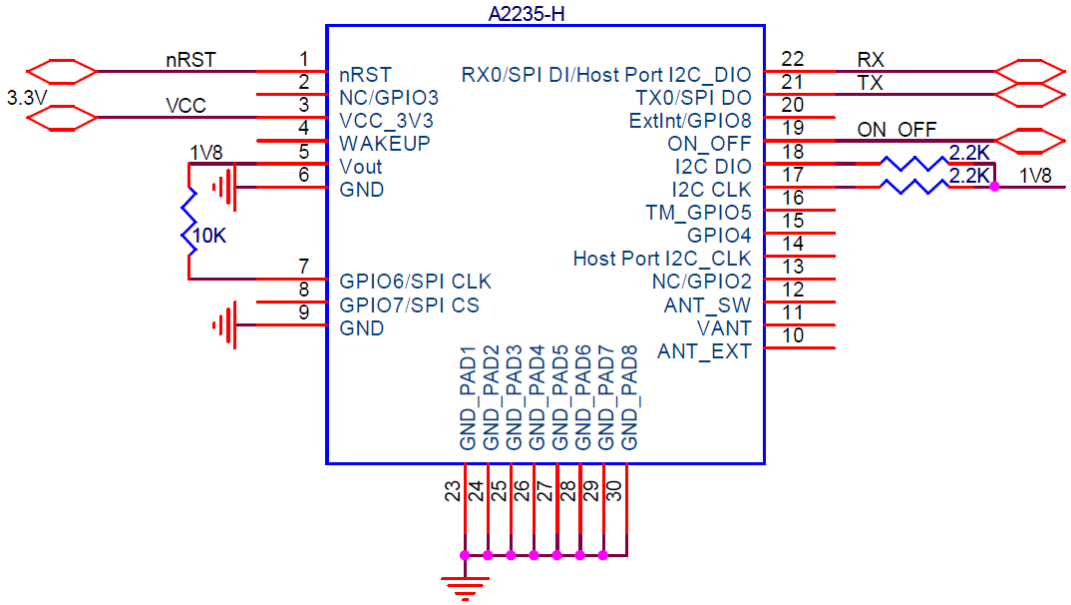


Figure 5: Minimum configuration A2235-H

NOTE: It is recommended to supply Vcc continuously! Use SiRFaware™ or other low power modes to reduce power consumption of the module while no position information is required.

- External antenna input impedance is 50 Ω. Match as close as possible.
- Maximum allowed external antenna current is 50 mA. Consider a current limiter.

For completeness the following picture shows the use of an RS232 level shifter.

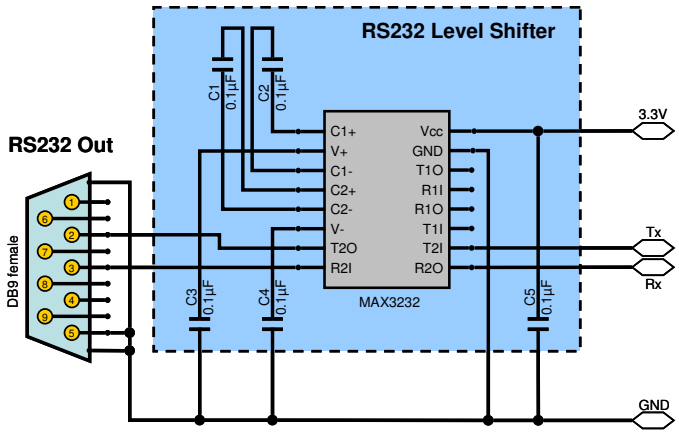


Figure 6: RS232 level shifter for minimum configurations

Remarks:

- Place C1 to C5 (here: 0.1µF) close to MAX3232. For capacity values see datasheet of actual component used.
- Use 3.3V level shifter (MAX3232 or equivalent).

3.2 Antenna

Although the A2235-H offers an on-module antenna, an additional external active antenna can be used. Switching between both antennas is done via pin 12 (see also "5.2Description A2235-H Signals"). It is recommended to use an active GPS antenna with supply voltage of 3 to 5 VDC and a current draw of 50 mA maximum. The quality of the GPS antenna chosen is off great importance to the overall sensitivity of the GPS system. An active antenna should have a gain $\geqslant$ 20 dB and a noise figure $\leqslant$ 1.5 dB, which applies to more than 95% of the active antennas available in the market.

3.3 Serial Port Settings

In UART operation (defined by the external pull-up resistor as outlined in Minimum Configuration) the default settings are:

- Serial 0 (NMEA) 4800 baud, 8 data bits, no parity, 1 stop bit, no flow control

3.4 Improved TTFF

In order to improve the TTFF (Time To First Fix), it is recommended to keep Vcc supplied at all times. This will allow taking advantage of sophisticated low power mode features of the SiRFstarIV ROM chip set.

3.5 Self-start configuration

In order to minimize the GPIO required for operating A2235-H, WAKEUP (pin 4) and ON_OFF (pin 19) can be tied together for entering the self-start mode such that no ON_OFF pulse requires. Figure 7 shows the recommended connection for self-start configuration with UART host port enabled.

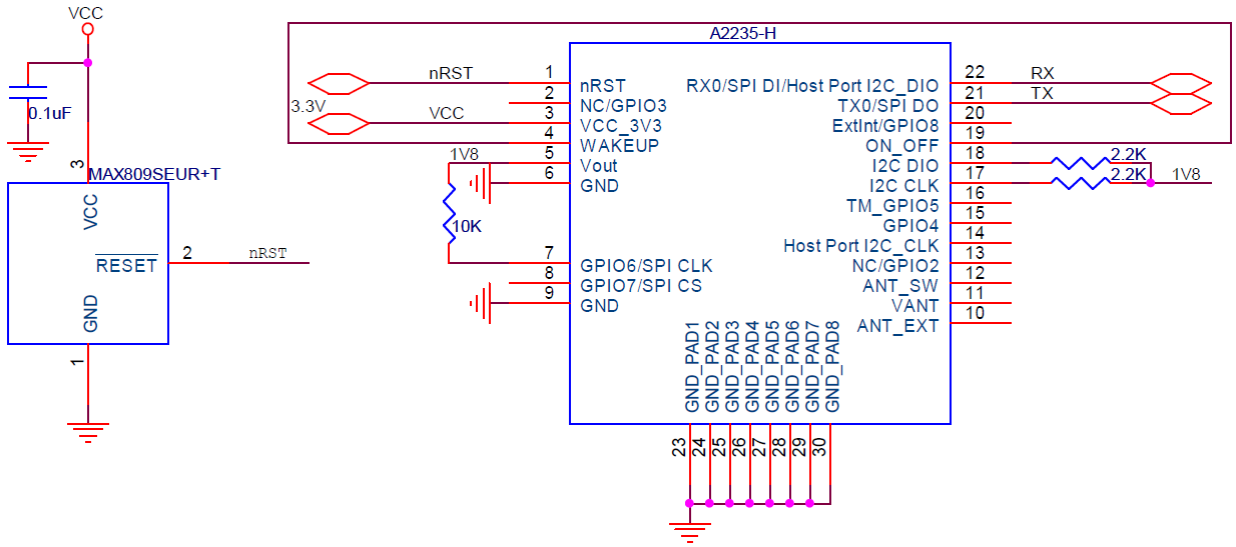


Figure 7: Self-start configuration A2235-H

For self-start mode, full power operation will be activated once Vcc applied. No power saving mode (PTF/MPM/Hibernation) will be supported. While using external EEPROM or SPI Flash power supervision chip (Maxim, MAX809SEUR+T) is mandatory in order to prevent any memory corruption if the Vcc removes abruptly.

3.6 Configure the baud rate

Baud rate and protocol selection can be set upon start up through GPIO configuration.A2235-H can be configured to output NMEA at standard baud rates, if the A2235-H is using the UART host interface.

Table 4 lists the settings for GPIO 0 and GPIO 1 to configure the baud rate at start-up. After start-up, the GPIOs can be used for other purposes.

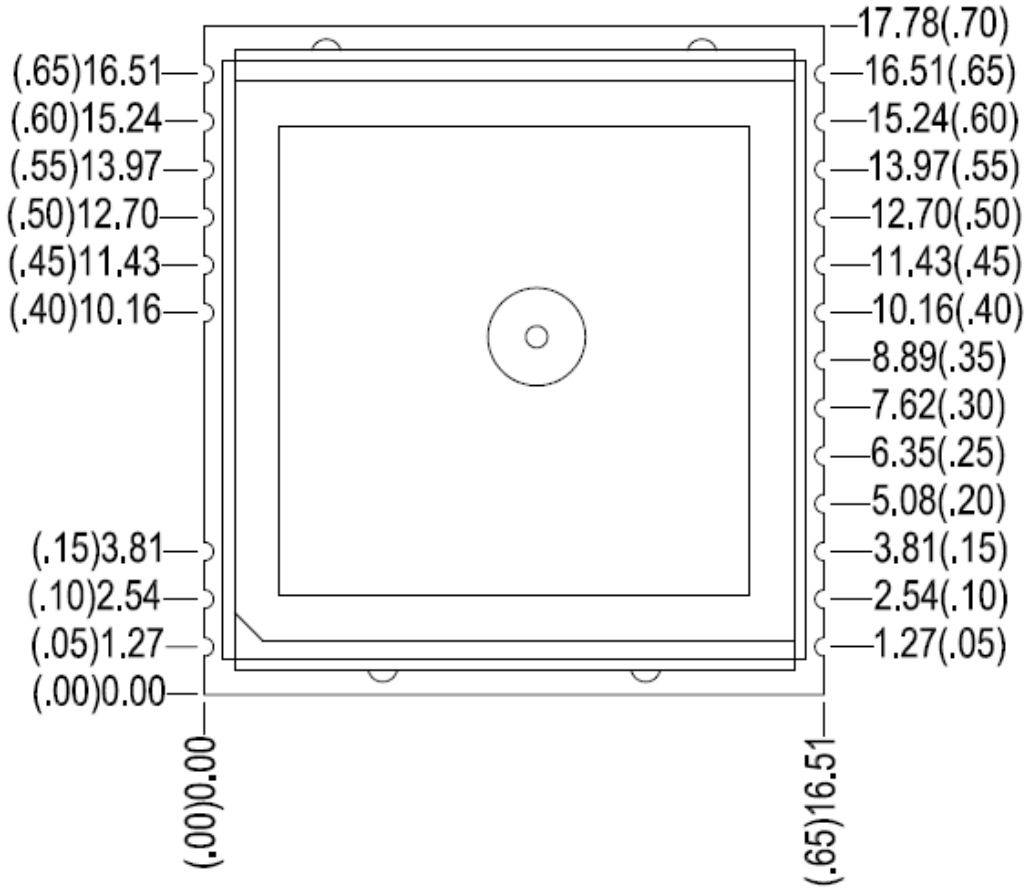
GPIO 0 (I2C_DIO)	GPIO 1(I2C_CLK)	Protocol	Baud Rate
Pull high	Pull high	NMEA	4800
Pull high	Pull low	NMEA	9600
Pull low	Pull high	NMEA	38400
Pull low	Pull low	OSP	115200
Remark: Pull high/low =2.2K			

Table 4: GPIO 0 and GPIO 1 Settings

Note: This feature is not available if any MEMS or non-volatile memory devices are attached to the auxiliary serial bus. The internal software default baud rate is NMEA 4800 when an EEPROM is connected.

4 Mechanical Outline

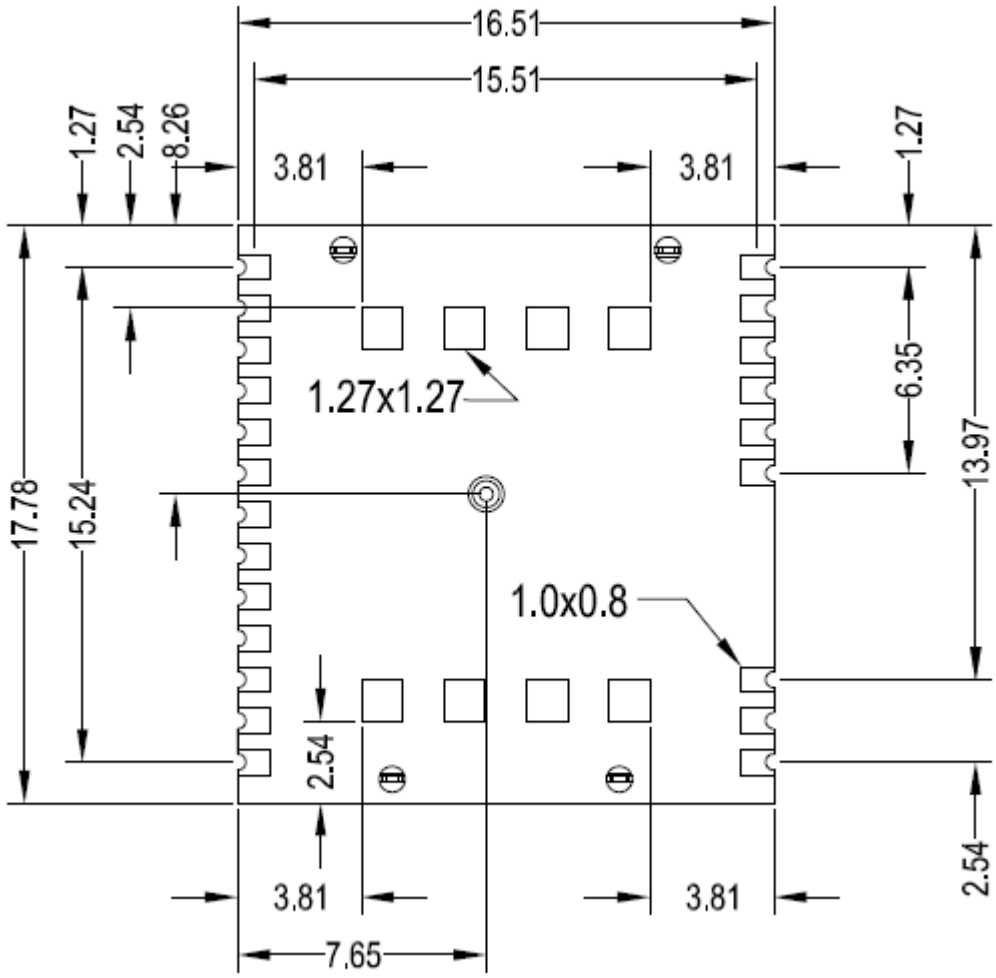
4.1 Details Component Side A2235-H



All dimensions in [mm] / [(inches)]

Figure 8: Mechanical outline component side A2235-H

4.2 Details Solder Side A2235-H



Solder pad size (outer pads): 1.0 x 0.8
Solder pad size (inner pads): 1.27 x 1.27
All dimensions in [mm]

Figure 9: Mechanical outline solder side A2235-H

5 Pin-out Information

5.1 Layout A2235-H

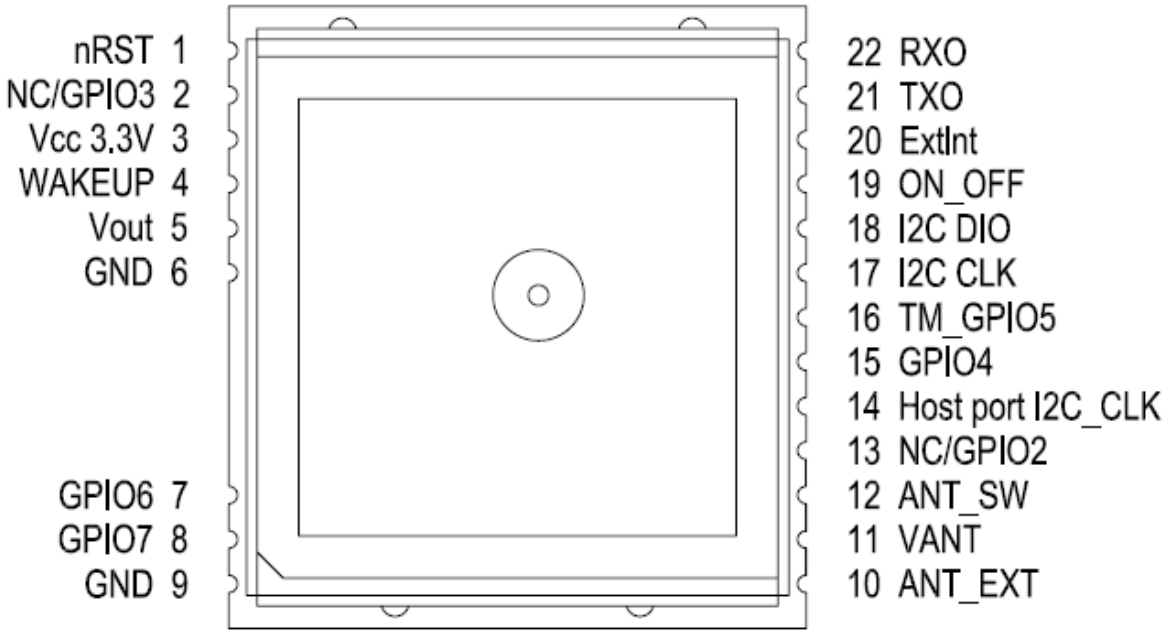


Figure 10: Pin-out information (top view) A2235-H

5.2 Description A2235-H Signals

Pin	Symbol	Function	Description
1	nRST	Input	Reset input, active low
2	GPIO3	None	Leave open
3	VCC3V3	Power Supply	3.0 – 3.6 V DC
4	WAKEUP	Output	- Status of digital section, Push-Pull output Low = OFF, KA (Keep Alive)-only, Hibernate, or Standby mode High = ON, operational mode - Connect it to ON_OFF pin for self-start mode
5	Vout	Voltage Output	Permanent 1.8V voltage output for up to 20mA current max.
6	GND	Power Supply	Ground (power supply)
7	GPIO6 CTS (SPI CLK)	Input	Configuration pin for communication mode. 10K to 1.8V for UART mode; leave open for SPI & host port I2C modes. SPI clock pin when module works in SPI mode
8	GPIO7 RTS (SPI CS)	Input	Configuration pin for communication mode. 10K to GND for host port I2C mode; leave open for SPI & UART modes. SPI chip select pin when module works in SPI mode
9	GND	Power Supply	Ground (power supply)
10	ANT_EXT	Antenna Input	Antenna signal / Z=50 Ohm (external active antenna in-put)
11	VANT	Power supply	Power supply antenna – provide according voltage (up to 5.0 VDC) - VANT feeds Pin 10 ANT_EXT
12	ANT_SW	Input	Antenna switch (LOW or open = internal antenna, HIGH = external antenna)
13	GPIO2	None	Leave open
14	Host Port I2C_CLK	Input	Host port I2C clock pin when module works in host port I2C mode
15	GPIO4	Input	External interrupt input pin – reserved for future use, leave open
16	TM_GPIO5	Output	Time Mark – 1PPS signal
17	GPIO 1 I2C CLK	Input / Output	Configuration pin for the baud rate,2.2K to 1.8V for the baud rate 4800 bps (see also“Configure the baud rate“). I2C clock output to MEMS interface
18	GPIO 0 I2C DIO	Input / Output	Configuration pin for the baud rate,2.2K to 1.8V for the baud rate 4800 bps (see also“Configure the baud rate“). I2C I/O to MEMS interface
19	ON_OFF	Input	Connect to push-pull output! This is mandatory! - Set to LOW by default - Toggle to HIGH and back to LOW > for first start-up after power on > to request a fix in SiRFaware™ or PTF mode > to go into or wake up out of hibernate mode - Connect it to WAKEUP pin for self-start mode

20	ExtInt (GPIO8)	Input	Interrupt input for MEMS interface (If ExtInt is not going to be used, it is recommended that this pin be tied directly to ground. Otherwise, a 100K pull-down resistor to ground should be connected to the ExtInt pin.)
21	TX0 / (SPI DO)	Output	Serial output 0.NMEA out if configured for UART; SPI data out pin when module works in SPI mode.
22	RX0 / (SPI DI) / (Host Port I2C_DIO)	Input	Serial input 0.NMEA in if configured for UART; SPI data in pin when module works in SPI mode; Host port I2C data I/O pin when module works in hist port I2C mode.

Table 5: Pin description A2235-H

6 Electrical Characteristics

6.1 Operating Conditions

Pin	Description	Min	Typical	Max
3	Vcc	3.0V	3.3V	3.6V
	Full power mode (Searching) Peak Current (1)		42mA	
	Full power mode (Searching) Average Current (2)		36mA	
	Full power mode (Tracking) Average Current (3)		22mA	
	TricklePower™ Mode		7.2mA	
	Push-to-Fix Mode		0.9mA	
	Micro Power Mode（SiRFaware™）		29uA	
	Hibernate Status		27uA	

Table 6: A2235-H electrical characteristics

(1) Peak searching current is characterized by millisecond bursts above average searching current
(2) Average searching current is typically only the first two seconds of TTFF
(3) Tracking current typically includes tracking and the post searching portion of TTFF

6.2 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
Vcc	Power supply	-0.3	+4.6	V
Vin	Voltage to I/O pin	-0.3	+3.6	V
Iov	Input current on any pin	-10	10	mA
Itdv	Absolute sum of all input currents during overload condition		200	mA
Tst	Storage temperature	-40	85	°C

Table 7: Absolute maximum ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.3 DC Electrical Characteristics

Symbol	Parameter	Min	Max	Unit
TX0, WAKEUP	Voh @ 4mA	2.6	Vcc	V
	Vol @ 4mA		0.45	V
RX0	Vih	2.0	Vcc	V
	Vil		0.8	V
nRST	For safe reset		0.2	V
ON_OFF	Vih	1.35	Vcc	V
	Vil	-0.3	0.45	V

Table 8: DC electrical characteristics

7 Mounting

This chapter describes the suggested mounting process for the A2235-H GPS receiver modules. In a RoHS compliant product with a RoHS compliant process it is recommended to use chemical tin as the counter-part to the module's pins. This will guarantee highest resistance against shocks.

7.1 Proposed Footprint for Soldering

The following proposal of a footprint for soldering is assuming a stencil thickness of 150µm. ✕ marks the center of the through holes.

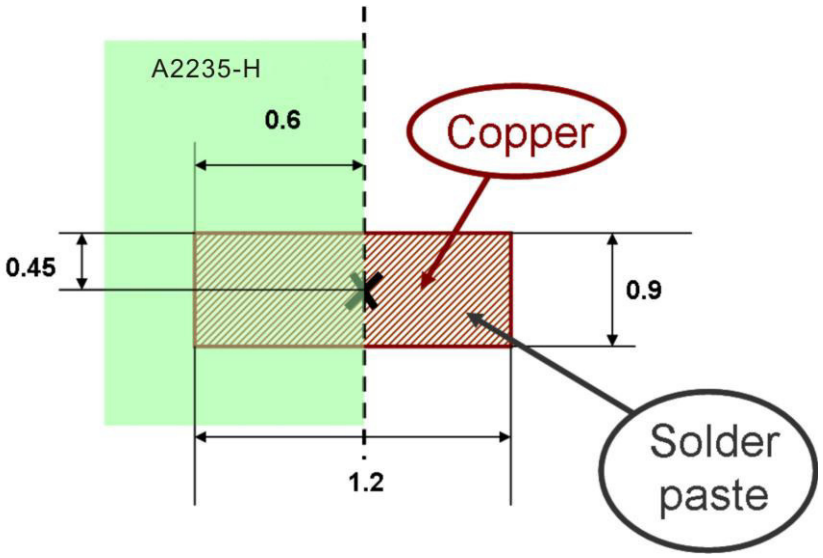


Figure 11: Proposal of Soldering footprint

Please note that copper and solder paste footprints are identical. The final footprint has to be evaluated and qualified by the manufacturer according to the specific process.

7.2 PCB Design Guide

1. Drill a through hole with diameter greater than or equal to 3mm in the application PCB which is underneath the RF feed-point to alleviate the interference from RF signal to other part of circuitries. Besides, ground vias (says, 8) should be placed surrounding the through hole for further shielding purpose.

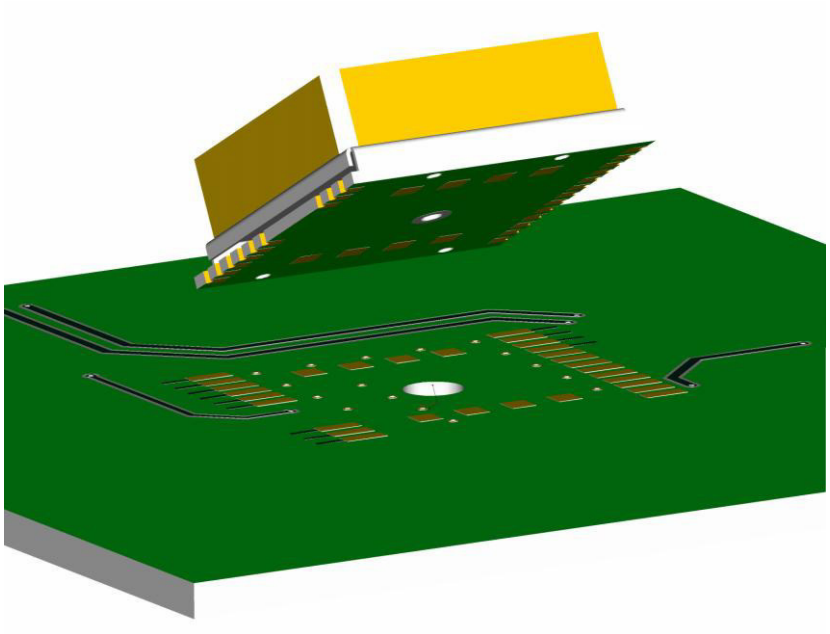


Figure 12: Proposal (1) of the PCB design

2. If proposal 1 is not allowed. Placed a round Copper keep out region (diameter ≥3mm) on the application PCB underneath the RF feed-point to alleviate the interference from RF signal to other part of circuitries. Besides, ground vias (says, 8) should be placed surrounding the through hole for further shielding purpose.

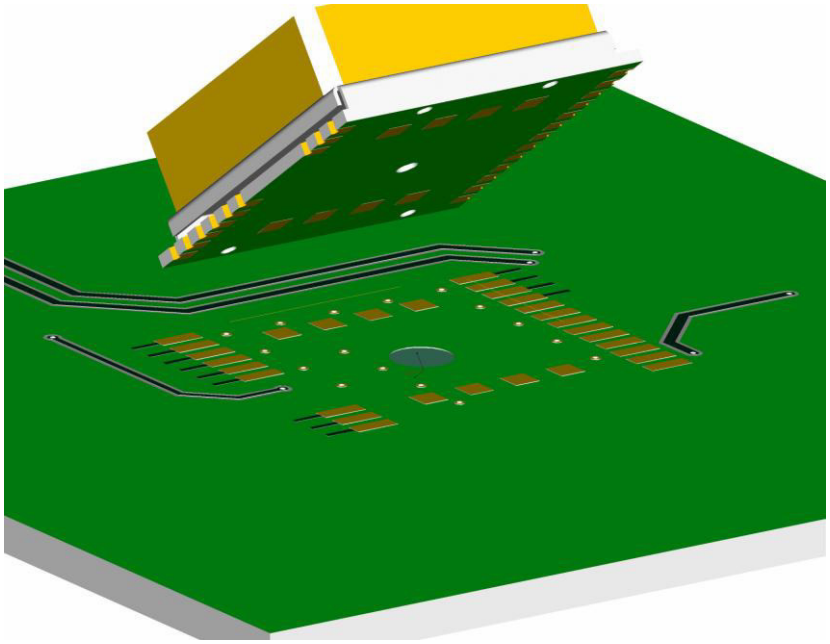


Figure 13: Proposal (2) of the PCB design

7.3 Recommended Profile for Reflow Soldering

Typical values for reflow soldering of the module in convection or IR/convection ovens are as follows (according to IPC/JEDEC J-STD-020D):

Parameter	Value
Peak temperature (RoHS compliant process)	245°C
Average ramp up rate to peak (217°C to Peak)	3°C / second max.
Preheat temperature	min=150°C; max=200°C
Ramp up time from min. to max. preheat temperature	60 … 120 seconds
Temperature maintained above 217°C	60 … 150 seconds
Time within 5°C of actual peak temperature	30 seconds
Ramp down rate	6°C / second max.
Time 25°C to peak temperature	8 minutes max.

Table 9: Reflow soldering profile A2235-H

As results of soldering may vary among different soldering systems and types of solder and depend on additional factors like density and types of components on board, the values above should be considered as a starting point for further optimization.

8 Use of External Antenna

8.1 Connection of RF Signal

The ANT_EXT pin is used to connect the receiver with the GPS antenna. The design of the antenna connection has to be strictly done according to RF design rules. A 50 Ω PCB strip line is required. The following drawings shall explain the guidelines. A major rule is to keep the strip line as short as possible. Additionally, Strip line needs a good reference ground.

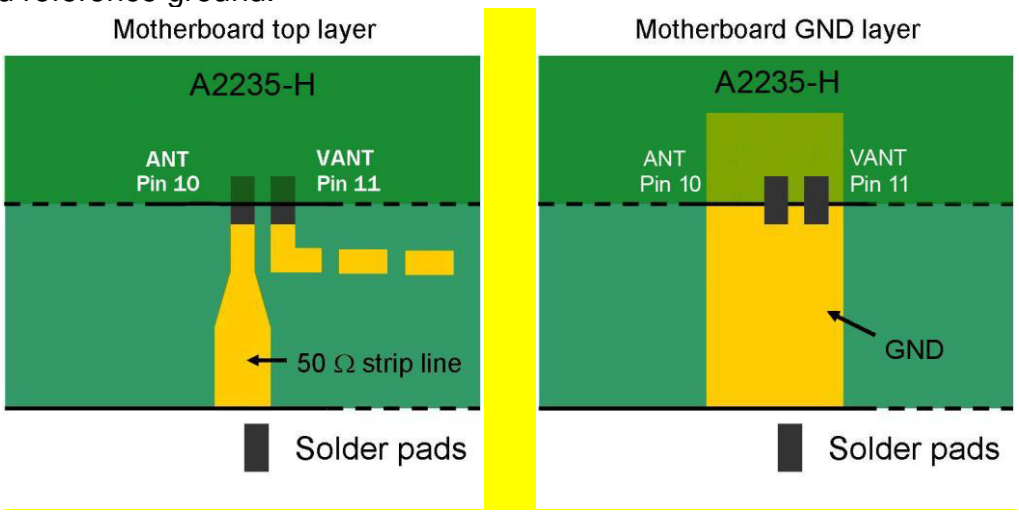


Figure 14: Antenna connector strip line A2235-H

In order to achieve the impedance of 50 Ω, the width of the strip line needs to be calculated. It depends on the thickness or height of the PCB layer (both parameters are shown in following drawing). For the calculation, it is assumed that the PCB material is FR4.

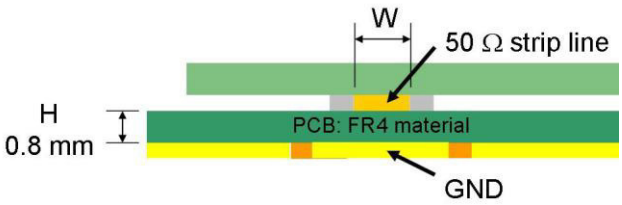


Figure 15: Strip line parameters A2235-H

In this case, the width should be about 1.8 times the height of the PCB:

$$W = 1.8 \times H$$

In the example, one would get a width of W = 1.8 x 0.8 mm = 1.44 mm.

8.2 External Antenna

8.2.1 Recommended Parameters

General GPS active antenna specification:

Limitations:

- Supply voltage according to voltage fed into VANT pin (5 V max.)
- Supply current 50 mA (max.)

Recommendations:

- Gain ≥ 20 dB (should not exceed 35 dB)
- Noise figure ≤ 1.5 dB

The recommendations apply to the majority of active antennas that can be found in the market. The quality and suitability of the GPS antenna chosen is off great importance to the overall sensitivity of the GPS system.

The system design needs to reflect the supply voltage of the antenna. If the supply voltage is equal to Vcc, then it could be connected to VANT. If the antenna requires a different supply voltage, the antenna bias can be provided through the VANT pin.

8.2.2 Hints

Unused antenna inputs should be terminated with 50 Ω ± 20%. Do not feed the antenna supply voltage into terminated antenna inputs.

9 Quality and Reliability

9.1 Environmental Conditions

Operating temperature	-40°C … +85°C
Operating humidity	Max. 85% r. H., non-condensing, at 85°C
MSL JEDEC (Moisture Sensitivity Level)	3
Storage	6 months in original package

Table 10: Environmental conditions

9.2 Product Qualification

Prior to product qualification the GPS receiver is preconditioned according to EIA/JEDEC standard JESD22-A113-B / Level 3.

Basic qualification tests:

- MSL Classification according to J-STD-020C (MSL3 @ 245°C)
  (Refer to report: SZRL2011110048)
- MSL Rework Compatibility according to J-STD-020C
  (Refer to report: SZRL2011110048)
- Temperature Cycling –40°C … +85°C
- Temperature Humidity Bias 70°C / 85% RH
- Low / High Temperature Operating –40°C / +85°C
- High Temperature Operating Life +85°C
- Vibration Variable Frequency
- Mechanical Shock

Please contact Maestro for detailed information.

9.3 Production Test

Each module is electrically tested prior to packing and shipping to ensure state of the art GPS receiver performance and accuracy.

10 Applications and Hints

10.1 Initial Module Start

After initially applying power to the module, it is necessary to start the internal firmware by toggling the ON_OFF pin. Toggling is done by pulling the signal to HIGH for about 200ms. This first toggling can be done after a LOW – HIGH transmission was detected at the WAKEUP pin or by simply waiting for 1s after power-up. In UART mode, output messages should immediately be displayed. If no messages then a new toggling should be applied.

10.2 Proper Shutdown and Power-On-Reset (POR)

The A2235-H modules require an orderly shutdown process to properly stop internal operation and complete any writes of critical data to BBRAM or EEPROM data area. Abrupt removal or drop of main power while the system is running has risks ranging from minor impact on TTFF to fatal, permanent corruption of EEPROM code area on the module (Please refer to “Power ONOFF Sequences and Power -On-Reset (POR) on A2100-AB Application Notes”).

A controlled and orderly shutdown while the A2235-H is running in full power mode can be initiated by

- A 200ms pulse on the ON_OFF pin, or
- Appropriate messages either in NMEA or OSP mode.

The shutdown is completed after maximum 1s. Therefore the module should be supplied with voltage for that time after the shutdown sequence was initiated.

10.3 SiRFaware™ Support

SiRFaware™ is a low-power operating mode that seeks to maintain low uncertainty in position, time, and frequency, and to maintain valid current Ephemeris using either data collected from satellites in view or Extended Ephemeris methods.

The SiRFaware™ mode is entered using the One Socket Protocol, an extension of the SiRF Binary Protocol. Please refer to the appropriate manual. In order to request a fix and to exit SiRFaware™ it is necessary to toggle the ON_OFF pin. Toggling is done by pulling the signal to HIGH for about 200ms.

10.4 Push-to-Fix Mode

Push-to-Fix mode is designed for the application that requires infrequent position reporting. The receiver generally stays in a low-power mode, up to 2 hours, but wakes up periodically to refresh position, time, ephemeris data and RTC calibration.

The push-to-fix mode is initialized and entered using the SiRF Binary Protocol. Please refer to the appropriate manual, paying particular attention to the paragraph titled “Set TricklePower Parameters”. In order to request a fix outside the specified duty cycles, it is necessary to toggle the ON_OFF pin. Toggling is done by pulling the signal to HIGH for about 200ms.

10.5 Hibernate Mode

In order to enter Hibernate Mode it is necessary to send a shutdown command or to toggle to ON_OFF pin by pulling the signal to HIGH for about 200ms. Starting with firmware version 4.0.1 the according command is supported in NMEA and SiRF Binary mode. After a short delay the module will switch into hibernate mode. The RTC will keep on running and SRAM is backed with the typical current of 20 µA drawn from Vcc. To wake the module up again, toggling the ON_OFF pin is necessary (200ms pulse width).

10.6 Extended Ephemeris

The receiver is capable of supporting two versions of using Extended Ephemeris (EE) data. The first one is the version, where the EE data are calculated on a server, are transmitted to device incorporating the receiver, and are then loaded into the receiver. These data can be valid for up to seven days.

The second version is the internal extrapolation of available “natural” Ephemeris data. This is done automatically and no external support is required. The internally calculated EE data are valid for up to 3 days.

The receiver firmware will define which set of EE data to use or will neglect those in case “natural” data are available (need add an external EEPROM part). Both versions of EE data will help to further lower power consumption in SiRFaware™ mode.

10.7 TM_GPIO5 pin (1 pulse per second pin)

The 1PPS pin is an output pin.

In addition to precise positioning, GPS also allows for accurate timing due to the synchronized atomic clocks in the GPS satellites. While the current date and time is transmitted in NMEA sentences (UTC), an exact and accurate timing signal is provided via the 1PPS pin of the A2235-H GPS receiver.

Under good signal conditions the 1PPS signal comes between 620ns and 710ns after the full GPS system second which is accurately (around 10ns) synchronized to UTC. Therefore the 1 second clock can be derived and maintained within around 90ns under good signal conditions.

Note:
The 1PPS clock accuracy directly depends on the position accuracy!

The GPS signals travel at the speed of light, therefore a position inaccuracy directly translates into 1PPS inaccuracies.

10m position deviation ≈ 33ns 1PPS deviation (typically)
100m position deviation ≈ 333ns 1PPS deviation (typically)

The NMEA messages containing absolute timing information (UTC time) are provided around 300ms after the 1PPS signal typically. This may change with the GPS receiver setup.

The 1PPS signal is provided on a “as is” basis with no accuracy specification. It’s NOT recommended to use 1PPS signal for accurate timing application.
The given values are based on a 10 satellite, static GPS simulator scenario.

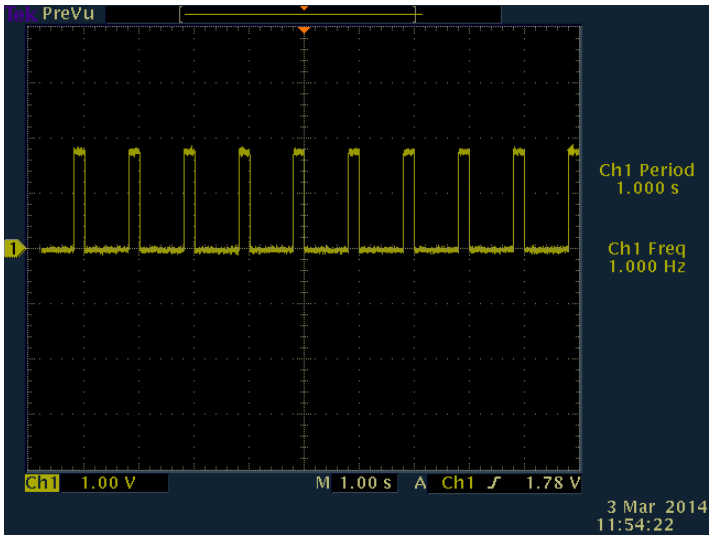


Figure 16: 1PPS waveform (reference)

10.8 5 Hz Navigation Update Rate

User can select 1Hz or 5Hz output rate of navigation computation and message, it supports rapid change of direction and improves accuracy on sport-related applications.1Hz is the default Navigation Update Rate, If the user want to change to 5Hz Navigation Update Rate, Please refer to command below:

Enable 5Hz Navigation Update Rate command

- NMEA command MID103 ($PSRF103,00,6,00,0*23)
- OSP command MID136 (A0 A2 00 0E 88 00 00 04 04 00 00 00 00 00 00 00 0F 02 00 A1 B0 B3)

Disable 5Hz and return to 1Hz Navigation Update Rate, command:

- NMEA command MID103 ($PSRF103,00,7,00,0*22)
- OSP command MID136 (A0 A2 00 0E 88 00 00 04 00 00 00 00 00 00 00 00 0F 02 00 9D B0 B3)

11 Evaluation Kit EVA2235-H

For demonstration and easy evaluation of GPS performance Maestro offers an evaluation kit (including one GPS A2235-H module). It contains a USB interface with according drivers to connect easily to a PC. The USB interface is an extension of the serial port 0, therefore sending NMEA sentences and accepting commands. At the same time it provides power to the module. Accompanied by an antenna it offers a ready-to-go set.

For the development of new software and applications the Evaluation Kit also provides NMEA messages on CMOS level via a terminal plug.

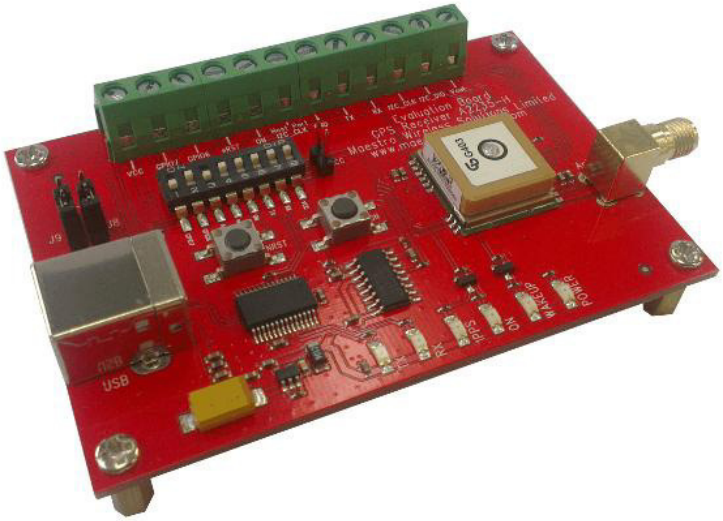


Figure 17: Evaluation kit EVA2235-H

For further information please contact Maestro.

12 Related Information

12.1 Contact

This manual was created with due diligence. We hope that it will be helpful to the user to get the most out of the GPS module.

Any inputs regarding possible errors or mistakable verbalizations, and comments or proposals for further improvements to this document, made to Maestro, HongKong, are highly appreciated.

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Fax: (852)25254701

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www.maestro-wireless.com

12.2 Related Documents

- GPS Evaluation Kit EVA2235-H (Maestro)
- Power ONOFF Sequences and Power-On-Reset (POR) on A2100-AB (Maestro)
- SiRF_OSP_Reference_Manual (SiRF)
- SiRF_NMEA_Reference_Manual (SiRF)

12.3 Related Tools

- GPS Cockpit (Maestro)
- SiRFLive (SiRF)

13 List of Figures

14 List of Tables

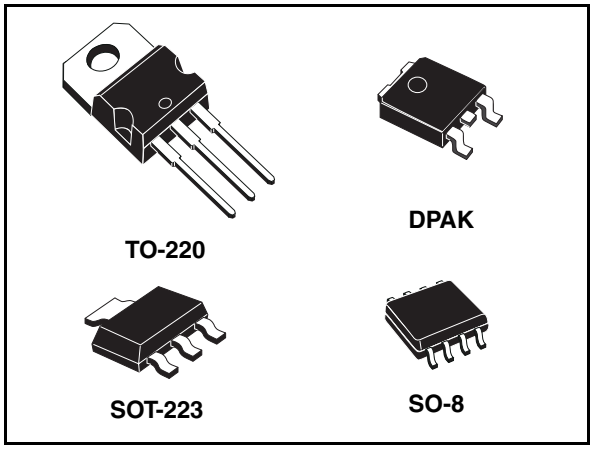
2.2.3. Regulador de tensión

LD1117 series

Low drop fixed and adjustable positive voltage regulators

Feature summary

- Low dropout voltage (1V TYP.)
- 2.85V Device performances are suitable for SCSI-2 active termination
- Output current up to 800 mA
- Fixed output voltage of: 1.2V, 1.8V, 2.5V, 2.85V, 3.0V, 3.3V, 5.0V
- Adjustable version availability (V_{rel}=1.25V)
- Internal current and thermal limit
- Available in ± 1% (at 25°C) and 2% in full temperature range
- Supply voltage rejection: 75dB (typ.)

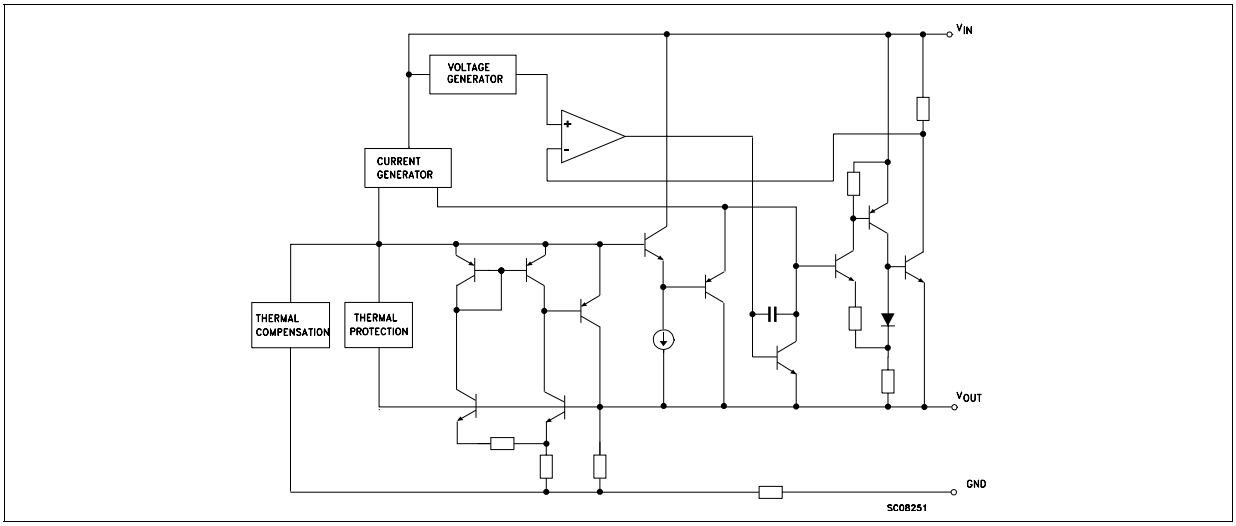


Description

The LD1117 is a LOW DROP Voltage Regulator able to provide up to 800mA of Output Current, available even in adjustable version (Vref=1.25V). Concerning fixed versions, are offered the following Output Voltages: 1.2V,1.8V,2.5V,2.85V, 3.0V 3.3V and 5.0V. The 2.85V type is ideal for SCSI-2 lines active termination. The device is supplied in: SOT-223, DPAK, SO-8 and TO-220.

The SOT-223 and DPAK surface mount packages optimize the thermal characteristics even offering a relevant space saving effect. High efficiency is assured by NPN pass transistor. In fact in this case, unlike than PNP one, the Quiescent Current flows mostly into the load. Only a very common 10µF minimum capacitor is needed for stability. On chip trimming allows the regulator to reach a very tight output voltage tolerance, within ± 1% at 25°C. The ADJUSTABLE LD1117 is pin to pin compatible with the other standard. Adjustable voltage regulators maintaining the better performances in terms of Drop and Tolerance.

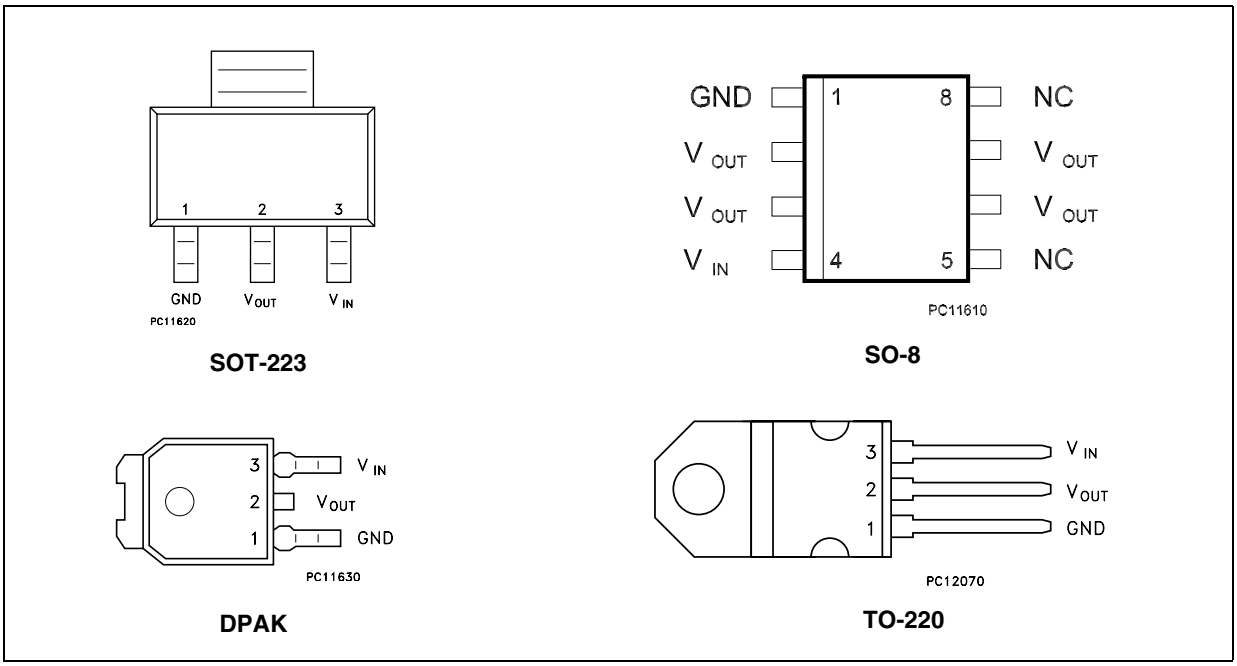
Block diagram



Contents

1 Pin configuration

Figure 1. Pin connections (top view)



Note: The TAB is connected to the V_{OUT}.

2 Maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{IN}	DC Input Voltage		15	V
P_{TOT}	Power Dissipation		12	W
T_{STG}	Storage Temperature Range		-40 to +150	°C
T_{OP}	Operating Junction Temperature Range	for C Version	-40 to +150	°C
		for standard Version	0 to +150	°C

Table 2. Thermal Data

Symbol	Parameter	SOT-223	SO-8	DPAK	TO-220	Unit
R_{thJC}	Thermal Resistance Junction-case	15	20	8	3	°C/W
R_{thJA}	Thermal Resistance Junction-ambient				50	°C/W

3 Schematic application

Figure 2. Application circuit (for 1.2V)

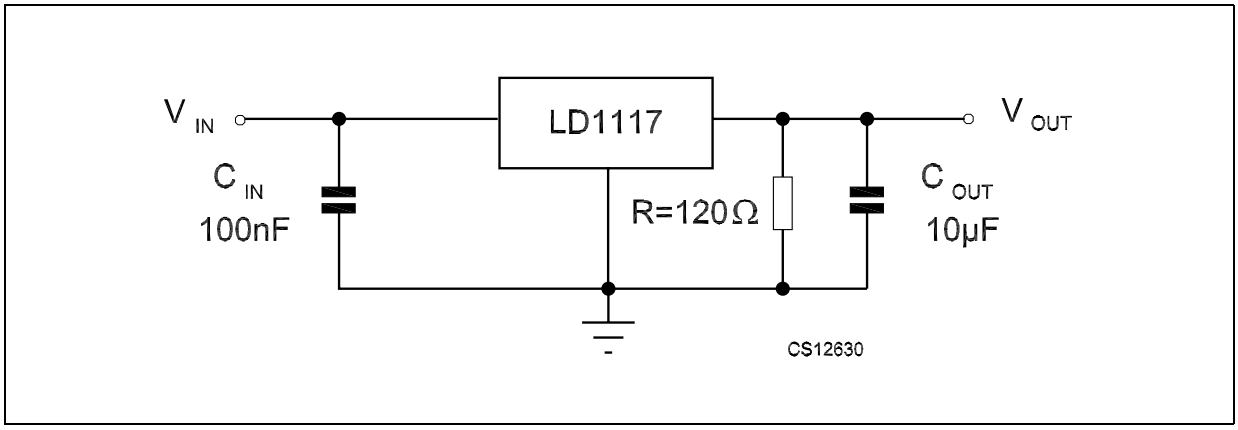
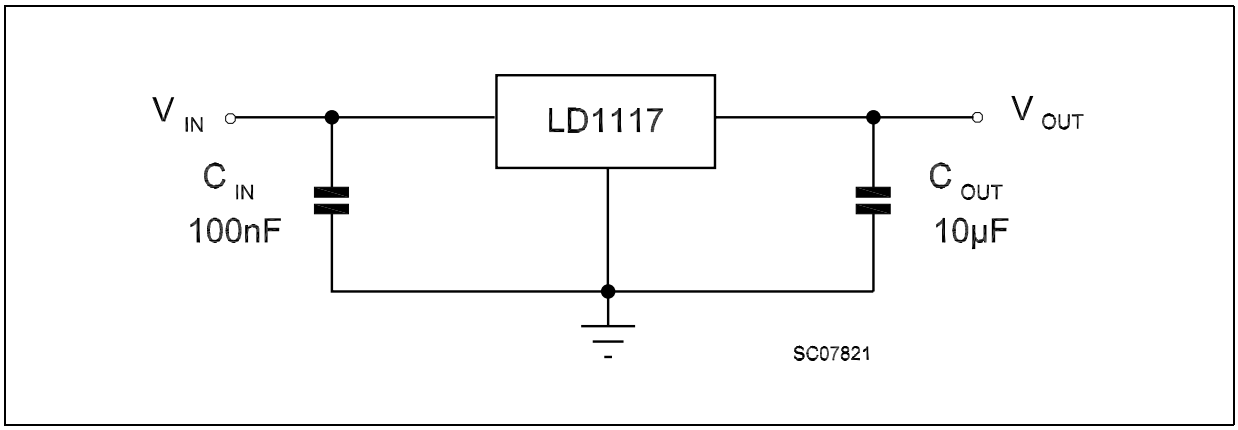


Figure 3. Application circuit (for other fixed output voltages)



4 Electrical characteristics

Table 3. Electrical characteristics of LD1117#12
(refer to the test circuits, T_J = 0 to 125°C, C_O = 10 µF, R = 120 Ω between GND and OUT pins, unless otherwise specified).

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_{in} = 3.2 V, I_O = 10 mA, T_J = 25°C	1.188	1.20	1.212	V
V_O	Reference voltage	I_O = 10 to 800 mA V_{in} - V_O= 1.4 to 10 V	1.140	1.20	1.260	V
ΔV_O	Line regulation	V_{in} - V_O = 1.5 to 13.75 V, I_O = 10 mA		0.035	0.2	%
ΔV_O	Load regulation	V_{in} - V_O = 3 V, I_O = 10 to 800 mA		0.1	0.4	%
ΔV_O	Temperature stability			0.5		%
ΔV_O	Long term stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating input voltage				15	V
I_{adj}	Adjustment pin current	V_{in} ≤15 V		60	120	µA
ΔI_{adj}	Adjustment pin current change	V_{in} - V_O = 1.4 to 10 V I_O = 10 to 800 mA		1	5	µA
$I_{O(min)}$	Minimum load current	V_{in} = 15 V		2	5	mA
I_O	Output current	V_{in} - V_O = 5 V, T_J = 25°C	800	950	1300	mA
eN	Output noise (%V_O)	B =10Hz to 10KHz, T_J = 25°C		0.003		%
SVR	Supply voltage rejection	I_O = 40 mA, f = 120Hz, T_J = 25°C V_{in} - V_O = 3 V, V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout voltage	I_O = 100 mA		1	1.1	V
		I_O = 500 mA		1.05	1.15	
		I_O = 800 mA		1.10	1.2	
	Thermal regulation	T_a = 25°C, 30ms Pulse		0.01	0.1	%/W

Table 4. Electrical characteristics of LD1117#18
(refer to the test circuits, T_J = 0 to 125°C, C_O = 10 µF, unless otherwise specified).

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_{in} = 3.8 V, I_O = 10 mA, T_J = 25°C	1.78	1.8	1.82	V
V_O	Output voltage	I_O = 0 to 800 mA, V_{in} = 3.3 to 8 V	1.76		1.84	V
ΔV_O	Line regulation	V_{in} = 3.3 to 8 V, I_O = 0 mA		1	6	mV
ΔV_O	Load regulation	V_{in} = 3.3 V, I_O = 0 to 800 mA		1	10	mV
ΔV_O	Temperature stability			0.5		%
ΔV_O	Long term stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating input voltage	I_O = 100 mA			10	V
I_d	Quiescent current	$V_{in} \leq$8 V		5	10	mA
I_O	Output current	V_{in} = 6.8 V, T_J = 25°C	800	950	1300	mA
eN	Output noise voltage	B =10Hz to 10KHz, T_J = 25°C		100		µV
SVR	Supply voltage rejection	I_O = 40 mA, f = 120Hz, T_J = 25°C V_{in} = 5.5 V, V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout voltage	I_O = 100 mA		1	1.1	V
		I_O = 500 mA		1.05	1.15	
		I_O = 800 mA		1.10	1.2	
	Thermal regulation	T_a = 25°C, 30ms Pulse		0.01	0.1	%/W

Table 5. Electrical characteristics of LD1117#25
(refer to the test circuits, T_J = 0 to 125°C, C_O = 10 µF, unless otherwise specified).

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_{in} = 4.5 V, I_O = 10 mA, T_J = 25°C	2.475	2.5	2.525	V
V_O	Output voltage	I_O = 0 to 800 mA, V_{in} = 3.9 to 10 V	2.45		2.55	V
ΔV_O	Line regulation	V_{in} = 3.9 to 10 V, I_O = 0 mA		1	6	mV
ΔV_O	Load regulation	V_{in} = 3.9 V, I_O = 0 to 800 mA		1	10	mV
ΔV_O	Temperature stability			0.5		%
ΔV_O	Long term stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating input voltage	I_O = 100 mA			15	V
I_d	Quiescent current	$V_{in} \leq$10 V		5	10	mA
I_O	Output current	V_{in} = 7.5 VT_J = 25°C	800	950	1300	mA
eN	Output noise voltage	B =10Hz to 10KHz, T_J = 25°C		100		µV
SVR	Supply voltage rejection	I_O = 40 mA, f = 120Hz, T_J = 25°C V_{in} = 5.5 V, V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout voltage	I_O = 100 mA		1	1.1	V
		I_O = 500 mA		1.05	1.15	
		I_O = 800 mA		1.10	1.2	
	Thermal regulation	T_a = 25°C, 30ms Pulse		0.01	0.1	%/W

Table 6. Electrical characteristics of LD1117#28
(refer to the test circuits, T_J = 0 to 125°C, C_O = 10 µF, unless otherwise specified).

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_{in} = 4.85 V, I_O = 10 mA, T_J = 25°C	2.82	2.85	2.88	V
V_O	Output voltage	I_O = 0 to 800 mA, V_{in} = 4.25 to 10 V	2.79		2.91	V
ΔV_O	Line regulation	V_{in} = 4.25 to 10 V, I_O = 0 mA		1	6	mV
ΔV_O	Load regulation	V_{in} = 4.25 V, I_O = 0 to 800 mA		1	10	mV
ΔV_O	Temperature stability			0.5		%
ΔV_O	Long term stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating input voltage	I_O = 100 mA			15	V
I_d	Quiescent current	V_{in} ≤10 V		5	10	mA
I_O	Output current	V_{in} = 7.85 VT_J = 25°C	800	950	1300	mA
eN	Output noise voltage	B =10Hz to 10KHz, T_J = 25°C		100		µV
SVR	Supply voltage rejection	I_O = 40 mA, f = 120Hz, T_J = 25°C V_{in} = 5.85 V, V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout voltage	I_O = 100 mA		1	1.1	V
		I_O = 500 mA		1.05	1.15	
		I_O = 800 mA		1.10	1.2	
	Thermal regulation	T_a = 25°C, 30ms Pulse		0.01	0.1	%/W

Table 7. Electrical characteristics of LD1117#30
(refer to the test circuits, T_J = 0 to 125°C, C_O = 10 µF, unless otherwise specified).

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_{in} = 5 V, I_O = 10 mA, T_J = 25°C	2.97	3	3.03	V
V_O	Output voltage	I_O = 0 to 800 mA, V_{in} = 4.5 to 10 V	2.94		3.06	V
ΔV_O	Line regulation	V_{in} = 4.5 to 12 V, I_O = 0 mA		1	6	mV
ΔV_O	Load regulation	V_{in} = 4.5 V, I_O = 0 to 800 mA		1	10	mV
ΔV_O	Temperature stability			0.5		%
ΔV_O	Long term stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating input voltage	I_O = 100 mA			15	V
I_d	Quiescent current	V_{in} ≤12 V		5	10	mA
I_O	Output current	V_{in} = 8 V, T_J = 25°C	800	950	1300	mA
eN	Output noise voltage	B =10Hz to 10KHz,T_J = 25°C		100		µV
SVR	Supply voltage rejection	I_O = 40 mA, f = 120Hz, T_J = 25°C V_{in} = 6 V, V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout voltage	I_O = 100 mA		1	1.1	V
		I_O = 500 mA		1.05	1.15	
		I_O = 800 mA		1.10	1.2	
	Thermal regulation	T_a = 25°C, 30ms Pulse		0.01	0.1	%/W

Table 8. Electrical characteristics of LD1117#33
(refer to the test circuits, T_J = 0 to 125°C, C_O = 10 µF, unless otherwise specified).

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_{in} = 5.3 V, I_O = 10 mA, T_J = 25°C	3.267	3.3	3.333	V
V_O	Output voltage	I_O = 0 to 800 mA, V_{in} = 4.75 to 10 V	3.235		3.365	V
ΔV_O	Line regulation	V_{in} = 4.75 to 15 V, I_O = 0 mA		1	6	mV
ΔV_O	Load regulation	V_{in} = 4.75 V, I_O = 0 to 800 mA		1	10	mV
ΔV_O	Temperature stability			0.5		%
ΔV_O	Long term stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating input voltage	I_O = 100 mA			15	V
I_d	Quiescent current	V_{in} ≤15 V		5	10	mA
I_O	Output current	V_{in} = 8.3 V, T_J = 25°C	800	950	1300	mA
eN	Output noise voltage	B =10Hz to 10KHz, T_J = 25°C		100		µV
SVR	Supply voltage rejection	I_O = 40 mA, f = 120Hz, T_J = 25°C V_{in} = 6.3 V, V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout voltage	I_O = 100 mA		1	1.1	V
		I_O = 500 mA		1.05	1.15	
		I_O = 800 mA		1.10	1.2	
	Thermal regulation	T_a = 25°C, 30ms Pulse		0.01	0.1	%/W

Table 9. Electrical characteristics of LD1117#50
(refer to the test circuits, T_J = 0 to 125°C, C_O = 10 µF, unless otherwise specified).

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_{in} = 7 V, I_O = 10 mA, T_J = 25°C	4.95	5	5.05	V
V_O	Output voltage	I_O = 0 to 800 mA, V_{in} = 6.5 to 15 V	4.9		5.1	V
ΔV_O	Line regulation	V_{in} = 6.5 to 15 V, I_O = 0 mA		1	10	mV
ΔV_O	Load regulation	V_{in} = 6.5 V, I_O = 0 to 800 mA		1	15	mV
ΔV_O	Temperature stability			0.5		%
ΔV_O	Long term stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating input voltage	I_O = 100 mA			15	V
I_d	Quiescent current	V_{in} ≤15 V		5	10	mA
I_O	Output current	V_{in} = 10 V, T_J = 25°C	800	950	1300	mA
eN	Output noise voltage	B =10Hz to 10KHz, T_J = 25°C		100		µV
SVR	Supply voltage rejection	I_O = 40 mA, f = 120Hz, T_J = 25°C V_{in} = 8 V, V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout voltage	I_O = 100 mA		1	1.1	V
		I_O = 500 mA		1.05	1.15	
		I_O = 800 mA		1.10	1.2	
	Thermal regulation	T_a = 25°C, 30ms Pulse		0.01	0.1	%/W

Table 10. Electrical characteristics of LD1117 (Adjustable)
(refer to the test circuits, T_J = 0 to 125°C, C_O = 10 µF, unless otherwise specified).

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
V_{ref}	Reference voltage	V_{in} - V_O = 2 V, I_O = 10 mA, T_J = 25°C	1.238	1.25	1.262	V
V_{ref}	Reference voltage	I_O = 10 to 800 mA, V_{in} - V_O = 1.4 to 10 V	1.225		1.275	V
ΔV_O	Line regulation	V_{in} - V_O = 1.5 to 13.75 V, I_O = 10 mA		0.035	0.2	%
ΔV_O	Load regulation	V_{in} - V_O = 3 V, I_O = 10 to 800 mA		0.1	0.4	%
ΔV_O	Temperature stability			0.5		%
ΔV_O	Long term stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating input voltage				15	V
I_{adj}	Adjustment pin current	V_{in} ≤15 V		60	120	µA
ΔI_{adj}	Adjustment pin current change	V_{in} - V_O = 1.4 to 10 V, I_O = 10 to 800 mA		1	5	µA
$I_{O(min)}$	Minimum load current	V_{in} = 15 V		2	5	mA
I_O	Output current	V_{in} - V_O = 5 V, T_J = 25°C	800	950	1300	mA
eN	Output noise (%V_O)	B =10Hz to 10KHz, T_J = 25°C		0.003		%
SVR	Supply voltage rejection	I_O = 40 mA, f = 120Hz, T_J = 25°C V_{in} - V_O = 3 V, V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout voltage	I_O = 100 mA		1	1.1	V
		I_O = 500 mA		1.05	1.15	
		I_O = 800 mA		1.10	1.2	
	Thermal regulation	T_a = 25°C, 30ms Pulse		0.01	0.1	%/W

Table 11. Electrical characteristics of LD1117#12C
(refer to the test circuits, T_J = 0 to 125°C, C_O = 10 µF, R = 120 Ω between GND and OUT pins, unless otherwise specified).

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
V_{ref}	Reference voltage	V_{in} - V_O= 2V, I_O = 10 mA, T_J = 25°C	1.176	1.20	1.224	V
V_{ref}	Reference voltage	I_O = 10 to 800 mA, V_{in} - V_O= 1.4 to 10 V	1.120	1.20	1.280	V
ΔV_O	Line regulation	V_{in} - V_O = 1.5 to 13.75 V, I_O = 10 mA			1	%
ΔV_O	Load regulation	V_{in} - V_O = 3 V, I_O = 10 to 800 mA			1	%
ΔV_O	Temperature stability			0.5		%
ΔV_O	Long term stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating input voltage				15	V
I_{adj}	Adjustment pin current	V_{in} ≤15 V		60	120	µA
ΔI_{adj}	Adjustment pin current change	V_{in} - V_O = 1.4 to 10 V I_O = 10 to 800 mA		1	5	µA
$I_{O(min)}$	Minimum load current	V_{in} = 15 V		2	5	mA
I_O	Output current	V_{in} - V_O = 5 V, T_J = 25°C	800	950	1300	mA
eN	Output noise (%V_O)	B =10Hz to 10KHz, T_J = 25°C		0.003		%
SVR	Supply voltage rejection	I_O = 40 mA, f = 120Hz, T_J = 25°C V_{in} - V_O = 3 V, V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout voltage	I_O = 100 mA, T_J = 0 to 125°C		1	1.1	V
		I_O = 500 mA, T_J = 0 to 125°C		1.05	1.2	
		I_O = 800 mA, T_J = 0 to 125°C		1.10	1.3	
	Thermal regulation	T_a = 25°C, 30ms Pulse		0.01	0.1	%/W

Table 12. Electrical characteristics of LD1117#18C
(refer to the test circuits, T_J = -40 to 125°C, C_O = 10 µF, unless otherwise specified).

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_{in} = 3.8 V, I_O = 10 mA, T_J = 25°C	1.76	1.8	1.84	V
V_O	Output voltage	I_O = 0 to 800 mA, V_{in} = 3.9 to 10 V	1.73		1.87	V
ΔV_O	Line regulation	V_{in} = 3.3 to 8 V, I_O = 0 mA		1	30	mV
ΔV_O	Load regulation	V_{in} = 3.3 V, I_O = 0 to 800 mA		1	30	mV
ΔV_O	Temperature stability			0.5		%
ΔV_O	Long term stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating input voltage	I_O = 100 mA			10	V
I_d	Quiescent current	$V_{in} \leq$8 V		5	10	mA
I_O	Output current	V_{in} = 6.8 VT_J = 25°C	800	950	1300	mA
eN	Output noise voltage	B =10Hz to 10KHz, T_J = 25°C		100		µV
SVR	Supply voltage rejection	I_O = 40 mA, f = 120Hz, T_J = 25°C V_{in} = 5.5 V, V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout voltage	I_O = 100 mA, T_J = 0 to 125°C		1	1.1	V
		I_O = 500 mA, T_J = 0 to 125°C		1.05	1.15	
		I_O = 800 mA, T_J = 0 to 125°C		1.10	1.2	
V_d	Dropout voltage	I_O = 100 mA			1.1	V
		I_O = 500 mA			1.2	
		I_O = 800 mA			1.3	
	Thermal regulation	T_a = 25°C, 30ms Pulse		0.01	0.1	%/W

Table 13. Electrical characteristics of LD1117#25C
(refer to the test circuits, T_J = -40 to 125°C, C_O = 10 µF, unless otherwise specified).

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_{in} = 4.5 V, I_O = 10 mA, T_J = 25°C	2.45	2.5	2.55	V
V_O	Output voltage	I_O = 0 to 800 mA, V_{in} = 3.9 to 10 V	2.4		2.6	V
ΔV_O	Line regulation	V_{in} = 3.9 to 10 V, I_O = 0 mA		1	30	mV
ΔV_O	Load regulation	V_{in} = 3.9 V, I_O = 0 to 800 mA		1	30	mV
ΔV_O	Temperature stability			0.5		%
ΔV_O	Long term stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating input voltage	I_O = 100 mA			15	V
I_d	Quiescent current	V_{in} ≤10 V		5	10	mA
I_O	Output current	V_{in} = 7.5 VT_J = 25°C	800	950	1300	mA
eN	Output noise voltage	B =10Hz to 10KHz, T_J = 25°C		100		µV
SVR	Supply voltage rejection	I_O = 40 mA, f = 120Hz, T_J = 25°C V_{in} = 5.5 V, V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout voltage	I_O = 100 mA, T_J = 0 to 125°C		1	1.1	V
		I_O = 500 mA, T_J = 0 to 125°C		1.05	1.15	
		I_O = 800 mA, T_J = 0 to 125°C		1.10	1.2	
V_d	Dropout voltage	I_O = 100 mA			1.1	V
		I_O = 500 mA			1.2	
		I_O = 800 mA			1.3	
	Thermal regulation	T_a = 25°C, 30ms Pulse		0.01	0.1	%/W

Table 14. Electrical characteristics of LD1117#30C
(refer to the test circuits, T_J = -40 to 125°C, C_O = 10 µF, unless otherwise specified).

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_{in} = 5 V, I_O = 10 mA, T_J = 25°C	2.94	3	3.06	V
V_O	Output voltage	I_O = 0 to 800 mA, V_{in} = 4.5 to 10 V	2.88		3.12	V
ΔV_O	Line regulation	V_{in} = 4.5 to 12 V, I_O = 0 mA		1	30	mV
ΔV_O	Load regulation	V_{in} = 4.5 V, I_O = 0 to 800 mA		1	30	mV
ΔV_O	Temperature stability			0.5		%
ΔV_O	Long term stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating input voltage	I_O = 100 mA			15	V
I_d	Quiescent current	V_{in} ≤12 V		5	10	mA
I_O	Output current	V_{in} = 8 V, T_J = 25°C	800	950	1300	mA
eN	Output noise voltage	B =10Hz to 10KHz, T_J = 25°C		100		µV
SVR	Supply voltage rejection	I_O = 40 mA, f = 120Hz, T_J = 25°C V_{in} = 6 V, V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout voltage	I_O = 100 mA, T_J = 0 to 125°C		1	1.1	V
		I_O = 500 mA, T_J = 0 to 125°C		1.05	1.15	
		I_O = 800 mA, T_J = 0 to 125°C		1.10	1.2	
V_d	Dropout voltage	I_O = 100 mA			1.1	V
		I_O = 500 mA			1.2	
		I_O = 800 mA			1.3	
	Thermal regulation	T_a = 25°C, 30ms Pulse		0.01	0.1	%/W

Table 15. Electrical characteristics of LD1117#33C
(refer to the test circuits, T_J = -40 to 125°C, C_O = 10 µF, unless otherwise specified).

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_{in} = 5.3 V, I_O = 10 mA, T_J = 25°C	3.24	3.3	3.36	V
V_O	Output voltage	I_O = 0 to 800 mA, V_{in} = 4.75 to 10 V	3.16		3.44	V
ΔV_O	Line regulation	V_{in} = 4.75 to 15 V, I_O = 0 mA		1	30	mV
ΔV_O	Load regulation	V_{in} = 4.75 V, I_O = 0 to 800 mA		1	30	mV
ΔV_O	Temperature stability			0.5		%
ΔV_O	Long term stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating input voltage	I_O = 100 mA			15	V
I_d	Quiescent current	V_{in} ≤15 V		5	10	mA
I_O	Output current	V_{in} = 8.3 V, T_J = 25°C	800	950	1300	mA
eN	Output noise voltage	B =10Hz to 10KHz, T_J = 25°C		100		µV
SVR	Supply voltage rejection	I_O = 40 mA, f = 120Hz, T_J = 25°C V_{in} = 6.3 V, V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout voltage	I_O = 100 mA, T_J = 0 to 125°C		1	1.1	V
		I_O = 500 mA, T_J = 0 to 125°C		1.05	1.15	
		I_O = 800 mA, T_J = 0 to 125°C		1.10	1.2	
V_d	Dropout voltage	I_O = 100 mA			1.1	V
		I_O = 500 mA			1.2	
		I_O = 800 mA			1.3	
	Thermal regulation	T_a = 25°C, 30ms Pulse		0.01	0.1	%/W

Table 16. Electrical characteristics of LD1117#50C
(refer to the test circuits, T_J = -40 to 125°C, C_O = 10 µF, unless otherwise specified).

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_{in} = 7 V, I_O = 10 mA, T_J = 25°C	4.9	5	5.1	V
V_O	Output voltage	I_O = 0 to 800 mA, V_{in} = 6.5 to 15 V	4.8		5.2	V
ΔV_O	Line regulation	V_{in} = 6.5 to 15 V, I_O = 0 mA		1	50	mV
ΔV_O	Load regulation	V_{in} = 6.5 V, I_O = 0 to 800 mA		1	50	mV
ΔV_O	Temperature stability			0.5		%
ΔV_O	Long term stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating input voltage	I_O = 100 mA			15	V
I_d	Quiescent current	V_{in} ≤15 V		5	10	mA
I_O	Output current	V_{in} = 10 V, T_J = 25°C	800	950	1300	mA
eN	Output noise voltage	B =10Hz to 10KHz, T_J = 25°C		100		µV
SVR	Supply voltage rejection	I_O = 40 mA, f = 120Hz, T_J = 25°C V_{in} = 8 V, V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout voltage	I_O = 100 mA, T_J = 0 to 125°C		1	1.1	V
		I_O = 500 mA, T_J = 0 to 125°C		1.05	1.15	
		I_O = 800 mA, T_J = 0 to 125°C		1.10	1.2	
V_d	Dropout voltage	I_O = 100 mA			1.1	V
		I_O = 500 mA			1.2	
		I_O = 800 mA			1.3	
	Thermal regulation	T_a = 25°C, 30ms Pulse		0.01	0.1	%/W

Table 17. Electrical characteristics of LD1117C (Adjustable)
(refer to the test circuits, T_J = -40 to 125°C, C_O = 10 µF, unless otherwise specified).

Symbol	Parameter	Test	Min.	Typ.	Max.	Unit
V_{ref}	Reference voltage	V_{in} - V_O = 2 V, I_O = 10 mA, T_J = 25°C	1.225	1.25	1.275	V
V_{ref}	Reference voltage	I_O = 10 to 800 mA, V_{in} - V_O= 1.4 to 10 V	1.2		1.3	V
ΔV_O	Line regulation	V_{in} - V_O = 1.5 to 13.75 V, I_O = 10 mA			1	%
ΔV_O	Load regulation	V_{in} - V_O = 3 V, I_O = 10 to 800 mA			1	%
ΔV_O	Temperature stability			0.5		%
ΔV_O	Long term stability	1000 hrs, T_J = 125°C		0.3		%
V_{in}	Operating input voltage				15	V
I_{adj}	Adjustment pin current	V_{in} ≤15 V		60	120	µA
ΔI_{adj}	Adjustment pin current change	V_{in} - V_O = 1.4 to 10 V, I_O = 10 to 800 mA		1	10	µA
$I_{O(min)}$	Minimum load current	V_{in} = 15 V		2	5	mA
I_O	Output current	V_{in} - V_O = 5 V, T_J = 25°C	800	950	1300	mA
eN	Output noise (%V_O)	B =10Hz to 10KHz, T_J = 25°C		0.003		%
SVR	Supply voltage rejection	I_O = 40 mA, f = 120Hz, T_J = 25°C V_{in} - V_O = 3 V, V_{ripple} = 1 V_{PP}	60	75		dB
V_d	Dropout voltage	I_O = 100 mA, T_J = 0 to 125°C		1	1.1	V
		I_O = 500 mA, T_J = 0 to 125°C		1.05	1.15	
		I_O = 800 mA, T_J = 0 to 125°C		1.10	1.2	
V_d	Dropout voltage	I_O = 100 mA			1.1	V
		I_O = 500 mA			1.2	
		I_O = 800 mA			1.3	
	Thermal regulation	T_a = 25°C, 30ms Pulse		0.01	0.1	%/W

5 Typical application

Figure 4. Negative supply

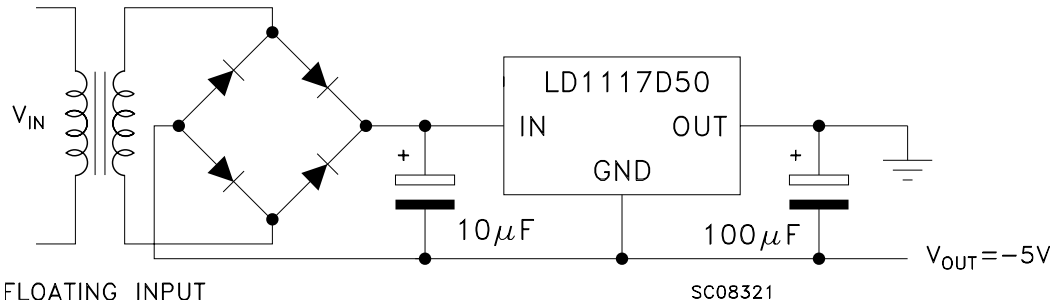


Figure 5. Active terminator for SCSI-2 BUS

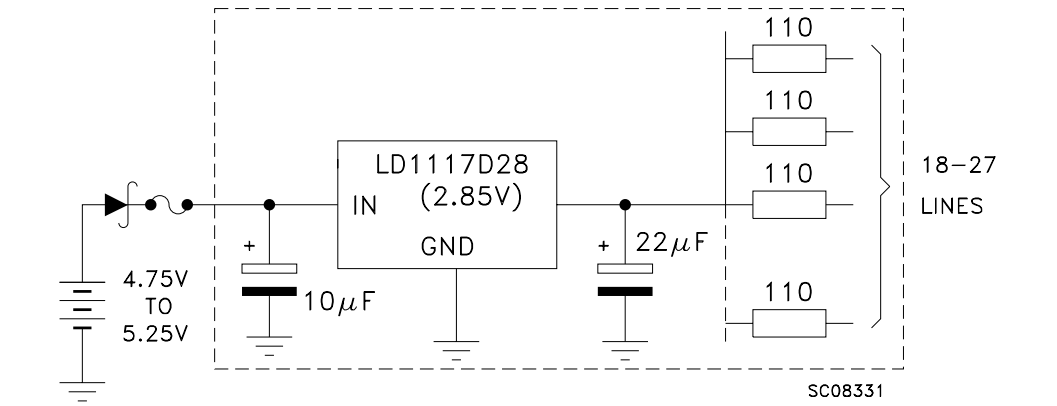


Figure 6. Circuit for increasing output voltage

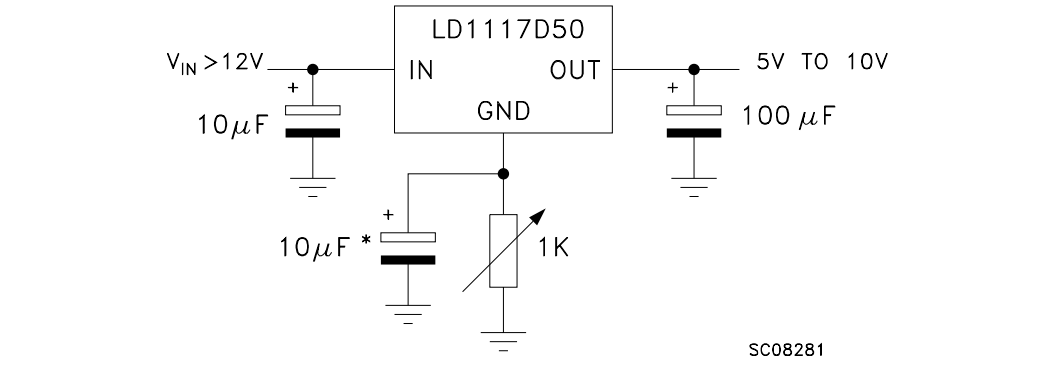


Figure 7. Voltage Regulator With Reference

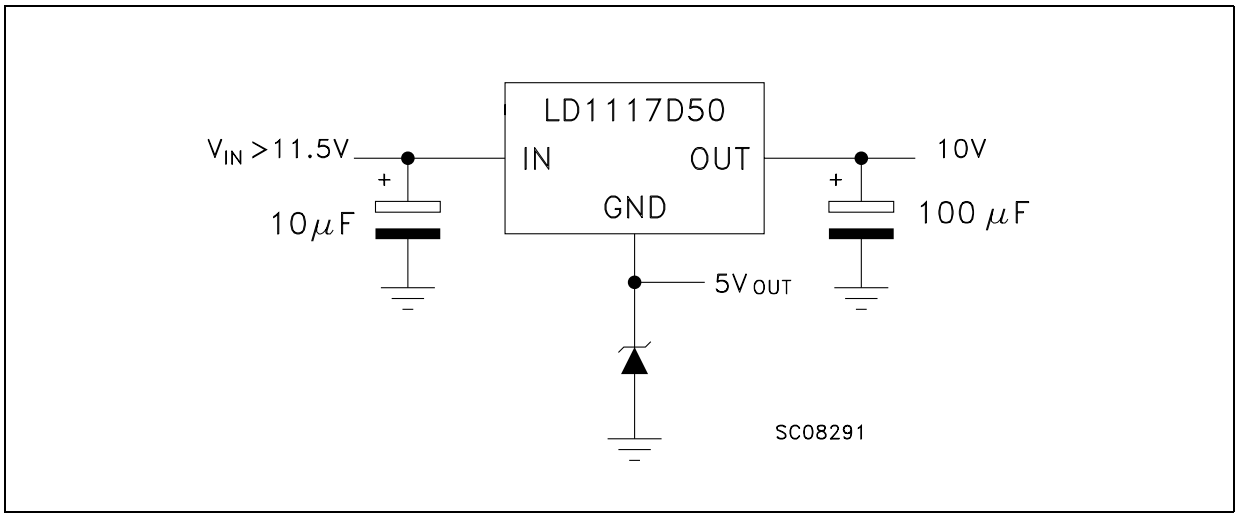


Figure 8. Battery backed-up regulated supply

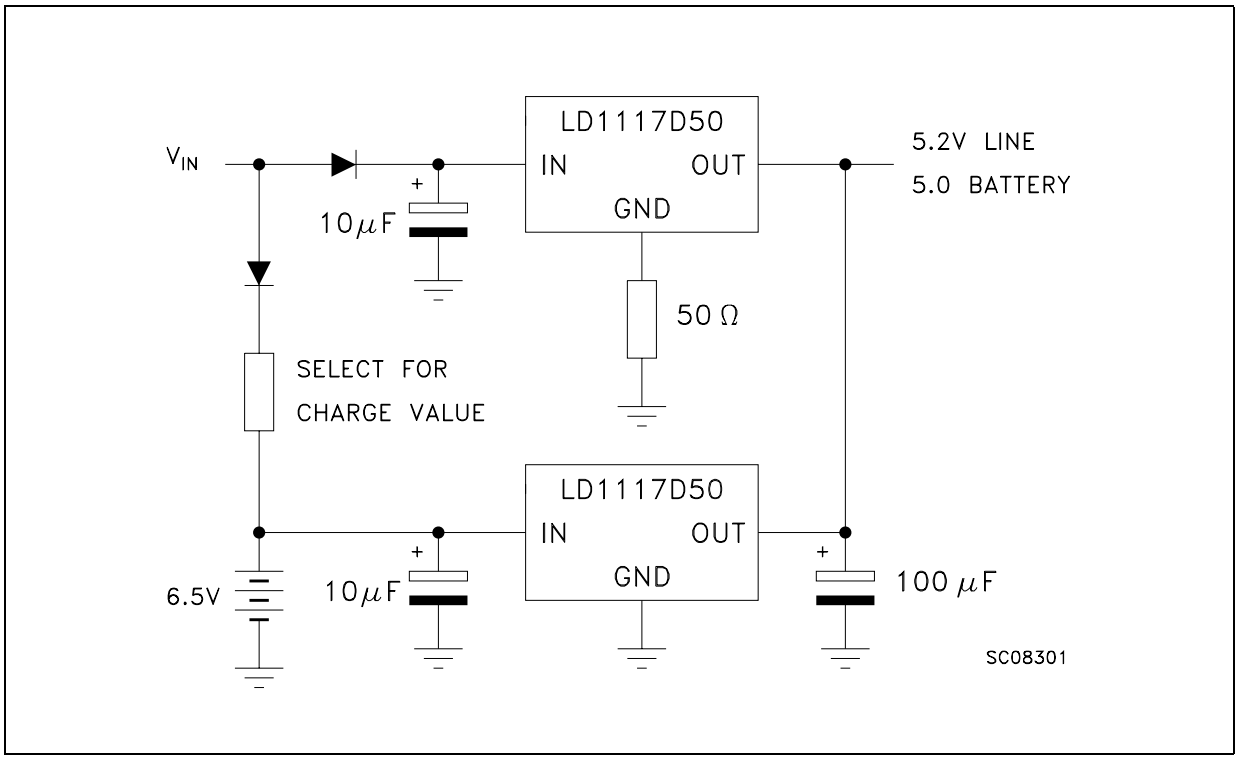
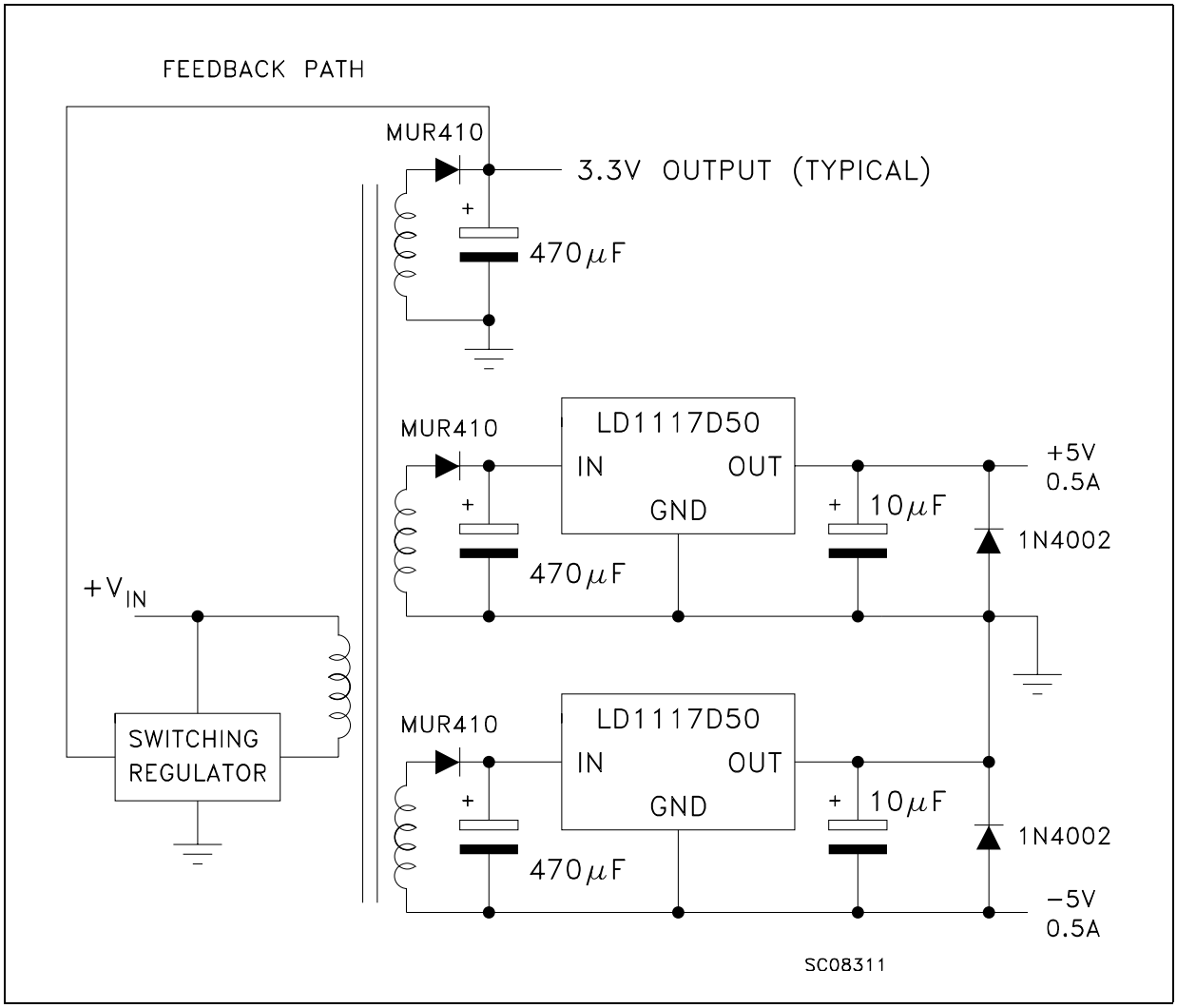


Figure 9. Post-regulated dual supply



6 LD1117 Adjustable: Application note

The LD1117 Adjustable has a thermal stabilized 1.25±0.012V reference voltage between the OUT and ADJ pins. I_{ADJ} is 60µA typ. (120µA max.) and ΔI_{ADJ} is 1µA typ. (5µA max.).

R1 is normally fixed to 120W. From figure 10 we obtain:

$V_{OUT} = V_{REF} + R2\ (I_{ADJ} + I_{R1}) = V_{REF} + R2\ (I_{ADJ} + V_{REF}/R_1) = V_{REF}\ (1 + R2 / R_1) + R2 \times I_{ADJ}$.

In normal application R2 value is in the range of few kohm, so the R2 x I_{ADJ} product could not be considered in the V_{OUT} calculation; then the above expression becomes:

$V_{OUT} = V_{REF}\ (1 + R2 / R1)$.

In order to have the better load regulation it is important to realize a good Kelvin connection of R1 and R2 resistors. In particular R1 connection must be realized very close to OUT and ADJ pin, while R2 ground connection must be placed as near as possible to the negative Load pin. Ripple rejection can be improved by introducing a 10µF electrolytic capacitor placed in parallel to the R2 resistor (see Fig. 11).

Figure 10. Adjustable output voltage application

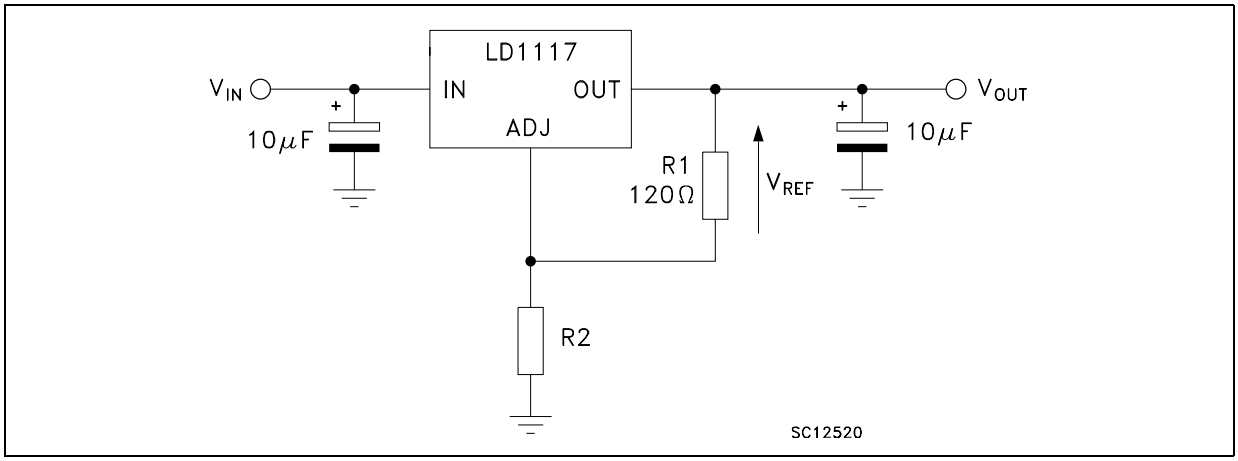
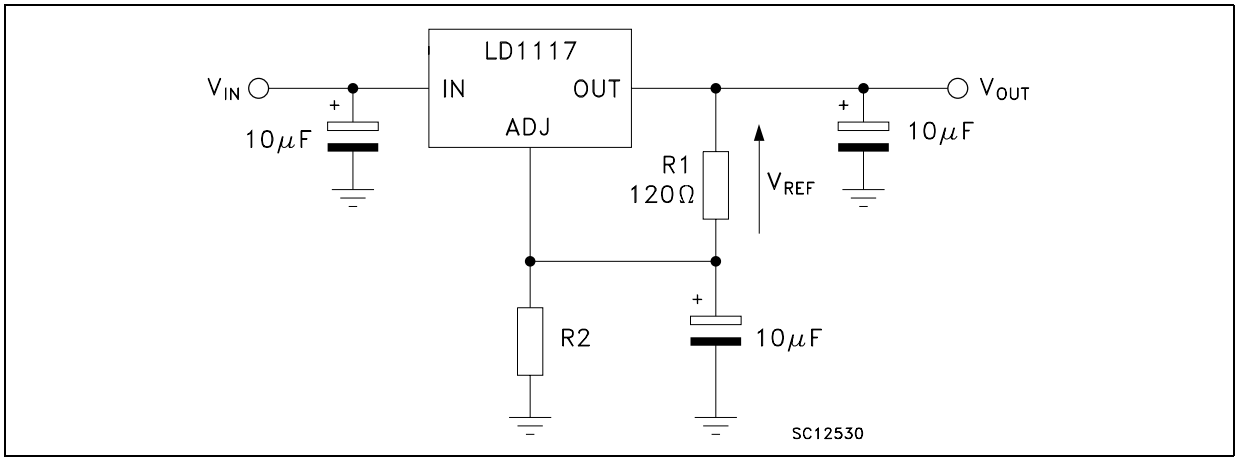


Figure 11. Adjustable output voltage application with improved ripple rejection

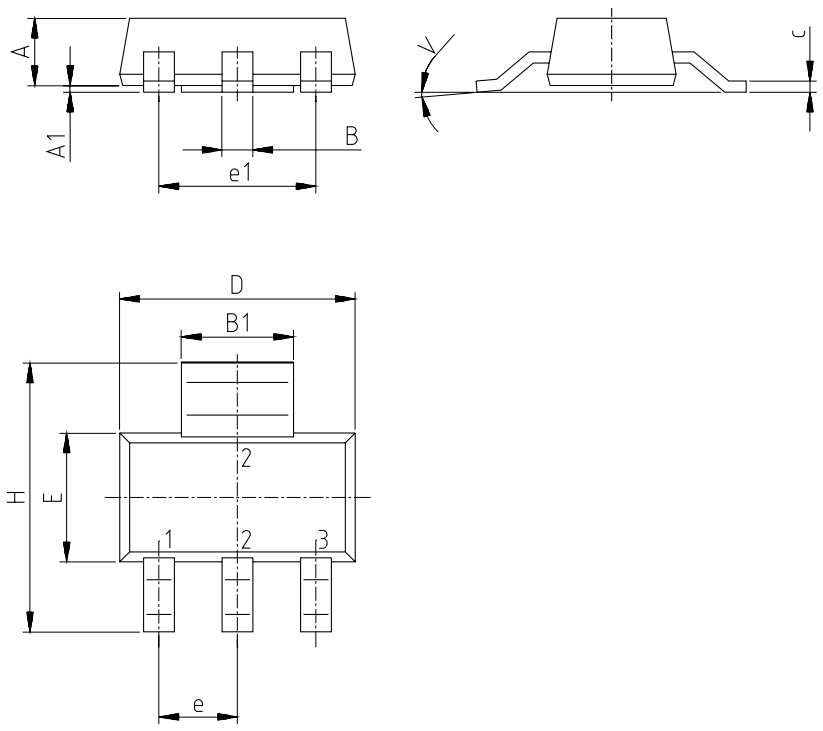


7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

SOT-223 MECHANICAL DATA

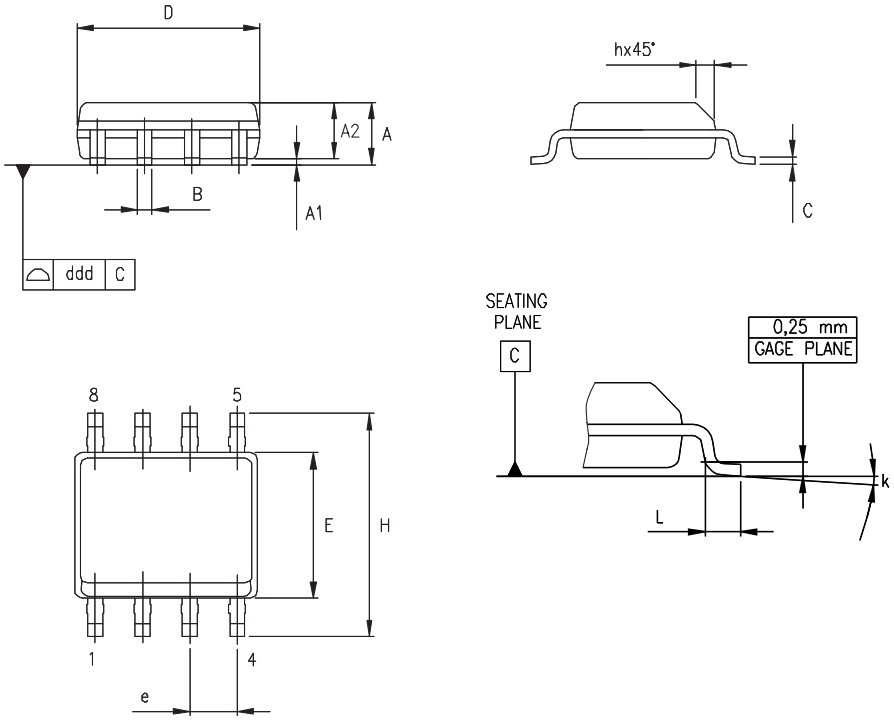
DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.8			70.9
A1	0.02		0.1	0.8		3.9
B	0.6	0.7	0.85	23.6	27.6	33.5
B1	2.9	3	3.15	114.2	118.1	124.0
c	0.24	0.26	0.35	9.4	10.2	13.8
D	6.3	6.5	6.7	248.0	255.9	263.8
e		2.3			90.6	
e1		4.6			181.1	
E	3.3	3.5	3.7	129.9	137.8	145.7
H	6.7	7	7.3	263.8	275.7	287.5
V			10°			10°



0046067/H

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



0016023/C

Figure 12. DRAWING DIMENSION DPAK (TYPE STD-ST)

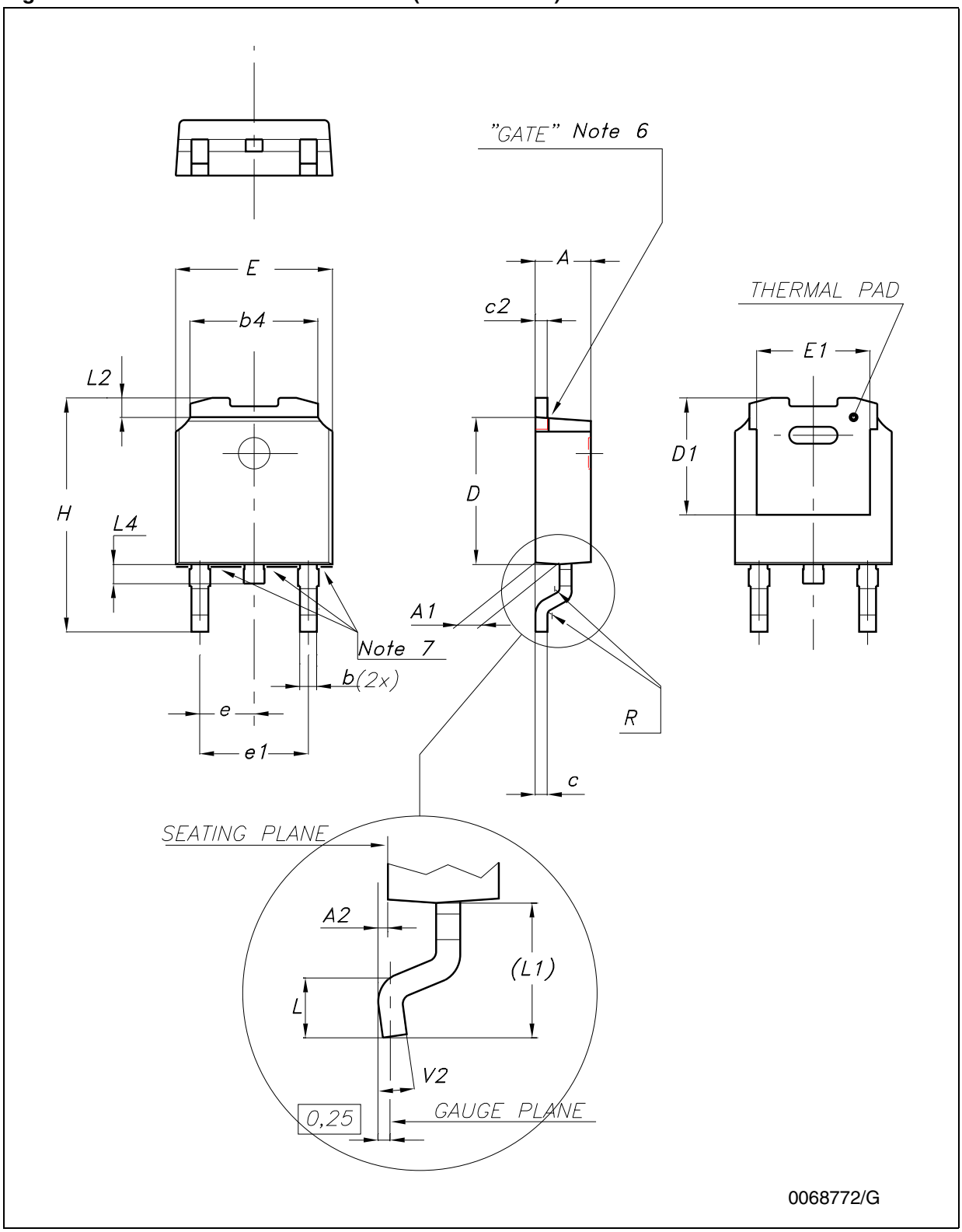


Figure 13. DRAWING DIMENSION DPAK (TYPE FUJITSU-SUBCON.)

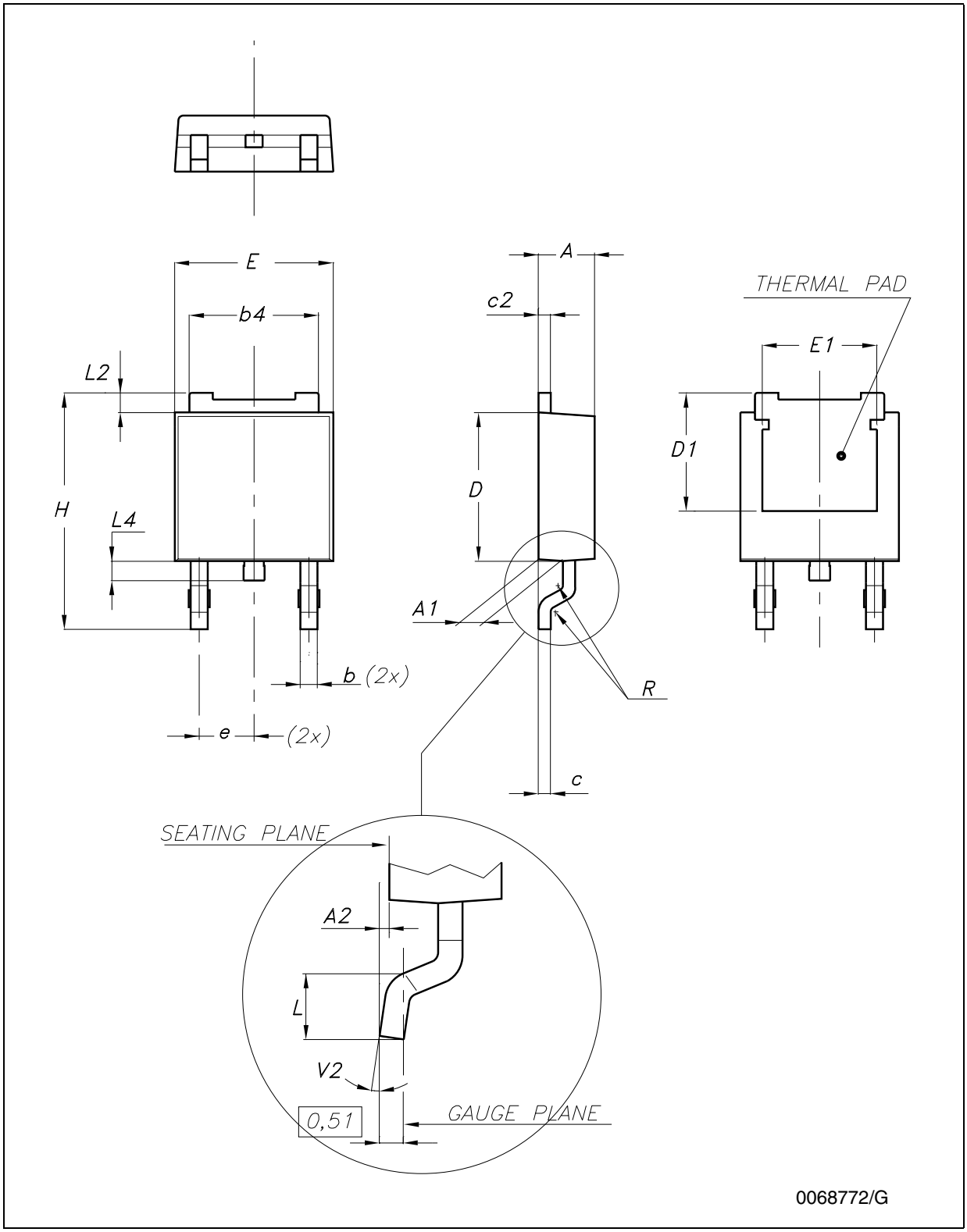


Figure 14. DRAWING DIMENSION DPAK (TYPE IDS-SUBCON.)

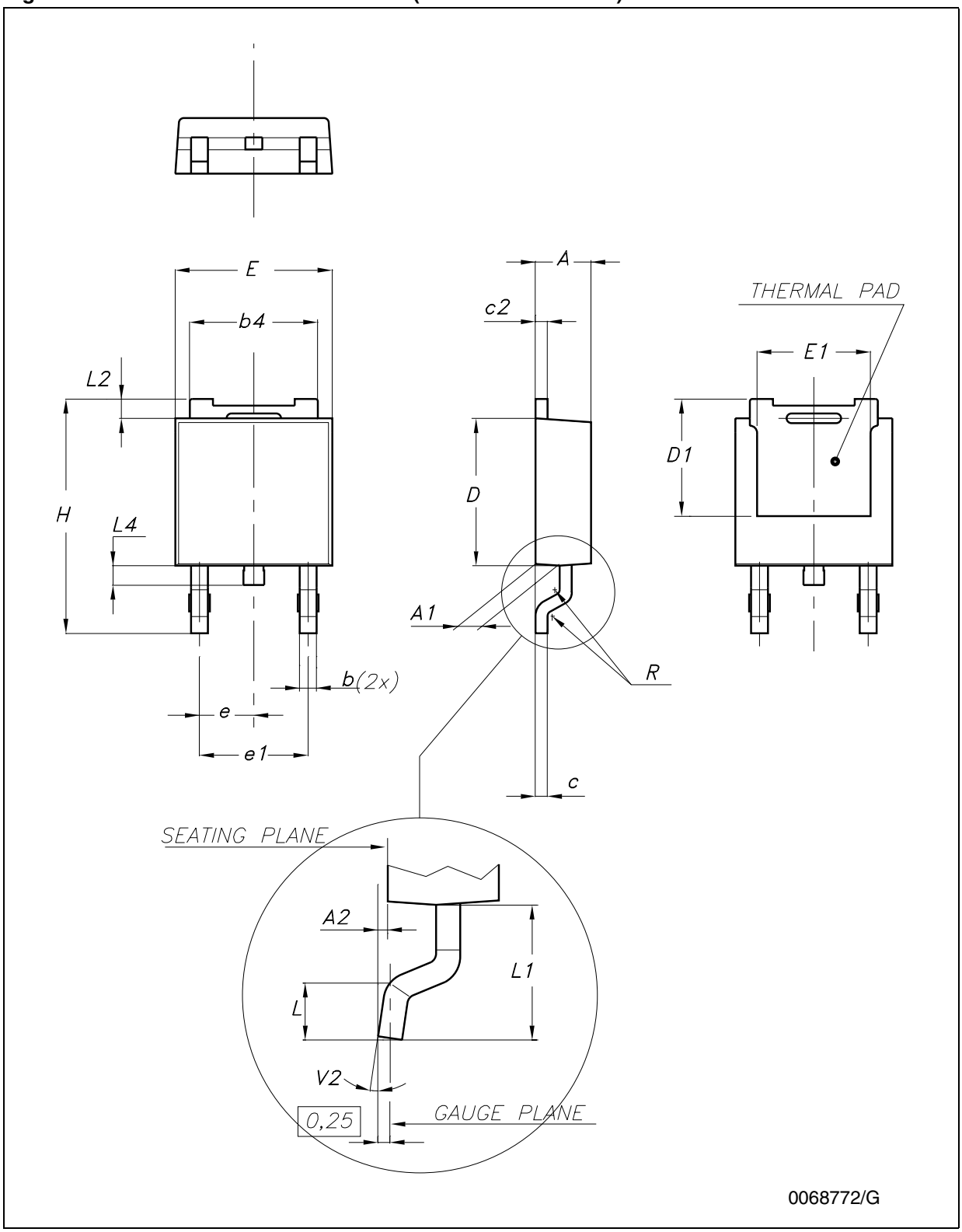


Table 18. DPAK MECHANICAL DATA

DIM.	TYPE STD-ST			TYPE FUJITSU-SUBCON.			TYPE IDS-SUBCON		
	mm.			mm.			mm.		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	2.25	2.30	2.35	2.19		2.38
A1	0.90		1.10	0.96		1.06	0.89		1.14
A2	0.03		0.23	0		0.10	0.03		0.23
b	0.64		0.90	0.76		0.86	0.64		0.88
b4	5.20		5.40	5.28		5.38	5.21		5.46
c	0.45		0.60	0.46		0.56	0.46		0.58
c2	0.48		0.60	0.46		0.56	0.46		0.58
D	6.00		6.20	6.05		6.15	5.97		6.22
D1		5.10		5.27		5.47		5.20	
E	6.40		6.60	6.55	6.60	6.65	6.35		6.73
E1		4.70			4.77			4.70	
e		2.28		2.23	2.28	2.33		2.28	
e1	4.40		4.60				4.51		4.61
H	9.35		10.10	9.90		10.30	9.40		10.42
L	1.00			1.40		1.60	0.90		
L1		2.80					2.50		2.65
L2		0.80		1.03		1.13	0.89		1.27
L4	0.60		1.00	0.70		0.90	0.64		1.02
R		0.20			0.40			0.20	
V2	0°		8°	0°		8°	0°		8°

Note: The DPAK package coming from the two subcontractors (Fujitsu and IDS) are fully compatible with the ST's package suggested footprint.

Figure 15. DPAK FOOTPRINT RECOMMENDED DATA

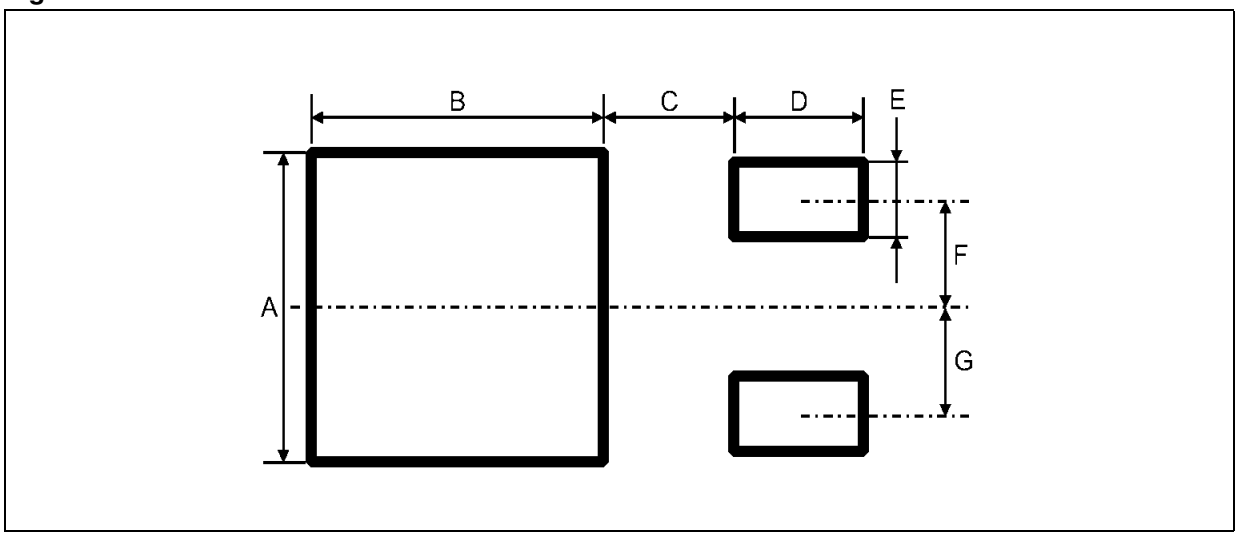
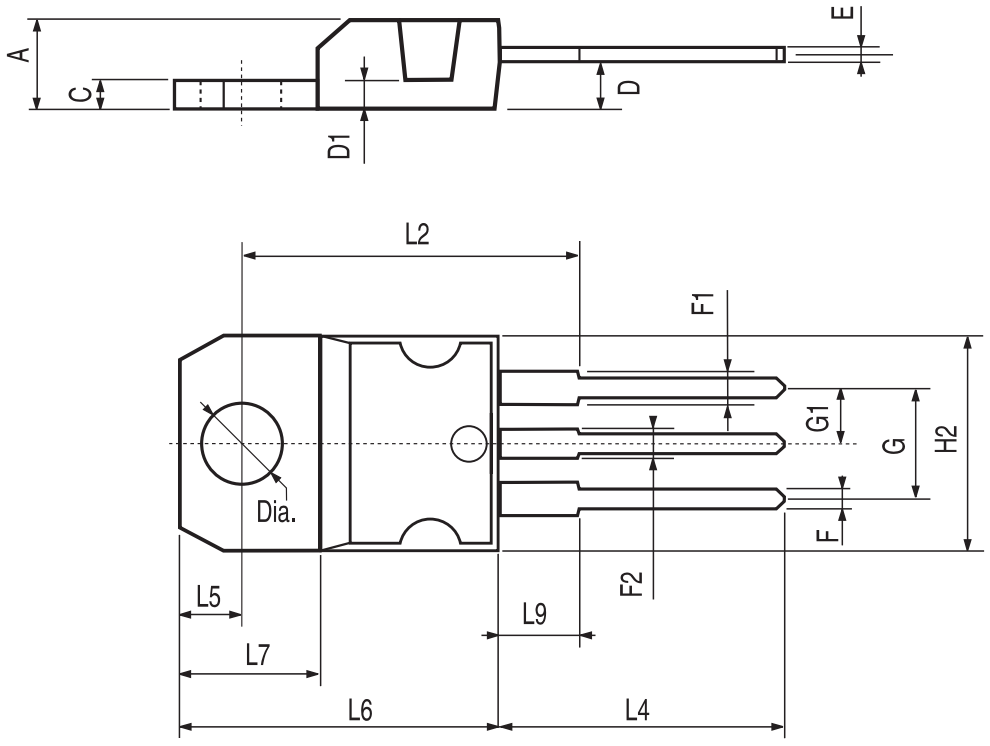


Table 19. FOOTPRINT DATA

VALUES		
	mm.	**inch.**
A	6.70	0.264
B	6.70	0.64
C	1.8	0.070
D	3.0	0.118
E	1.60	0.063
F	2.30	0.091
G	2.30	0.091

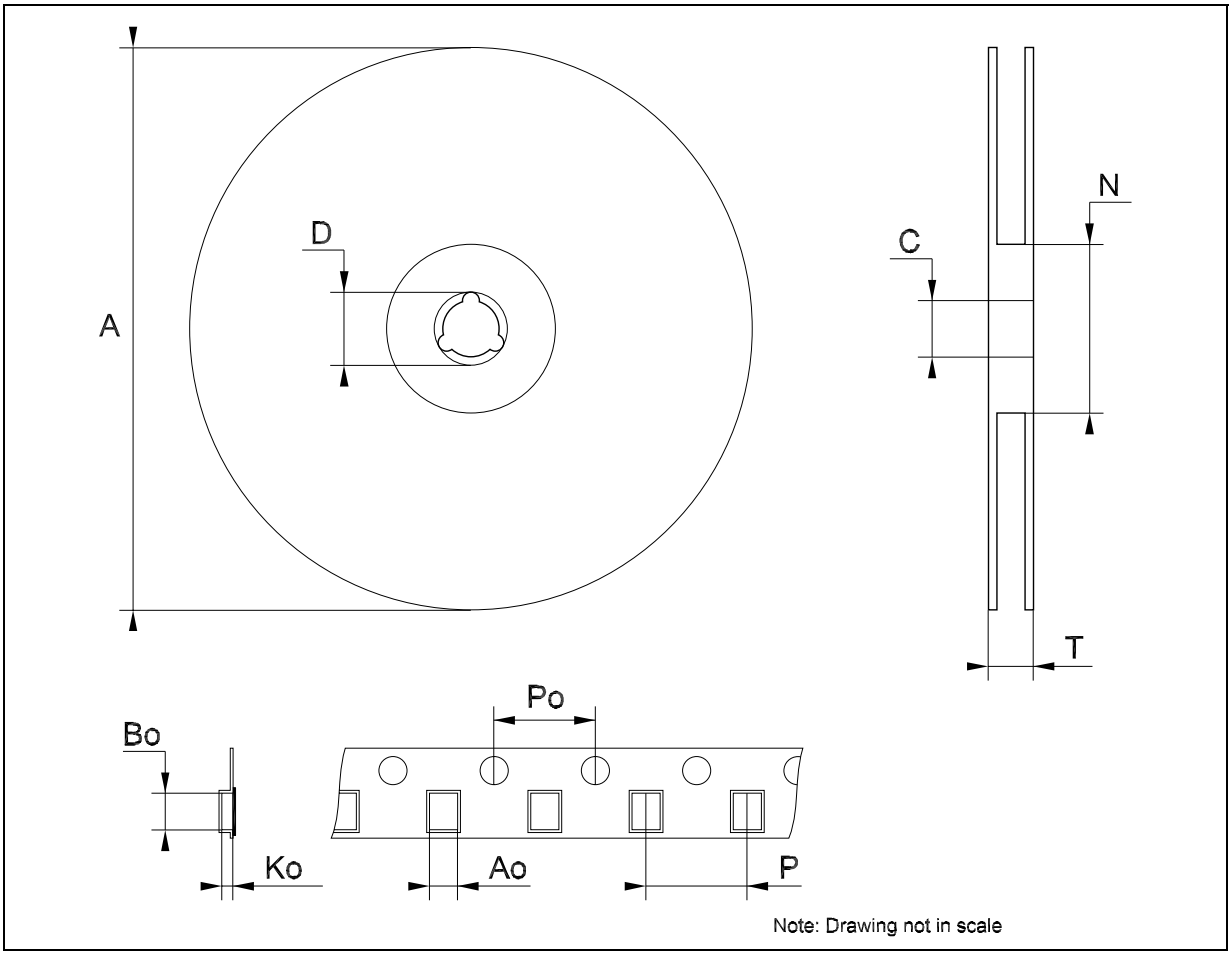
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



Tape & Reel SOT223 MECHANICAL DATA

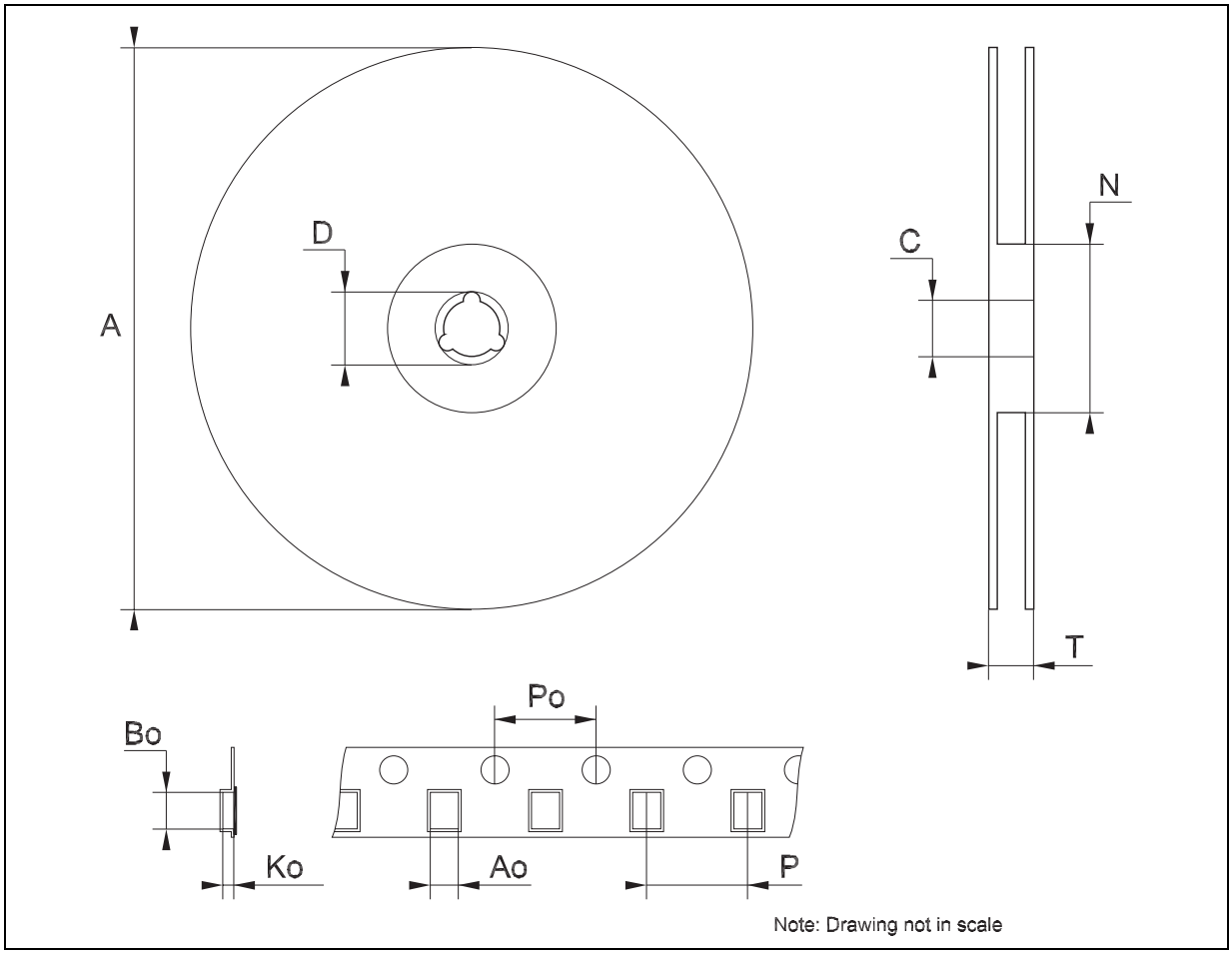
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	6.73	6.83	6.93	0.265	0.269	0.273
Bo	7.32	7.42	7.52	0.288	0.292	0.296
Ko	1.78		2	0.070		0.078
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	7.9	8.0	8.1	0.311	0.315	0.319



Note: Drawing not in scale

Tape & Reel SO-8 MECHANICAL DATA

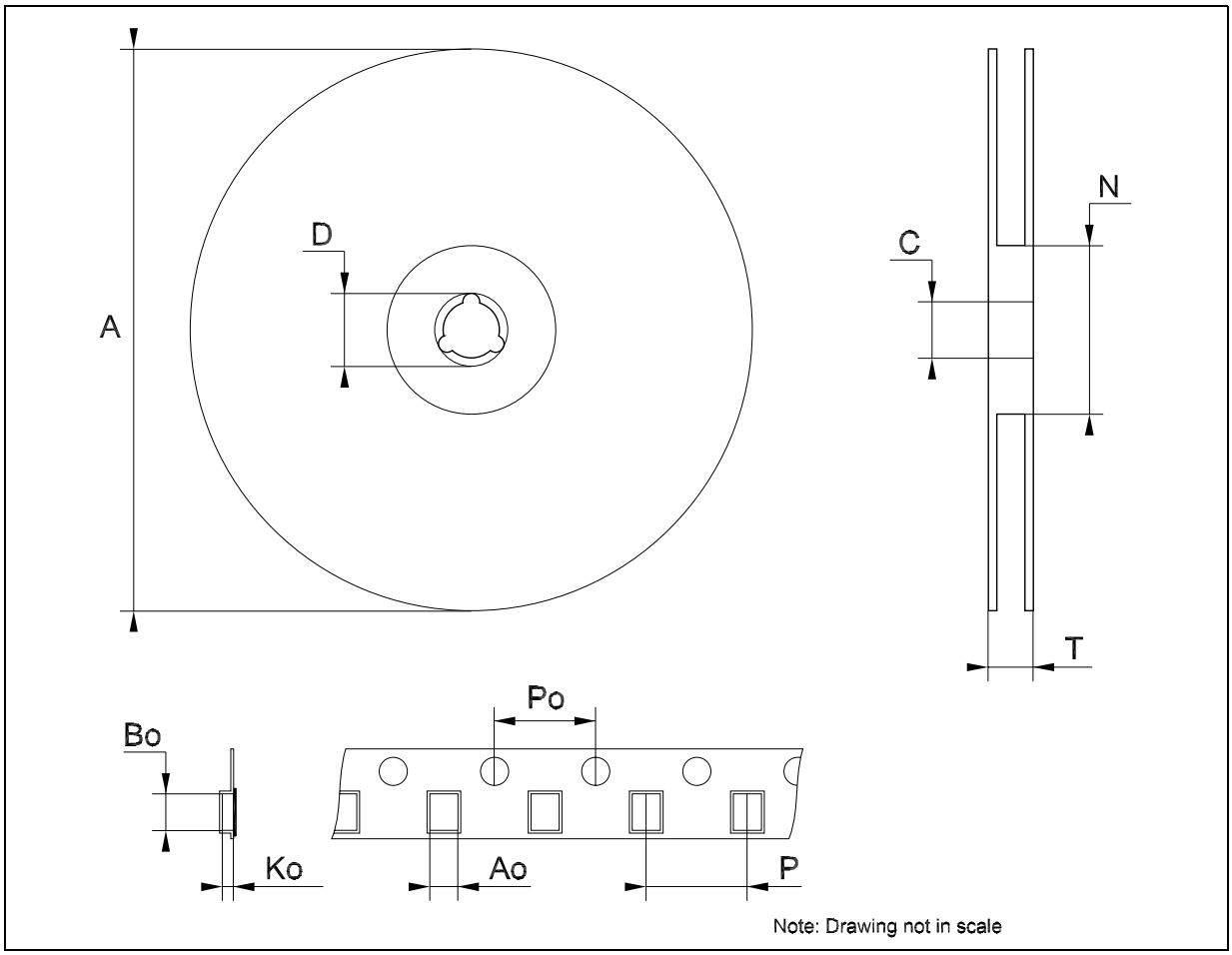
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	8.1		8.5	0.319		0.335
Bo	5.5		5.9	0.216		0.232
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale

Tape & Reel DPAK-PPAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.80	6.90	7.00	0.268	0.272	0.2.76
Bo	10.40	10.50	10.60	0.409	0.413	0.417
Ko	2.55	2.65	2.75	0.100	0.104	0.105
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	7.9	8.0	8.1	0.311	0.315	0.319



Note: Drawing not in scale

8 Order code

Table 20. Order code

Part numbers					
SOT-223	**SO-8**	**DPAK**	**DPAK (T&R)**	**TO-220**	**Output voltage**
LD1117S12TR	LD1117D12TR (*)	LD1117DT12 (*)	LD1117DT12TR	LD1117V12 (*)	1.2 V
LD1117S12CTR (*)	LD1117D12CTR (*)	LD1117DT12C (*)		LD1117V12C (*)	1.2 V
LD1117S18TR	LD1117D18TR (*)	LD1117DT18	LD1117DT18TR	LD1117V18	1.8 V
LD1117S18CTR (*)	LD1117D18CTR (*)	LD1117DT18C	LD1117DT18CTR	LD1117V18C (*)	1.8 V
LD1117S25TR	LD1117D25TR (*)	LD1117DT25	LD1117DT25TR	LD1117V25	2.5 V
LD1117S25CTR	LD1117D25CTR (*)	LD1117DT25C	LD1117DT25CTR	LD1117V25C	2.5 V
LD1117S28TR	LD1117D28TR (*)		LD1117DT28TR		2.85 V
LD1117S30TR	LD1117D30TR (*)				3 V
LD1117S33TR	LD1117D33TR	LD1117DT33	LD1117DT33TR	LD1117V33	3.3 V
LD1117S33CTR	LD1117D33CTR	LD1117DT33C	LD1117DT33CTR	LD1117V33C	3.3 V
LD1117S50TR	LD1117D50TR	LD1117DT50	LD1117DT50TR	LD1117V50	5 V
LD1117S50CTR	LD1117D50CTR (*)	LD1117DT50C	LD1117DT50CTR		5 V
LD1117STR	LD1117DTR (*)	LD1117DT	LD1117DTTR	LD1117V	ADJ FROM 1.25 TO 15V
LD1117SC-R	LD1117DC-R (*)	LD1117DTC (*)	LD1117DTC-R	LD1117VC (*)	ADJ FROM 1.25 TO 15V

(*) Available on request.

9 Revision history

Table 21. Document revision history

Date	Revision	Changes
22-Sep-2004	15	Add new Part Number #12C; Typing Error: Note on table 2.
25-Oct-2004	16	Add V_{ref} Reference Voltage on Table 12.
18-Jul-2005	17	The DPAK Mechanical Data has been updated.
25-Nov-2005	18	The TO220FM Package has been removed.
14-Dec-2005	19	The T_{op} on Table 2 has been updated.
06-Dec-2006	20	DPAK mechanical data has been updated and add footprint data.

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2.2.4. Controlador

ESP-WROOM-32 Datasheet

Espressif Systems

October 26, 2017

About This Guide

This document provides the specifications for the ESP-WROOM-32 module.

Release Notes

Date	Version	Release notes
2016.08	V1.0	First release.
2016.11	V1.1	Updated Chapter 6 Schematics.
2016.11	V1.2	Added Figure 7 Peripheral Schematics.
2016.12	V1.3	Updated Section 2.1 Pin Layout.
2017.03	V1.4	Updated Chapter 1 Preface; Updated Chapter 2 Pin Definitions; Updated Chapter 3 Functional Description; Updated Table Recommended Operating Conditions; Updated Table 9 Wi-Fi Radio Characteristics; Updated Section 5.4 Reflow Profile; Added Chapter 9 Learning Resources.
2017.03	V1.5	Updated Section 2.2 Pin Description; Updated Section 3.2 External Flash and SRAM; Updated Section 4.1 Peripherals and Sensors Description.
2017.04	V1.6	Added Figure 2 Reflow Profile.
2017.04	V1.7	Added the module's dimensional tolerance; Changed the input impedance value of 50Ω in Table 9 Wi-Fi Radio Characteristics to output impedance value of 30+j10 Ω.
2017.05	V1.8	Updated Figure 1 Top and Side View of ESP-WROOM-32.
2017.06	V1.9	Added a note to Section 2.1 Pin Layout; Updated Section 3.3 Crystal Oscillators; Updated Figure 3 ESP-WROOM-32 Schematics; Added Documentation Change Notification.
2017.08	V2.0	Changed the sensitivity of NZIF receiver to -97 dBm in Table 2; Updated the dimensions of the module; Updated Table 6 Power Consumption by Power Modes, and added two notes to it; Updated Table 8, 9, 10, 11; Added Chapter 8; Added the link to certification download.
2017.09	V2.1	Updated operating voltage/power supply range updated to 2.7 ~ 3.6V; Updated Chapter 7.
2017.10	V2.2	Updated the description of the chip's system reset in Section 2.3 Strapping Pins; Deleted "Association sleep pattern" in Table 6 and added notes to Active sleep and Modem-sleep; Updated the note to Figure 4 Peripheral Schematics; Added discharge circuit for VDD33 rail in Chapter 7 and a note to it.

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1. Overview

ESP-WROOM-32 is a powerful, generic Wi-Fi+BT+BLE MCU module that targets a wide variety of applications, ranging from low-power sensor networks to the most demanding tasks, such as voice encoding, music streaming and MP3 decoding.

At the core of this module is the ESP32-D0WDQ6 chip*. The chip embedded is designed to be scalable and adaptive. There are two CPU cores that can be individually controlled, and the clock frequency is adjustable from 80 MHz to 240 MHz. The user may also power off the CPU and make use of the low-power co-processor to constantly monitor the peripherals for changes or crossing of thresholds. ESP32 integrates a rich set of peripherals, ranging from capacitive touch sensors, Hall sensors, low-noise sense amplifiers, SD card interface, Ethernet, high-speed SPI, UART, I2S and I2C.

Note:

* For details on the part number of the ESP32 series, please refer to the document ESP32 Datasheet.

The integration of Bluetooth, Bluetooth LE and Wi-Fi ensures that a wide range of applications can be targeted, and that the module is future proof: using Wi-Fi allows a large physical range and direct connection to the internet through a Wi-Fi router, while using Bluetooth allows the user to conveniently connect to the phone or broadcast low energy beacons for its detection. The sleep current of the ESP32 chip is less than 5 μA, making it suitable for battery powered and wearable electronics applications. ESP32 supports a data rate of up to 150 Mbps, and 20.5 dBm output power at the antenna to ensure the widest physical range. As such the chip does offer industry-leading specifications and the best performance for electronic integration, range, power consumption, and connectivity.

The operating system chosen for ESP32 is freeRTOS with LwIP; TLS 1.2 with hardware acceleration is built in as well. Secure (encrypted) over the air (OTA) upgrade is also supported, so that developers can continually upgrade their products even after their release.

Table 2 provides the specifications of ESP-WROOM-32.

Table 2: ESP-WROOM-32 Specifications

Categories	Items	Specifications
Wi-Fi	RF certification	FCC/CE/IC/TELEC/KCC/SRRC/NCC
	Protocols	802.11 b/g/n/e/i (802.11n up to 150 Mbps)
		A-MPDU and A-MSDU aggregation and 0.4 μs guard interval support
	Frequency range	2.4 ~ 2.5 GHz
Bluetooth	Protocols	Bluetooth v4.2 BR/EDR and BLE specification
	Radio	NZIF receiver with -97 dBm sensitivity
		Class-1, class-2 and class-3 transmitter
		AFH
	Audio	CVSD and SBC

Categories	Items	Specifications
Hardware	Module interface	SD card, UART, SPI, SDIO, I2C, LED PWM, Motor PWM, I2S, IR
		GPIO, capacitive touch sensor, ADC, DAC, LNA pre-amplifier
	On-chip sensor	Hall sensor, temperature sensor
	On-board clock	40 MHz crystal
	Operating voltage/Power supply	2.7 ~ 3.6V
	Operating current	Average: 80 mA
	Minimum current delivered by power supply	500 mA
	Operating temperature range	-40°C ~ +85°C
	Ambient temperature range	Normal temperature
	Package size	18±0.2 mm x 25.5±0.2 mm x 3.1±0.15 mm
Software	Wi-Fi mode	Station/SoftAP/SoftAP+Station/P2P
	Wi-Fi Security	WPA/WPA2/WPA2-Enterprise/WPS
	Encryption	AES/RSA/ECC/SHA
	Firmware upgrade	UART Download / OTA (download and write firmware via network or host)
	Software development	Supports Cloud Server Development / SDK for custom firmware development
	Network protocols	IPv4, IPv6, SSL, TCP/UDP/HTTP/FTP/MQTT
	User configuration	AT instruction set, cloud server, Android/iOS app

2. Pin Definitions

2.1 Pin Layout

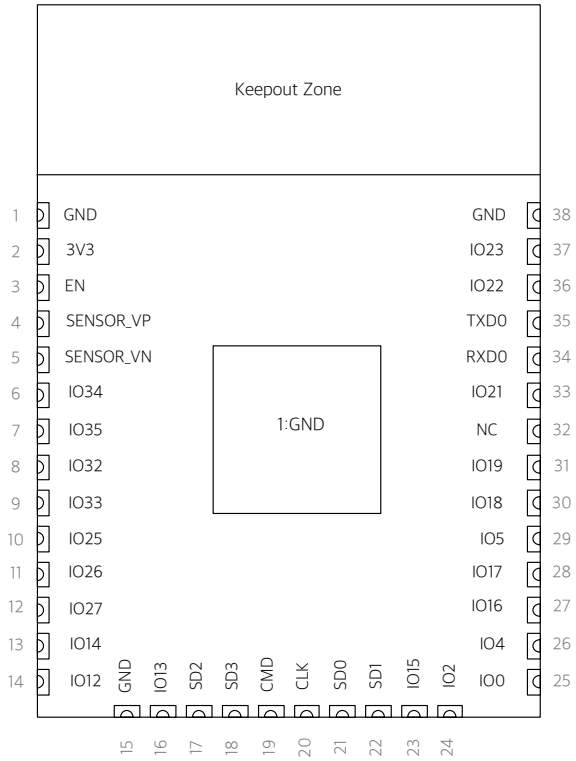


Figure 1: ESP-WROOM-32 Pin layout

2.2 Pin Description

ESP-WROOM-32 has 38 pins. See pin definitions in Table 3.

Table 3: Pin Definitions

Name	No.	Type	Function
GND	1	P	Ground
3V3	2	P	Power supply.
EN	3	I	Chip-enable signal. Active high.
SENSOR_VP	4	I	GPIO36, SENSOR_VP, ADC_H, ADC1_CH0, RTC_GPIO0
SENSOR_VN	5	I	GPIO39, SENSOR_VN, ADC1_CH3, ADC_H, RTC_GPIO3
IO34	6	I	GPIO34, ADC1_CH6, RTC_GPIO4
IO35	7	I	GPIO35, ADC1_CH7, RTC_GPIO5
IO32	8	I/O	GPIO32, XTAL_32K_P (32.768 kHz crystal oscillator input), ADC1_CH4, TOUCH9, RTC_GPIO9
IO33	9	I/O	GPIO33, XTAL_32K_N (32.768 kHz crystal oscillator output), ADC1_CH5, TOUCH8, RTC_GPIO8
IO25	10	I/O	GPIO25, DAC_1, ADC2_CH8, RTC_GPIO6, EMAC_RXD0
IO26	11	I/O	GPIO26, DAC_2, ADC2_CH9, RTC_GPIO7, EMAC_RXD1
IO27	12	I/O	GPIO27, ADC2_CH7, TOUCH7, RTC_GPIO17, EMAC_RX_DV

Name	No.	Type	Function
IO14	13	I/O	GPIO14, ADC2_CH6, TOUCH6, RTC_GPIO16, MTMS, HSPICLK, HS2_CLK, SD_CLK, EMAC_TXD2
IO12	14	I/O	GPIO12, ADC2_CH5, TOUCH5, RTC_GPIO15, MTDI, HSPIQ, HS2_DATA2, SD_DATA2, EMAC_TXD3
GND	15	P	Ground
IO13	16	I/O	GPIO13, ADC2_CH4, TOUCH4, RTC_GPIO14, MTCK, HSPID, HS2_DATA3, SD_DATA3, EMAC_RX_ER
SHD/SD2*	17	I/O	GPIO9, SD_DATA2, SPIHD, HS1_DATA2, U1RXD
SWP/SD3*	18	I/O	GPIO10, SD_DATA3, SPIWP, HS1_DATA3, U1TXD
SCS/CMD*	19	I/O	GPIO11, SD_CMD, SPICS0, HS1_CMD, U1RTS
SCK/CLK*	20	I/O	GPIO6, SD_CLK, SPICLK, HS1_CLK, U1CTS
SDO/SD0*	21	I/O	GPIO7, SD_DATA0, SPIQ, HS1_DATA0, U2RTS
SDI/SD1*	22	I/O	GPIO8, SD_DATA1, SPID, HS1_DATA1, U2CTS
IO15	23	I/O	GPIO15, ADC2_CH3, TOUCH3, MTDO, HSPICS0, RTC_GPIO13, HS2_CMD, SD_CMD, EMAC_RXD3
IO2	24	I/O	GPIO2, ADC2_CH2, TOUCH2, RTC_GPIO12, HSPIWP, HS2_DATA0, SD_DATA0
IO0	25	I/O	GPIO0, ADC2_CH1, TOUCH1, RTC_GPIO11, CLK_OUT1, EMAC_TX_CLK
IO4	26	I/O	GPIO4, ADC2_CH0, TOUCH0, RTC_GPIO10, HSPIHD, HS2_DATA1, SD_DATA1, EMAC_TX_ER
IO16	27	I/O	GPIO16, HS1_DATA4, U2RXD, EMAC_CLK_OUT
IO17	28	I/O	GPIO17, HS1_DATA5, U2TXD, EMAC_CLK_OUT_180
IO5	29	I/O	GPIO5, VSPICS0, HS1_DATA6, EMAC_RX_CLK
IO18	30	I/O	GPIO18, VSPICLK, HS1_DATA7
IO19	31	I/O	GPIO19, VSPIQ, U0CTS, EMAC_TXD0
NC	32	-	-
IO21	33	I/O	GPIO21, VSPIHD, EMAC_TX_EN
RXD0	34	I/O	GPIO3, U0RXD, CLK_OUT2
TXD0	35	I/O	GPIO1, U0TXD, CLK_OUT3, EMAC_RXD2
IO22	36	I/O	GPIO22, VSPIWP, U0RTS, EMAC_TXD1
IO23	37	I/O	GPIO23, VSPID, HS1_STROBE
GND	38	P	Ground

Note:

* Pins SCK/CLK, SDO/SD0, SDI/SD1, SHD/SD2, SWP/SD3 and SCS/CMD, namely, GPIO6 to GPIO11 are connected to the integrated SPI flash integrated on ESP-WROOM-32 and are not recommended for other uses.

2.3 Strapping Pins

Please refer to ESP-WROOM-32 schematics.

ESP32 has five strapping pins, which can be seen in Section 6 Schematics:

- MTDI

- GPIO0
- GPIO2
- MTDO
- GPIO5

Software can read the value of these five bits from the register "GPIO_STRAPPING".

During the chip's system reset (power-on reset, RTC watchdog reset and brownout reset), the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down. The strapping bits configure the device boot mode, the operating voltage of VDD_SDIO and other system initial settings.

Each strapping pin is connected with its internal pull-up/pull-down during the chip reset. Consequently, if a strapping pin is unconnected or the connected external circuit is high-impendence, the internal weak pull-up/pull-down will determine the default input level of the strapping pins.

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or apply the host MCU's GPIOs to control the voltage level of these pins when powering on ESP32.

After reset, the strapping pins work as the normal functions pins.

Refer to Table 4 for detailed boot modes' configuration by strapping pins.

Table 4: Strapping Pins

Voltage of Internal LDO (VDD_SDIO)					
Pin	Default	3.3V		1.8V	
MTDI	Pull-down	0		1	
Booting Mode					
Pin	Default	SPI Boot		Download Boot	
GPIO0	Pull-up	1		0	
GPIO2	Pull-down	Don't-care		0	
Debugging Log on U0TXD During Booting					
Pin	Default	U0TXD Toggling		U0TXD Silent	
MTDO	Pull-up	1		0	
Timing of SDIO Slave					
Pin	Default	Falling-edge Input Falling-edge Output	Falling-edge Input Rising-edge Output	Rising-edge Input Falling-edge Output	Rising-edge Input Rising-edge Output
MTDO	Pull-up	0	0	1	1
GPIO5	Pull-up	0	1	0	1

Note:
Firmware can configure register bits to change the settings of "Voltage of Internal LDO (VDD_SDIO)" and "Timing of SDIO Slave" after booting.

3. Functional Description

This chapter describes the modules and functions integrated in ESP-WROOM-32.

3.1 CPU and Internal Memory

ESP32-D0WDQ6 contains two low-power Xtensa® 32-bit LX6 microprocessors. The internal memory includes:

- 448 kB of ROM for booting and core functions.
- 520 kB (8 kB RTC FAST Memory included) of on-chip SRAM for data and instruction.
  - 8 kB of SRAM in RTC, which is called RTC FAST Memory and can be used for data storage; it is accessed by the main CPU during RTC Boot from the Deep-sleep mode.
- 8 kB of SRAM in RTC, which is called RTC SLOW Memory and can be accessed by the co-processor during the Deep-sleep mode.
- 1 kbit of eFuse, of which 256 bits are used for the system (MAC address and chip configuration) and the remaining 768 bits are reserved for customer applications, including Flash-Encryption and Chip-ID.

3.2 External Flash and SRAM

ESP32 supports up to four 16-MB of external QSPI flash and SRAM with hardware encryption based on AES to protect developers' programs and data.

ESP32 can access the external QSPI flash and SRAM through high-speed caches.

- Up to 16 MB of external flash are memory-mapped onto the CPU code space, supporting 8, 16 and 32-bit access. Code execution is supported.
- Up to 8 MB of external flash/SRAM are memory-mapped onto the CPU data space, supporting 8, 16 and 32-bit access. Data-read is supported on the flash and SRAM. Data-write is supported on the SRAM.

ESP-WROOM-32 integrates 4 MB of external SPI flash. The 4-MB SPI flash can be memory-mapped onto the CPU code space, supporting 8, 16 and 32-bit access. Code execution is supported. The integrated SPI flash is connected to GPIO6, GPIO7, GPIO8, GPIO9, GPIO10 and GPIO11. These six pins cannot be used as regular GPIO.

3.3 Crystal Oscillators

The ESP32 Wi-Fi/BT firmware can only support 40 MHz crystal oscillator for now.

3.4 RTC and Low-Power Management

With the use of advanced power management technologies, ESP32 can switch between different power modes (see Table 5).

- Power modes
  - Active mode: The chip radio is powered on. The chip can receive, transmit, or listen.
  - Modem-sleep mode: The CPU is operational and the clock is configurable. The Wi-Fi/Bluetooth baseband and radio are disabled.
  - Light-sleep mode: The CPU is paused. The RTC memory and RTC peripherals, as well as the ULP co-processor are running. Any wake-up events (MAC, host, RTC timer, or external interrupts) will wake up the chip.
  - Deep-sleep mode: Only the RTC memory and RTC peripherals are powered on. Wi-Fi and Bluetooth connection data are stored in the RTC memory. The ULP co-processor can work.
  - Hibernation mode: The internal 8-MHz oscillator and ULP co-processor are disabled. The RTC recovery memory is powered down. Only one RTC timer on the slow clock and some RTC GPIOs are active. The RTC timer or the RTC GPIOs can wake up the chip from the Hibernation mode.
- Sleep Patterns
  - Association sleep pattern: The power mode switches between the Active mode, Modem- and Light-sleep mode during this sleep pattern. The CPU, Wi-Fi, Bluetooth, and radio are woken up at predetermined intervals to keep Wi-Fi/BT connections alive.
  - ULP sensor-monitored pattern: The main CPU is in the Deep-sleep mode. The ULP co-processor takes sensor measurements and wakes up the main system, based on the data collected from sensors.

Table 5: Functionalities Depending on the Power Modes

Power mode	Active	Modem-sleep	Light-sleep	Deep-sleep	Hibernation
Sleep pattern	Association sleep pattern			ULP sensor-monitored pattern	-
CPU	ON	ON	PAUSE	OFF	OFF
Wi-Fi/BT baseband and radio	ON	OFF	OFF	OFF	OFF
RTC memory and RTC peripherals	ON	ON	ON	ON	OFF
ULP co-processor	ON	ON	ON	ON/OFF	OFF

The power consumption varies with different power modes/sleep patterns and work statuses of functional modules. Please see Table 6 for details.

Table 6: Power Consumption by Power Modes

Power mode	Description	Power consumption
Active (RF working)	Wi-Fi Tx packet 14 dBm ~ 19.5 dBm	Please refer to ESP32 Datasheet.
	Wi-Fi / BT Tx packet 0 dBm	
	Wi-Fi / BT Rx and listening	
	Association sleep pattern (by Light-sleep)	1 mA ~ 4 mA @DTIM3

Power mode	Description	Power consumption
Modem-sleep	The CPU is powered on.	Max speed 240 MHz: 30 mA ~ 50 mA
		Normal speed 80 MHz: 20 mA ~ 25 mA
		Slow speed 2 MHz: 2 mA ~ 4 mA
Light-sleep	-	0.8 mA
Deep-sleep	The ULP co-processor is powered on.	150 μA
	ULP sensor-monitored pattern	100 μA @1% duty
	RTC timer + RTC memory	10 μA
Hibernation	RTC timer only	5 μA
Power off	CHIP_PU is set to low level, the chip is powered off	0.1 μA

Note:

- When Wi-Fi is enabled, the chip switches between Active and Modem-sleep mode. Therefore, power consumption changes accordingly.
- In Modem-sleep mode, the CPU frequency changes automatically. The frequency depends on the CPU load and the peripherals used.
- During Deep-sleep, when the ULP co-processor is powered on, peripherals such as GPIO and I2C are able to work.
- When the system works in the ULP sensor-monitored pattern, the ULP co-processor works with the ULP sensor periodically; ADC works with a duty cycle of 1%, so the power consumption is 100 μA.

4. Peripherals and Sensors

4.1 Peripherals and Sensors Description

Table 7: Description of Peripherals and Sensors

Interface	Signal	Pin	Function
ADC	ADC1_CH0	SENSOR_VP	Two 12-bit SAR ADCs
	ADC1_CH3	SENSOR_VN	
	ADC1_CH4	IO32	
	ADC1_CH5	IO33	
	ADC1_CH6	IO34	
	ADC1_CH7	IO35	
	ADC2_CH0	IO4	
	ADC2_CH1	IO0	
	ADC2_CH2	IO2	
	ADC2_CH3	IO15	
	ADC2_CH4	IO13	
	ADC2_CH5	IO12	
	ADC2_CH6	IO14	
	ADC2_CH7	IO27	
	ADC2_CH8	IO25	
	ADC2_CH9	IO26	
Ultra-Low Noise Analog Pre-Amplifier	SENSOR_VP	IO36	Provides about 60 dB gain by using larger capacitors on PCB
	SENSOR_VN	IO39	
DAC	DAC_1	IO25	Two 8-bit DACs
	DAC_2	IO26	
Touch Sensor	TOUCH0	IO4	Capacitive touch sensors
	TOUCH1	IO0	
	TOUCH2	IO2	
	TOUCH3	IO15	
	TOUCH4	IO13	
	TOUCH5	IO12	
	TOUCH6	IO14	
	TOUCH7	IO27	
	TOUCH8	IO33	
	TOUCH9	IO32	
SD/SDIO/MMC Host Controller	HS2_CLK	MTMS	Supports SD memory card V3.01 standard
	HS2_CMD	MTDO	
	HS2_DATA0	IO2	
	HS2_DATA1	IO4	
	HS2_DATA2	MTDI	
	HS2_DATA3	MTCK	

Interface	Signal	Pin	Function
Motor PWM	PWM0_OUT0~2	Any GPIOs*	Three channels of 16-bit timers generate PWM waveforms. Each channel has a pair of output signals, three fault detection signals, three event-capture signals, and three sync signals.
	PWM1_OUT_IN0~2		
	PWM0_FLT_IN0~2		
	PWM1_FLT_IN0~2		
	PWM0_CAP_IN0~2		
	PWM1_CAP_IN0~2		
	PWM0_SYNC_IN0~2		
	PWM1_SYNC_IN0~2		
LED PWM	ledc_hs_sig_out0~7	Any GPIOs*	16 independent channels @80 MHz clock/RTC CLK. Duty accuracy: 16 bits.
	ledc_ls_sig_out0~7		
UART	U0RXD_in	Any GPIOs*	Two UART devices with hardware flow-control and DMA
	U0CTS_in		
	U0DSR_in		
	U0TXD_out		
	U0RTS_out		
	U0DTR_out		
	U1RXD_in		
	U1CTS_in		
	U1TXD_out		
	U1RTS_out		
	U2RXD_in		
	U2CTS_in		
	U2TXD_out		
	U2RTS_out		
I2C	I2CEXT0_SCL_in	Any GPIOs*	Two I2C devices in slave or master modes
	I2CEXT0_SDA_in		
	I2CEXT1_SCL_in		
	I2CEXT1_SDA_in		
	I2CEXT0_SCL_out		
	I2CEXT0_SDA_out		
	I2CEXT1_SCL_out		
	I2CEXT1_SDA_out		

Interface	Signal	Pin	Function
I2S	I2S0I_DATA_in0~15	Any GPIOs*	Stereo input and output from/to the audio codec, and parallel LCD data output
	I2S0O_BCK_in		
	I2S0O_WS_in		
	I2S0I_BCK_in		
	I2S0I_WS_in		
	I2S0I_H_SYNC		
	I2S0I_V_SYNC		
	I2S0I_H_ENABLE		
	I2S0O_BCK_out		
	I2S0O_WS_out		
	I2S0I_BCK_out		
	I2S0I_WS_out		
	I2S0O_DATA_out0~23		
	I2S1I_DATA_in0~15		
	I2S1O_BCK_in		
	I2S1O_WS_in		
	I2S1I_BCK_in		
	I2S1I_WS_in		
	I2S1I_H_SYNC		
	I2S1I_V_SYNC		
	I2S1I_H_ENABLE		
	I2S1O_BCK_out		
	I2S1O_WS_out		
	I2S1I_BCK_out		
	I2S1I_WS_out		
	I2S1O_DATA_out0~23		
Remote Controller	RMT_SIG_IN0~7	Any GPIOs*	Eight channels of IR transmitter and receiver for various waveforms
	RMT_SIG_OUT0~7		

Interface	Signal	Pin	Function
Parallel QSPI	SPIHD	SHD/SD2	Supports Standard SPI, Dual SPI, and Quad SPI that can be connected to the external flash and SRAM
	SPIWP	SWP/SD3	
	SPICS0	SCS/CMD	
	SPICLK	SCK/CLK	
	SPIQ	SDO/SD0	
	SPID	SDI/SD1	
	HSPICLK	IO14	
	HSPICS0	IO15	
	HSPIQ	IO12	
	HSPID	IO13	
	HSPIHD	IO4	
	HSPIWP	IO2	
	VSPICLK	IO18	
	VSPICS0	IO5	
	VSPIQ	IO19	
	VSPID	IO23	
	VSPIHD	IO21	
	VSPIWP	IO22	
General Purpose SPI	HSPIQ_in/_out	Any GPIOs*	Standard SPI consists of clock, chip-select, MOSI and MISO. These SPIs can be connected to LCD and other external devices. They support the following features: • both master and slave modes; • 4 sub-modes of the SPI format transfer that depend on the clock phase (CPHA) and clock polarity (CPOL) control; • configurable SPI frequency; • up to 64 bytes of FIFO and DMA.
	HSPID_in/_out		
	HSPICLK_in/_out		
	HSPI_CS0_in/_out		
	HSPI_CS1_out		
	HSPI_CS2_out		
	VSPIQ_in/_out		
	VSPID_in/_out		
	VSPICLK_in/_out		
	VSPI_CS0_in/_out		
	VSPI_CS1_out		
	VSPI_CS2_out		
JTAG	MTDI	IO12	JTAG for software debugging
	MTCK	IO13	
	MTMS	IO14	
	MTDO	IO15	

Interface	Signal	Pin	Function
SDIO Slave	SD_CLK	IO6	SDIO interface that conforms to the industry standard SDIO 2.0 card specification.
	SD_CMD	IO11	
	SD_DATA0	IO7	
	SD_DATA1	IO8	
	SD_DATA2	IO9	
	SD_DATA3	IO10	
EMAC	EMAC_TX_CLK	IO0	Ethernet MAC with MII/RMII interface
	EMAC_RX_CLK	IO5	
	EMAC_TX_EN	IO21	
	EMAC_TXD0	IO19	
	EMAC_TXD1	IO22	
	EMAC_TXD2	IO14	
	EMAC_TXD3	IO12	
	EMAC_RX_ER	IO13	
	EMAC_RX_DV	IO27	
	EMAC_RXD0	IO25	
	EMAC_RXD1	IO26	
	EMAC_RXD2	TXD0	
	EMAC_RXD3	IO15	
	EMAC_CLK_OUT	IO16	
	EMAC_CLK_OUT_180	IO17	
	EMAC_TX_ER	IO4	
	EMAC_MDC_out	Any GPIOs*	
	EMAC_MDI_in	Any GPIOs*	
	EMAC_MDO_out	Any GPIOs*	
	EMAC_CRS_out	Any GPIOs*	
	EMAC_COL_out	Any GPIOs*	

Note:

- Functions of Motor PWM, LED PWM, UART, I2C, I2S, general purpose SPI and Remote Controller can be configured to any GPIO except GPIO6, GPIO7, GPIO8, GPIO9, GPIO10 and GPIO11.
- For the items marked with "Any GPIOs*" in the "Pin" column, users should note that GPIO6, GPIO7, GPIO8, GPIO9, GPIO10 and GPIO11 are connected to the integrated SPI flash of ESP-WROOM-32 and are not recommended for other uses.

5. Electrical Characteristics

Note:
The specifications in this chapter have been tested under the following general condition: VDD = 3.3V, T_A = 27°C, unless otherwise specified.

5.1 Absolute Maximum Ratings

Table 8: Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Power supply	VDD	2.7	3.3	3.6	V
Minimum current delivered by power supply	I_{VDD}	0.5	-	-	A
Input low voltage	V_{IL}	-0.3	-	0.25×V_{IO}[1]	V
Input high voltage	V_{IH}	0.75×V_{IO}[1]	-	V_{IO}[1]+0.3	V
Input leakage current	I_{IL}	-	-	50	nA
Input pin capacitance	C_{pad}	-	-	2	pF
Output low voltage	V_{OL}	-	-	0.1×V_{IO}[1]	V
Output high voltage	V_{OH}	0.8×V_{IO}[1]	-	-	V
Maximum output drive capability	I_{MAX}	-	-	40	mA
Storage temperature range	T_{STR}	-40	-	85	°C
Operating temperature range	T_{OPR}	-40	-	85	°C

1. V_{IO} is the power supply for a specific pad. More details can be found in the ESP32 Datasheet, Appendix IO_MUX. For example, the power supply for SD_CLK is the VDD_SDIO.

5.2 Wi-Fi Radio

Table 9: Wi-Fi Radio Characteristics

Description	Min	Typical	Max	Unit
Input frequency	2412	-	2484	MHz
Input reflection	-	-	-10	dB
Tx power				
Output power of PA for 72.2 Mbps	13	14	15	dBm
Output power of PA for 11b mode	19.5	20	20.5	dBm
Sensitivity				
DSSS, 1 Mbps	-	-98	-	dBm
CCK, 11 Mbps	-	-91	-	dBm
OFDM, 6 Mbps	-	-93	-	dBm
OFDM, 54 Mbps	-	-75	-	dBm
HT20, MCS0	-	-93	-	dBm
HT20, MCS7	-	-73	-	dBm

Description	Min	Typical	Max	Unit
HT40, MCS0	-	-90	-	dBm
HT40, MCS7	-	-70	-	dBm
MCS32	-	-89	-	dBm
Adjacent channel rejection				
OFDM, 6 Mbps	-	37	-	dB
OFDM, 54 Mbps	-	21	-	dB
HT20, MCS0	-	37	-	dB
HT20, MCS7	-	20	-	dB

5.3 BLE Radio

5.3.1 Receiver

Table 10: Receiver Characteristics — BLE

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity @30.8% PER	-	-	-97	-	dBm
Maximum received signal @30.8% PER	-	0	-	-	dBm
Co-channel C/I	-	-	+10	-	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	-	-5	-	dB
	F = F0 - 1 MHz	-	-5	-	dB
	F = F0 + 2 MHz	-	-25	-	dB
	F = F0 - 2 MHz	-	-35	-	dB
	F = F0 + 3 MHz	-	-25	-	dB
	F = F0 - 3 MHz	-	-45	-	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	-10	-	-	dBm
	2000 MHz ~ 2400 MHz	-27	-	-	dBm
	2500 MHz ~ 3000 MHz	-27	-	-	dBm
	3000 MHz ~ 12.5 GHz	-10	-	-	dBm
Intermodulation	-	-36	-	-	dBm

5.3.2 Transmitter

Table 11: Transmitter Characteristics — BLE

Parameter	Conditions	Min	Typ	Max	Unit
RF transmit power	-	-	0	-	dBm
Gain control step	-	-	±3	-	dBm
RF power control range	-	-12	-	+12	dBm

Parameter	Conditions	Min	Typ	Max	Unit
Adjacent channel transmit power	F = F0 + 1 MHz	-	-14.6	-	dBm
	F = F0 - 1 MHz	-	-12.7	-	dBm
	F = F0 + 2 MHz	-	-44.3	-	dBm
	F = F0 - 2 MHz	-	-38.7	-	dBm
	F = F0 + 3 MHz	-	-49.2	-	dBm
	F = F0 - 3 MHz	-	-44.7	-	dBm
	F = F0 + > 3 MHz	-	-50	-	dBm
	F = F0 - > 3 MHz	-	-50	-	dBm
$\Delta f1_{avg}$	-	-	-	265	kHz
$\Delta f2_{max}$	-	247	-	-	kHz
$\Delta f2_{avg}/\Delta f1_{avg}$	-	-	-0.92	-	-
ICFT	-	-	-10	-	kHz
Drift rate	-	-	0.7	-	kHz/50 μs
Drift	-	-	2	-	kHz

5.4 Reflow Profile

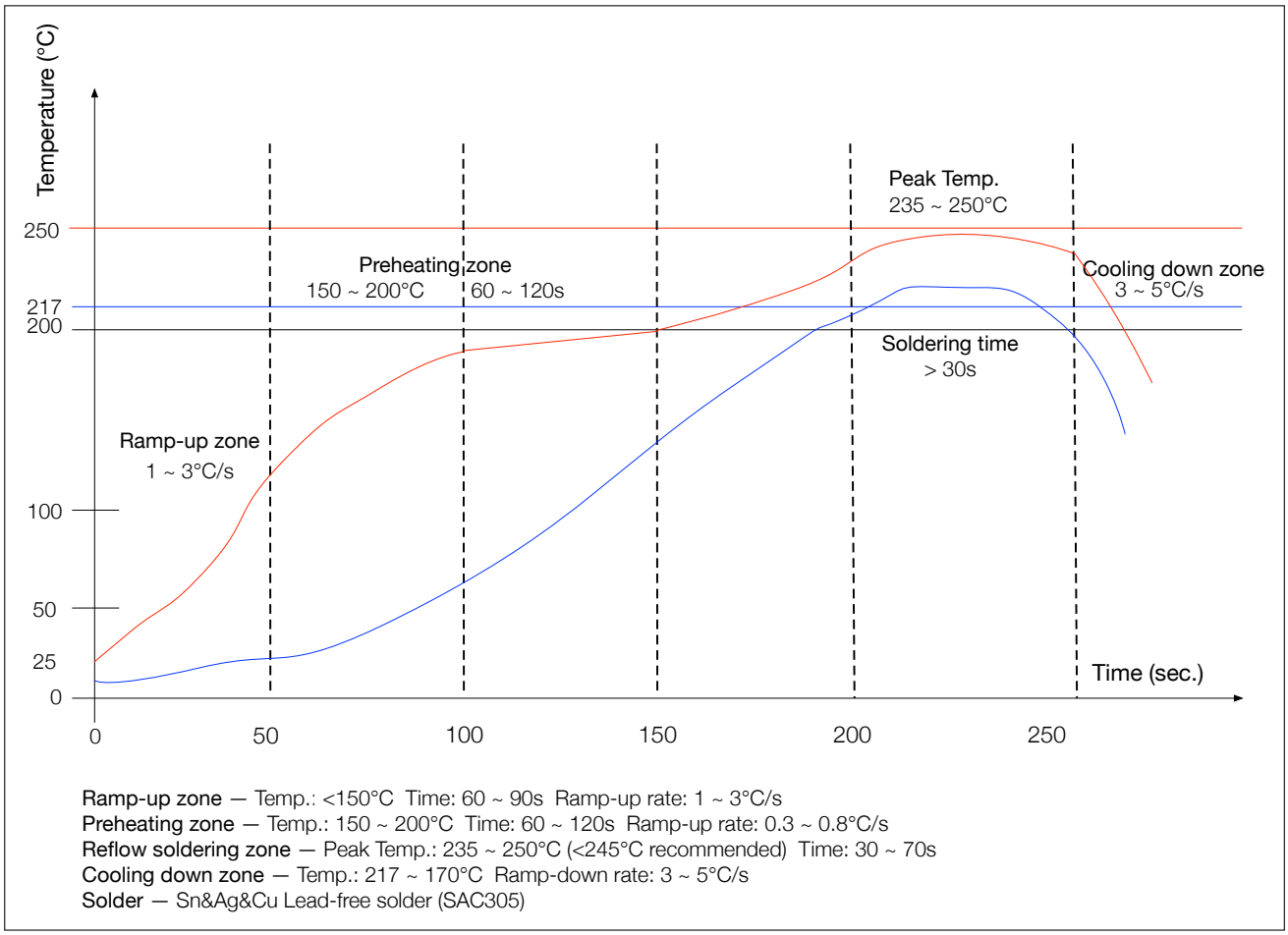


Figure 2: Reflow Profile

6. Schematics

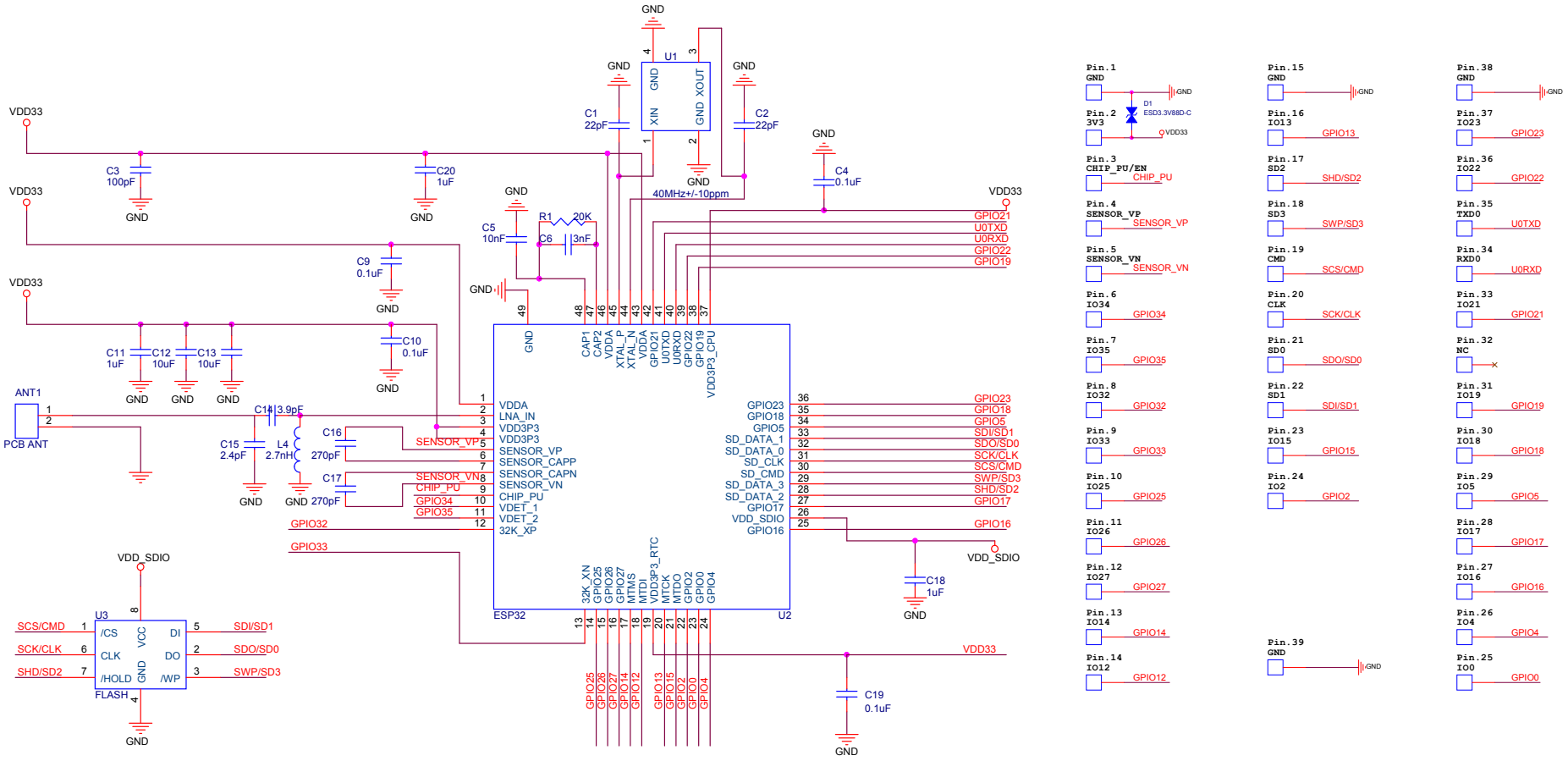


Figure 3: ESP-WROOM-32 Schematics

7. Peripheral Schematics

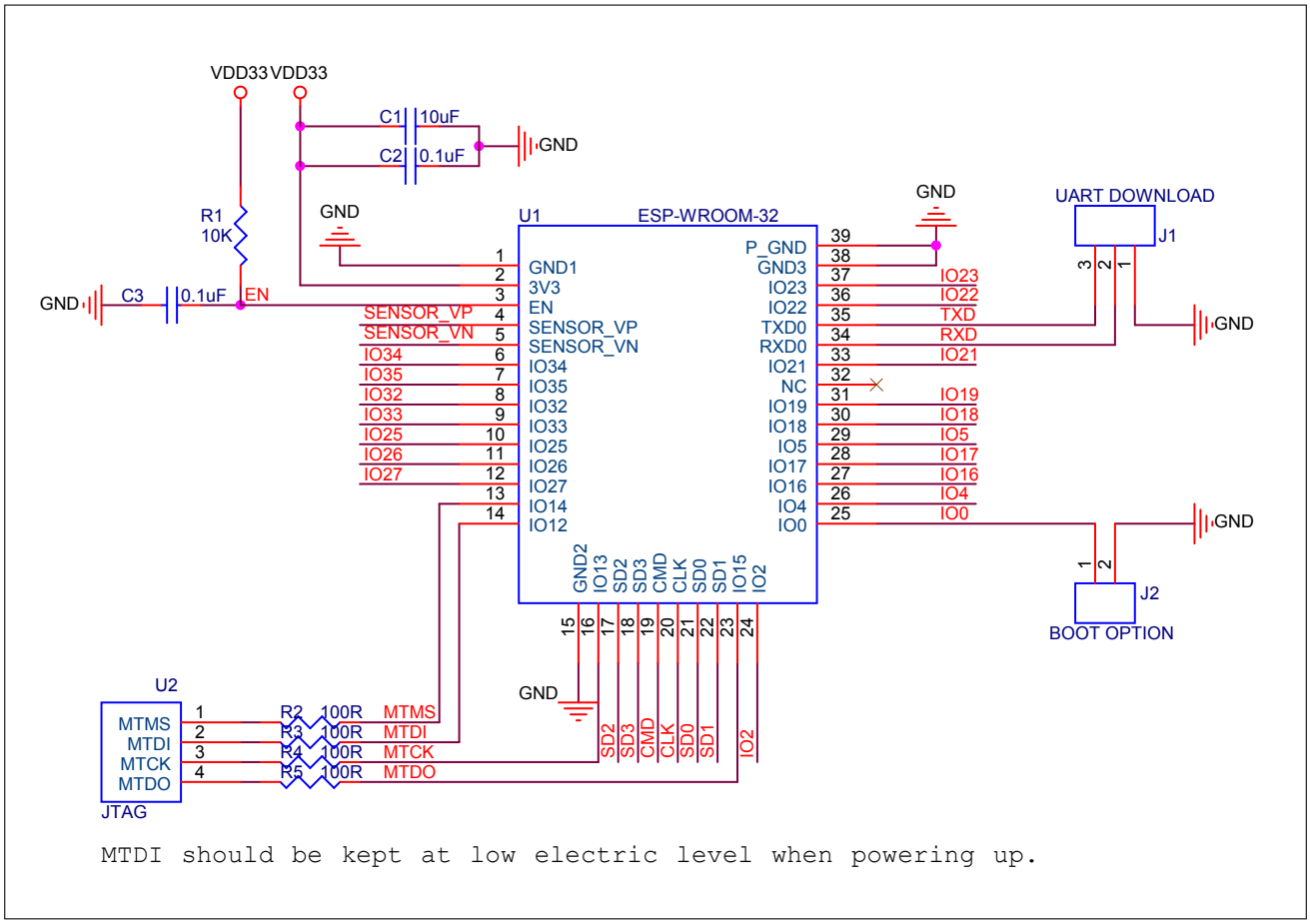


Figure 4: ESP-WROOM-32 Peripheral Schematics

Note:

Soldering Pad 39 to the Ground of the base board is not necessary for a satisfactory thermal performance. If users do want to solder it, they need to ensure that the correct quantity of soldering paste is applied.

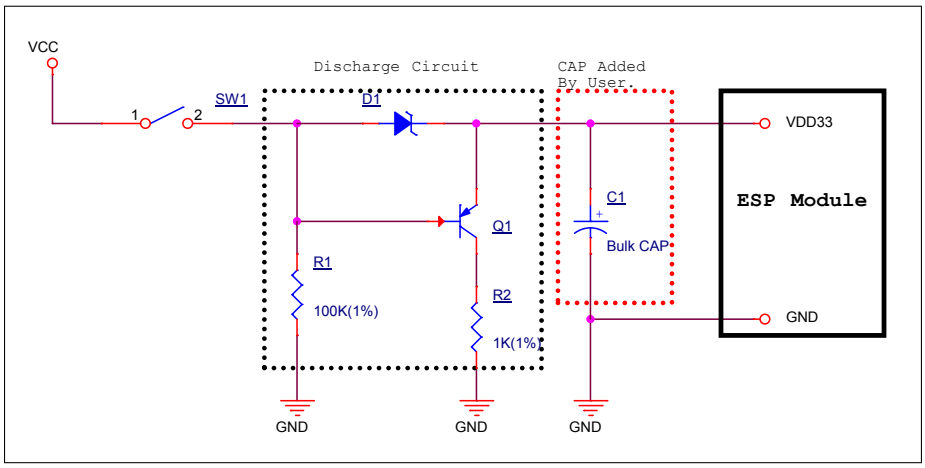


Figure 5: Discharge Circuit for VDD33 Rail

Note:

The discharge circuit can be applied in scenarios where ESP32 is powered on and off repeatedly by switching the power rails, and there is a large capacitor on the VDD33 rail. For details, please refer to Section **Power Scheme** in ESP32 Datasheet.

8. Dimensions

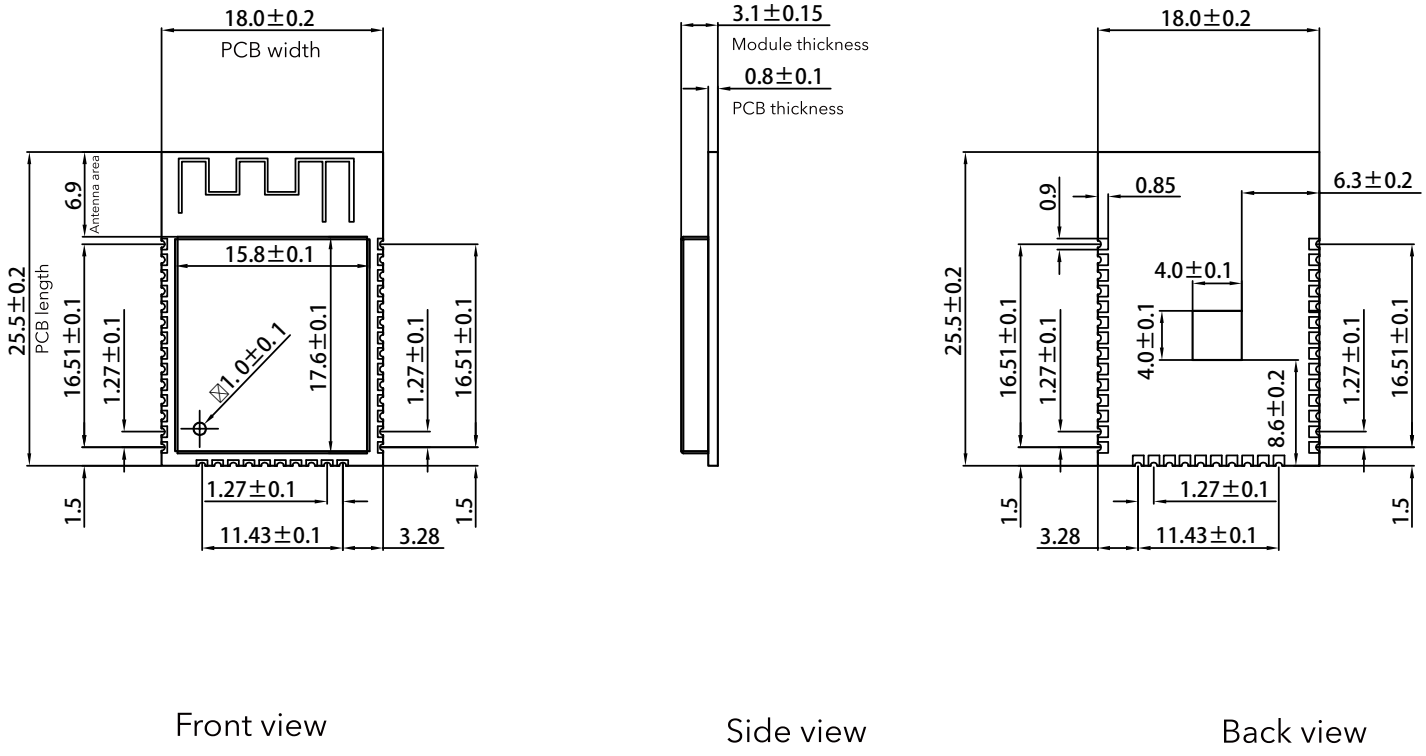


Figure 6: Dimensions of ESP-WROOM-32

Note:
All dimensions are in millimeters.

9. Learning Resources

9.1 Must-Read Documents

The following link provides documents related to ESP32.

- ESP32 Datasheet
  This document provides an introduction to the specifications of the ESP32 hardware, including overview, pin definitions, functional description, peripheral interface, electrical characteristics, etc.
- ESP32 Technical Reference Manual
  The manual provides detailed information on how to use the ESP32 memory and peripherals.
- ESP32 Hardware Resources
  The zip files include the schematics, PCB layout, Gerber and BOM list of ESP32 modules and development boards.
- ESP32 Hardware Design Guidelines
  The guidelines outline recommended design practices when developing standalone or add-on systems based on the ESP32 series of products, including ESP32, the ESP-WROOM-32 module, and ESP32-DevKitC—the development board.
- ESP32 AT Instruction Set and Examples
  This document introduces the ESP32 AT commands, explains how to use them, and provides examples of several common AT commands.

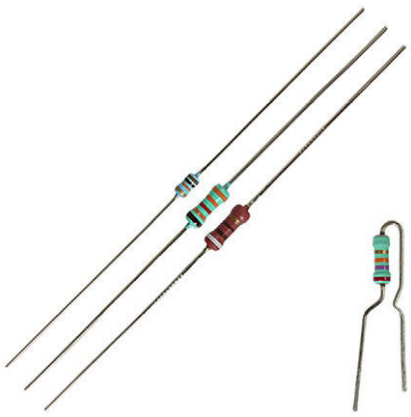
9.2 Must-Have Resources

Here are the ESP32-related must-have resources.

- ESP32 BBS
  This is an Engineer-to-Engineer (E2E) Community for ESP32 where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
- ESP32 GitHub
  ESP32 development projects are freely distributed under Espressif's MIT license on GitHub. It is established to help developers get started with ESP32 and foster innovation and the growth of general knowledge about the hardware and software surrounding ESP32 devices.
- ESP32 Tools
  This is a webpage where users can download ESP32 Flash Download Tools and the zip file "ESP32 Certification and Test".
- ESP-IDF
  This webpage links users to the official IoT development framework for ESP32.
- ESP32 Resources
  This webpage provides the links to all available ESP32 documents, SDK and tools.

2.2.5. Resistencias

Standard Metal Film Leaded Resistors



FEATURES

- Small size (SFR16S: 0204, SFR25 / SFR25H: 0207)
- Low noise (max. 1.5 µV/V for $R > 1$ MΩ)
- Compatible to both lead (Pb)-free and lead containing soldering processes
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

HALOGEN FREE

APPLICATIONS

- General purpose resistors

A homogeneous film of metal alloy is deposited on a high grade ceramic body. After a helical groove has been cut in the resistive layer, tinned connecting leads of electrolytic copper are welded to the end-caps.

The resistors are coated with a colored lacquer (light-blue for type SFR16S; light-green for type SFR25 and red-brown for type SFR25H) which provides electrical, mechanical, and climatic protection. The encapsulation is resistant to all cleaning solvents in accordance with IEC 60068-2-45.

TECHNICAL SPECIFICATIONS

DESCRIPTION	SFR16S	SFR25	SFR25H
DIN size	0204	0207	0207
Resistance range	1 Ω to 3 MΩ; jumper (0 Ω)	0.22 Ω to 10 MΩ; jumper (0 Ω)	0.22 Ω to 10 MΩ
Resistance tolerance	± 5 %; ± 1 %		
Temperature coefficient	± 250 ppm/K; ± 100 ppm/K		
Rated dissipation, P_{70}	0.5 W	0.4 W	0.5 W
Thermal resistance	170 K/W	200 K/W	150 K/W
Operating voltage, $U_{max.}$ AC/DC	200 V	250 V	350 V
Operating temperature range	-55 °C to 155 °C		
Permissible film temperature	155 °C		
Max. resistance change at rated dissipation $\lvert\Delta R/R$ max.$\rvert$, after 1000 h	± (2 % R + 0.05 Ω)		

Note

- R value is measured with probe distance of 24 mm ± 1 mm using 4-terminal method.

TEMPERATURE COEFFICIENT AND RESISTANCE RANGE

TYPE	TOLERANCE	TCR	RESISTANCE	E-SERIES
SFR16S	± 5 %	± 250 ppm/K	1 Ω to ≤ 4.7 Ω	E24
		± 100 ppm/K	4.7 Ω to 100 kΩ	
		± 250 ppm/K	> 100 kΩ to 3 MΩ	
	± 1 %	± 100 ppm/K	5.6 Ω to 100 kΩ	E24; E96
		± 250 ppm/K	> 100 kΩ to 976 kΩ	
	Jumper (0 Ω)	-	≤ 30 mΩ; $I_{max.}$ = 3 A	-
SFR25, SFR25H	± 5 %	± 250 ppm/K	0.22 Ω to 4.7 Ω	E24
		± 100 ppm/K	> 4.7 Ω to 1 MΩ	
		± 250 ppm/K	> 1 MΩ to 10 MΩ	
	± 1 %	± 250 ppm/K	1 Ω to 4.7 Ω	E24; E96
		± 100 ppm/K	> 4.7 Ω to 1 MΩ	
		± 250 ppm/K	> 1 MΩ to 10 MΩ	
	Jumper (0 Ω) (1)	-	≤ 30 mΩ; $I_{max.}$ = 5 A	-

Note

(1) Jumper is only available for SFR25.

PART NUMBER AND PRODUCT DESCRIPTION

PART NUMBER: SFR2500001001FA500

S	F	R	2	5	0	0	0	0	1	0	0	1	F	A	5	0	0

TYPE	VARIANT	TCR/MATERIAL	RESISTANCE	TOLERANCE	PACKAGING	SPECIAL
SFR16S0 **SFR2500** **SFR25H0**	**0** = neutral **Z** = value overflow (special)	**0** = standard **Z** = jumper	**3 digit value** **1 digit multiplier** MULTIPLIER **7** = $*10^{-3}$ **2** = $*10^{2}$ **8** = $*10^{-2}$ **3** = $*10^{3}$ **9** = $*10^{-1}$ **4** = $*10^{4}$ **0** = $*10^{0}$ **5** = $*10^{5}$ **1** = $*10^{1}$ **Z** = 0000	**F** = ± 1 % **J** = ± 5 % **Z** = jumper	**N4** **A5** **A1** **R5**	The 2 digits are used for all special parts. **00** = standard

PRODUCT DESCRIPTION: SFR25 1 % A5 1K0

SFR25	1 %	A5	1K0
TYPE	TOLERANCE	PACKAGING (1)	RESISTANCE VALUE
SFR16S **SFR25** **SFR25H**	**± 1 %** **± 5 %**	**N4** **A5** **A1** **R5**	**47K** = 47 kΩ **51R1** = 51.1 Ω

Notes

- The products can be ordered using either the PRODUCT DESCRIPTION or the PART NUMBER.

(1) N4 packaging indicates SFR25 and SFR25H radial version.

PACKAGING						
TYPE	CODE	QUANTITY	PACKAGING STYLE	WIDTH	PITCH	DIMENSIONS
SFR16S	A5	5000	Taped acc. to IEC 60286-1 fan-folded in a box	52 mm	5 mm	75 mm x 73 mm x 270 mm
	R5	5000	Taped acc. to IEC 60286-1 on a reel			92 mm x 278 mm x 278 mm
	A1 (1)	1000	Taped acc. to IEC 60286-1 fan-folded in a box			75 mm x 28 mm x 262 mm
SFR25, SFR25H	A5	5000	Taped acc. to IEC 60286-1 fan-folded in a box	52 mm	5 mm	75 mm x 98 mm x 270 mm
	R5	5000	Taped acc. to IEC 60286-1 on a reel			93 mm x 300 mm x 298 mm
	A1 (1)	1000	Taped acc. to IEC 60286-1 fan-folded in a box			75 mm x 28 mm x 262 mm
	N4 (2)	4000	Taped acc. to IEC 60286-2 fan-folded in a box	-	12.7 mm	45 mm x 262 mm x 330 mm

Notes

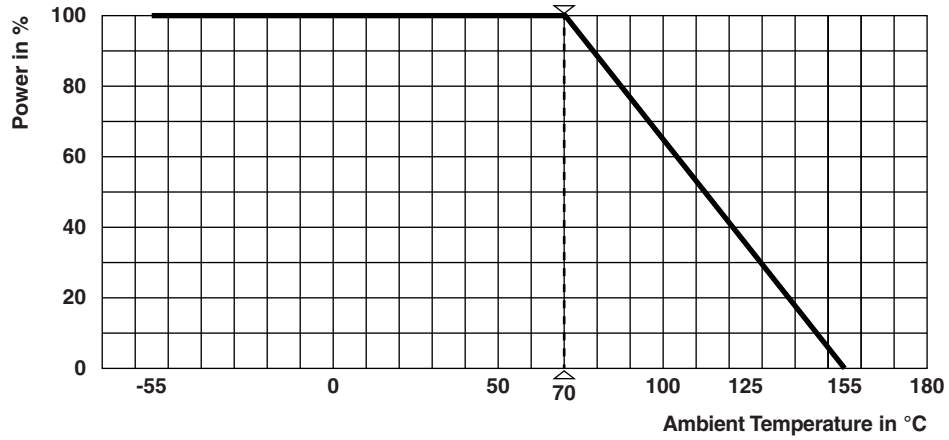
(1) A1 packaging only available for resistors with ± 5 % tolerance.

(2) N4 packaging only available for SFR25 and SFR25H radial version.

MARKING

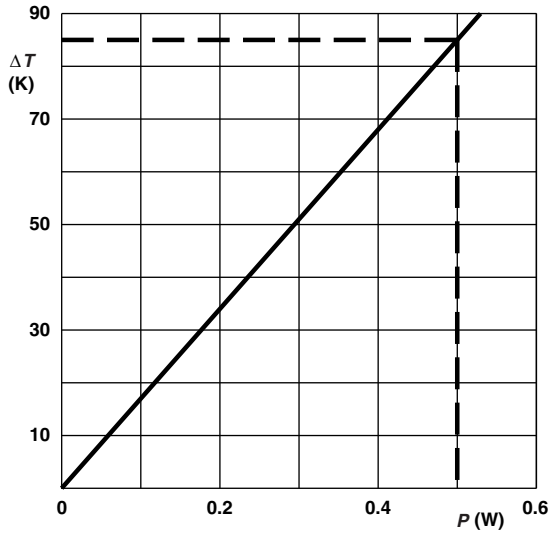
The nominal resistance and tolerance are marked on the resistor using four or five colored bands in accordance with IEC 60062, marking codes for resistors and capacitors.

FUNCTIONAL PERFORMANCE

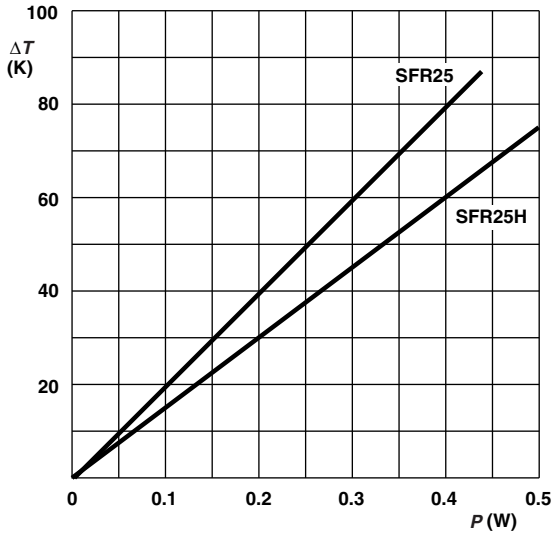


Derating

Maximum dissipation ($P_{max.}$) in percentage of rated power as a function of the ambient temperature (T_{amb})



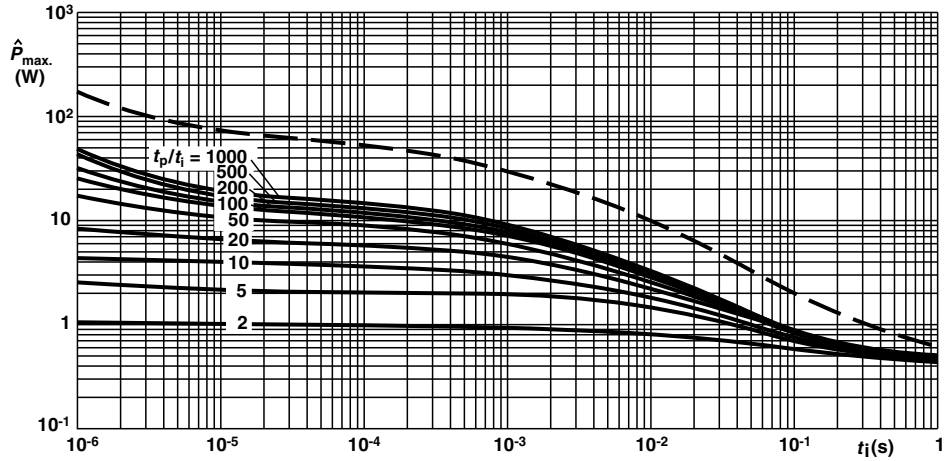
SFR16S Hot-spot temperature rise (ΔT) as a function of dissipated power



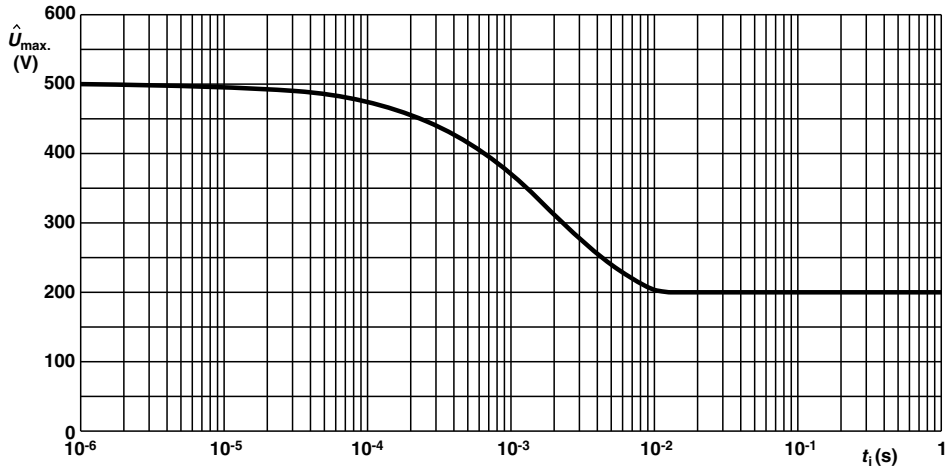
SFR25/SFR25H Hot-spot temperature rise (ΔT) as a function of dissipated power

Note

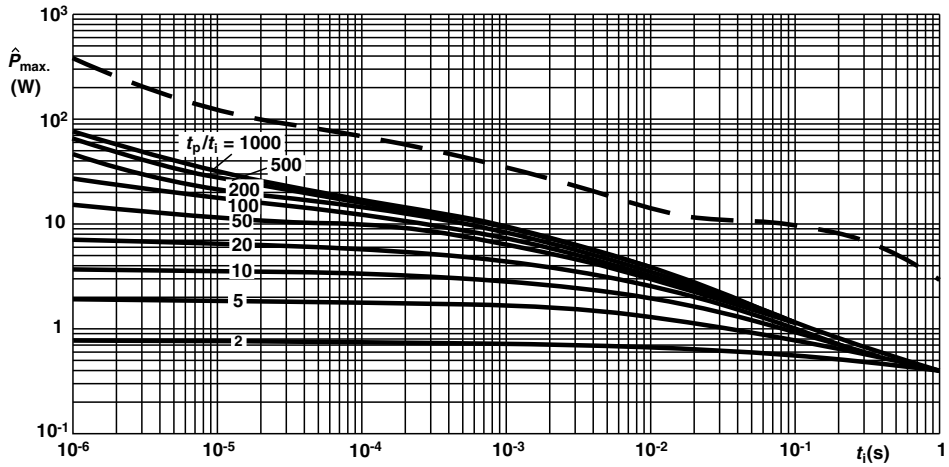
- The maximum permissible hot-spot temperature is 155 °C.



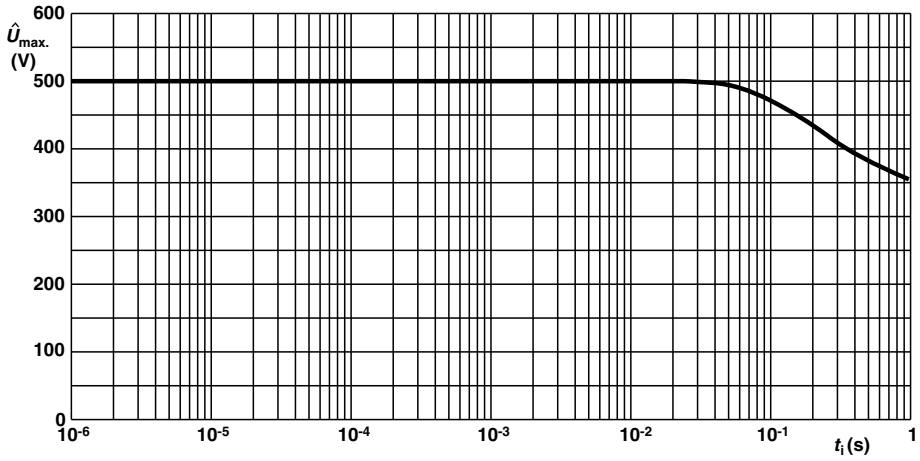
SFR16S Pulse on a regular basis; maximum permissible peak pulse power ($\hat{P}_{max.}$) as a function of pulse duration (t_i)



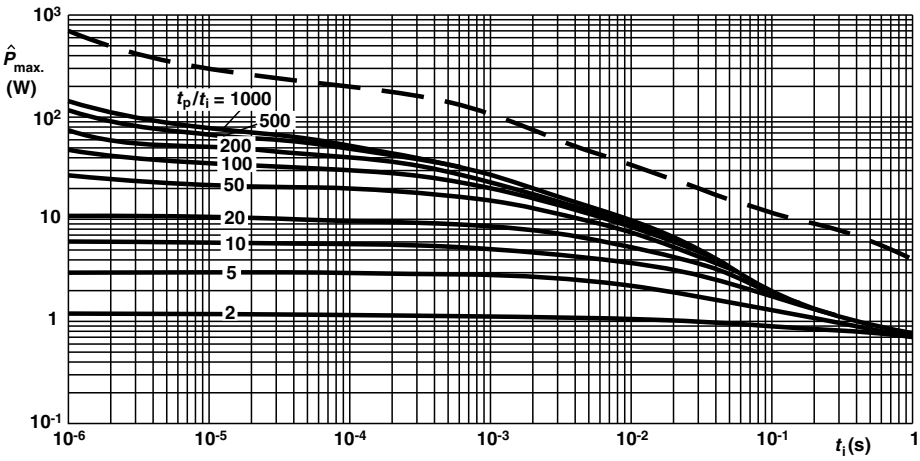
SFR16S Pulse on a regular basis; maximum permissible peak pulse voltage ($\hat{U}_{max.}$) as a function of pulse duration (t_i)



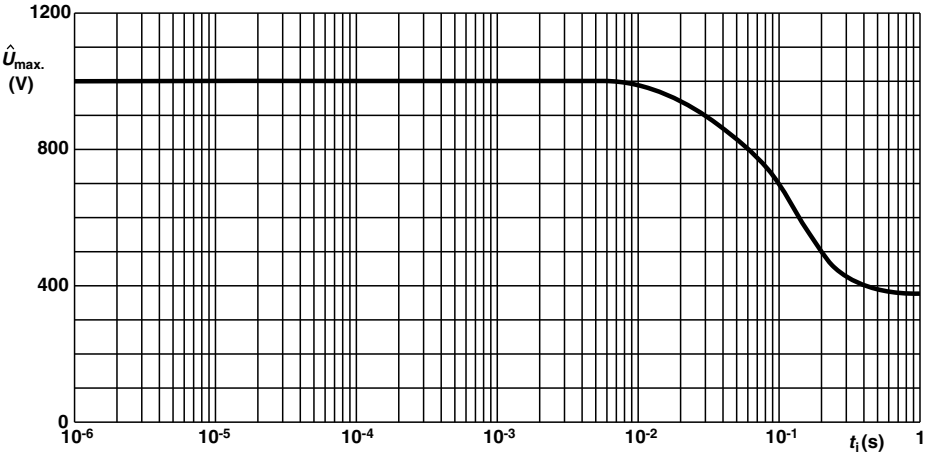
SFR25 Pulse on a regular basis; maximum permissible peak pulse power ($\hat{P}_{max.}$) as a function of pulse duration (t_i)



SFR25 Pulse on a regular basis; maximum permissible peak pulse voltage ($\hat{U}_{max.}$) as a function of pulse duration (t_i)



SFR25H Pulse on a regular basis; maximum permissible peak pulse power ($\hat{P}_{max.}$) as a function of pulse duration (t_i)



SFR25H Pulse on a regular basis; maximum permissible peak pulse voltage ($\hat{U}_{max.}$) as a function of pulse duration (t_i)

TESTS PROCEDURES AND REQUIREMENTS

All tests are carried out in accordance with the following specifications:

- EN 60115-1, generic specification (includes tests)

The test and requirements table contains only the most important tests. For the full test schedule refer to the documents listed above.

The tests are carried out in accordance with IEC 60068-2-xx test method and under standard atmospheric conditions in accordance with IEC 60068-1, 5.3.

Unless otherwise specified the following values apply:

- Temperature: 15 °C to 35 °C
- Relative humidity: 45 % to 75 %
- Air pressure: 86 kPa to 106 kPa (860 mbar to 1060 mbar).

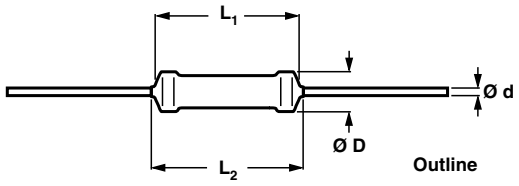
For performing some of the tests, the components are mounted on a test board in accordance with IEC 60115-1, 4.31. In test procedures and requirements table, only the tests and requirements are listed with reference to the relevant clauses of IEC 60115-1 and IEC 60068-2-xx test methods. A short description of the test procedure is also given.

TEST PROCEDURES AND REQUIREMENTS

IEC 60115-1 CLAUSE	IEC 60068-2 TEST METHOD	TEST	PROCEDURE	REQUIREMENTS PERMISSIBLE CHANGE ($\Delta R_{max.}$)				
4.5	-	Resistance	-	± 5 %; ± 1 %				
4.8	-	Temperature coefficient	At (20 / -55 / 20) °C and (20 / 155 / 20) °C	± 250 ppm/K; ± 100 ppm/K				
4.12	-	Noise	IEC 60195		< 68 kΩ	68 kΩ to 100 kΩ	> 100 kΩ to 1 MΩ	> 1 MΩ
				SFR16S	≤ 0.1 µV/V	≤ 0.5 µV/V	≤ 1.5 µV/V	≤ 1.5 µV/V
				SFR25, SFR25H	≤ 0.1 µV/V	≤ 0.1 µV/V	≤ 0.1 µV/V	≤ 1.5 µV/V
4.13	-	Short time overload	Room temperature; $P = 6.25 \times P_n$; (voltage not more than 2 x limiting voltage); 5 s	± (0.25 % R + 0.05 Ω)				
4.16	21 (Ua1) 21 (Ub) 21 (Uc)	Robustness of terminations	Tensile, bending, and torsion	± (0.25 % R + 0.05 Ω)				
4.17	20 (Ta)	Solderability	at +235 °C; 2 s; solder bath method; SnPb40 at +245 °C; 3 s; solder bath method; SnAg3Cu0.5	Good tinning (≥ 95 % covered); no damage				
4.18	20 (Tb)	Resistance to soldering heat	Unmounted components (260 ± 5) °C; (10 ± 1) s	± (0.25 % R + 0.05 Ω)				
4.19	14 (Na)	Rapid change of temperature	30 min at -55 °C and 30 min at +155 °C; 5 cycles	± (0.25 % R + 0.05 Ω)				
4.20	29 (Eb)	Bump	3 x 1500 bumps in 3 directions; 40 g	± (0.25 % R + 0.05 Ω); no damage				
4.22	6 (Fc)	Vibration	10 sweep cycles per direction; 10 Hz to 2000 Hz 1.5 mm or 200 m/s^2	± (0.25 % R + 0.05 Ω); no damage				
4.23		Climatic sequence:						
4.23.2	2 (Ba)	Dry heat	155 °C; 16 h					
4.23.3	30 (Db)	Damp heat, cyclic	55 °C; 24 h; 90 % to 100 % RH; 1 cycle					
4.23.4	1 (Aa)	Cold	-55 °C; 2 h					
4.23.5	13 (M)	Low air pressure	8.5 kPa; 2 h; 15 °C to 35 °C					
4.23.6	30 (Db)	Damp heat, cyclic	55 °C; 5 days; 95 % to 100 % RH; 5 cycles	**SFR16S, SFR25, SFR25H**	± (1 % R + 0.05 Ω); no visible damage ± (1 % R + 0.05 Ω); no visible damage			
4.23.7		DC load	apply rated power for 1 min		± 2 % R; no visible damage			

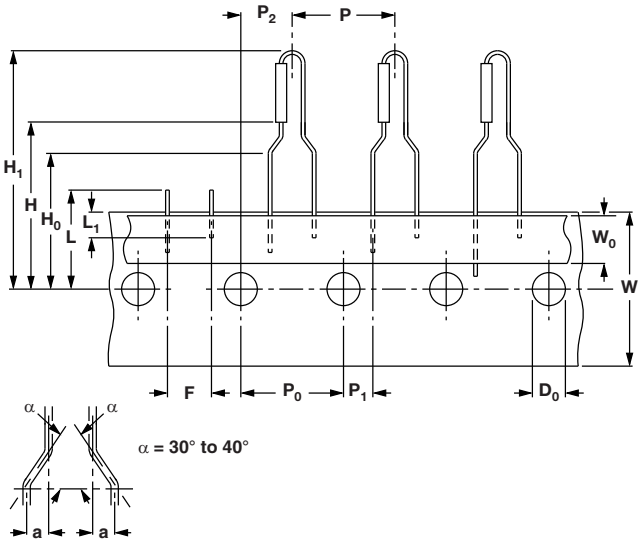
TEST PROCEDURES AND REQUIREMENTS				
IEC 60115-1 CLAUSE	IEC 60068-2 TEST METHOD	TEST	PROCEDURE	REQUIREMENTS PERMISSIBLE CHANGE ($\Delta R_{max.}$)
4.24	78 (Cab)	Damp heat (steady state)	(40 ± 2) °C; 56 days; (93 ± 3) % RH	± (2 % R + 0.05 Ω)
4.25.1		Endurance (at 70 °C)	$U = \sqrt{P_{70} \times R}$ or $U = U_{max.}$; 1.5 h on; 0.5 h off 70 °C; 1000 h	± (2 % R + 0.05 Ω)

DIMENSIONS



DIMENSIONS - Leaded resistor types, mass and relevant physical dimensions					
TYPE	Ø $D_{max.}$ (mm)	$L_{1\ max.}$ (mm)	$L_{2\ max.}$ (mm)	Ø d (mm)	MASS (mg)
SFR16S	1.9	3.5	4.1	0.45 ± 0.05	102
SFR25	2.5	6.5	7.5	0.58 ± 0.05	205
SFR25H	2.5	6.5	7.5	0.58 ± 0.05	205

SFR25, SFR25H WITH RADIAL TAPING



DIMENSIONS in millimeters		
Pitch of components	P	12.7 ± 1.0
Feed-hole pitch	P_0	12.7 ± 0.2
Feed-hole center to lead at topside at the tape	P_1	3.85 ± 0.5
Feed-hole center to body center	P_2	6.35 ± 1.0
Lead-to-lead distance	F	4.8 + 0.7 / - 0
Tape width	W	18.0 ± 0.5
Minimum hold down tape width	W_0	5.5
Maximum component height	H1	29
Lead wire clinch height	H_0	16.5 ± 0.5
Height of component from tape center	H	19.5 ± 1
Feed-hole diameter	D_0	4.0 ± 0.2
Maximum length of snipped lead	L	11.0
Minimum lead wire (tape portion) shortest lead	L_1	2.5

Note

- Please refer to document “Packaging” for more detail (www.vishay.com/doc?28721).

HISTORICAL 12NC INFORMATION

- The resistors had a 12-digit numeric code starting with 23.
- The subsequent 6 digits for 1 % or 7 digits for 5 % indicated the resistor type and packaging.
- The remaining digits indicated the resistance value:
  - The first 3 digits for 1 % or 2 digits for 5 % indicated the resistance value.
  - The last digit indicated the resistance decade.

Resistance Decade for ± 5 % Tolerance

RESISTANCE DECADE	LAST DIGIT
0.10 Ω to 0.91 Ω	7
1 Ω to 9.1 Ω	8
10 Ω o 91 Ω	9
100 Ω to 910 Ω	1
1 kΩ to 9.1 kΩ	2
10 kΩ to 91 kΩ	3
100 kΩ to 910 kΩ	4
1 MΩ to 9.1 MΩ	5
= 10 MΩ	6

Resistance Decade for ± 1 % Tolerance

RESISTANCE DECADE	LAST DIGIT
1 Ω to 9.76 Ω	8
10 Ω to 97.6 Ω	9
100 Ω to 976 Ω	1
1 kΩ to 9.76 kΩ	2
10 kΩ to 97.6 kΩ	3
100 kΩ to 976 kΩ	4
1 MΩ to 9.76 MΩ	5
= 10 MΩ	6

12NC Example

The 12NC of a SFR25 resistor, value 5600 Ω ± 5 %, taped on a bandolier of 5000 units in ammopack was:
2322 181 43562.

HISTORICAL 12NC - Resistor type and packaging

TYPE	TOL.	23..			
		BANDOLIER IN AMMOPACK			BANDOLIER ON REEL
		RADIAL TAPED	STRAIGHT LEADS		STRAIGHT LEADS
		4000 UNITS	1000 UNITS	5000 UNITS	5000 UNITS
SFR16S	± 5 %	-	..22 187 73...	..22 187 53...	..06 187 23...
	± 1 %	-	-	..06 187 3...	..06 187 1....
	Jumper	-	-	..06 187 90013	..22 187 90346
SFR25	± 5 %	..06 184 03...	..22 181 53...	..22 181 43...	..22 181 63...
	± 1 %	-	-	..22 188 2...	..06 181 8....
	Jumper	-	..22 181 90018	..22 181 90019	..06 181 90011
SFR25H	± 5 %	..06 186 03...	..22 186 16...	..22 186 76...	..06 186 63...
	± 1 %	-	-	..22 186 3....	..06 186 8....

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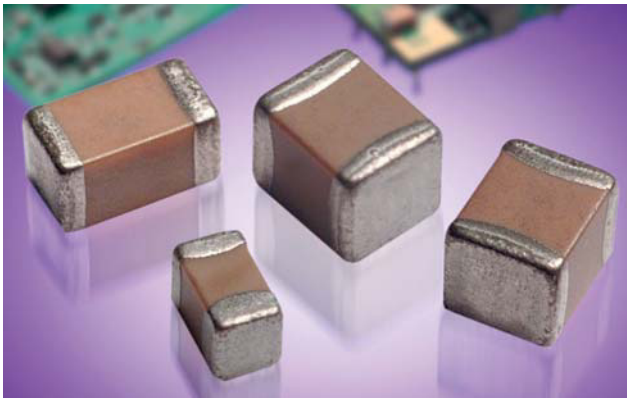
2.2.6. Condensadores

X7R Dielectric

General Specifications



X7R formulations are called “temperature stable” ceramics and fall into EIA Class II materials. X7R is the most popular of these intermediate dielectric constant materials. Its temperature variation of capacitance is within ±15% from -55°C to +125°C. This capacitance change is non-linear.

Capacitance for X7R varies under the influence of electrical operating conditions such as voltage and frequency.

X7R dielectric chip usage covers the broad spectrum of industrial applications where known changes in capacitance due to applied voltages are acceptable.

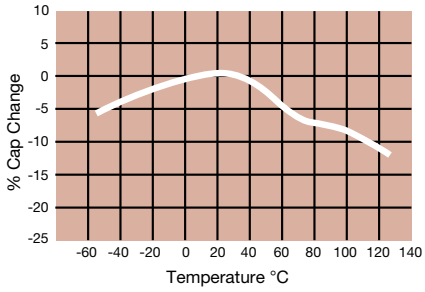
RoHS COMPLIANT

PART NUMBER (see page 2 for complete part number explanation)

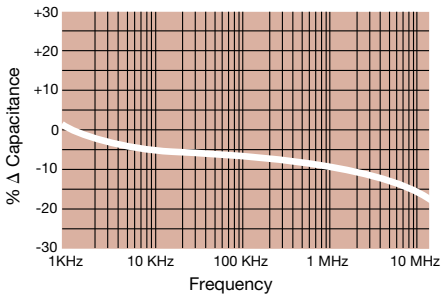
0805	5	C	103	M	A	T	2	A
Size (L" x W")	**Voltage** 4V = 4, 6.3V = 6, 10V = Z, 16V = Y, 25V = 3, 50V = 5, 100V = 1, 200V = 2, 500V = 7	**Dielectric** X7R = C	**Capacitance Code (In pF)** 2 Sig. Digits + Number of Zeros	**Capacitance Tolerance** J = ± 5%* K = ±10% M = ± 20% *≤1µF only, contact factory for additional values	**Failure Rate** A = Not Applicable	**Terminations** T = Plated Ni and Sn, 7 = Gold Plated*, Z = FLEXITERM®** *Optional termination **See FLEXITERM® X7R section	**Packaging** 2 = 7" Reel, 4 = 13" Reel **Contact Factory For Multiples**	**Special Code** A = Std. Product

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers. Contact factory for non-specified capacitance values.

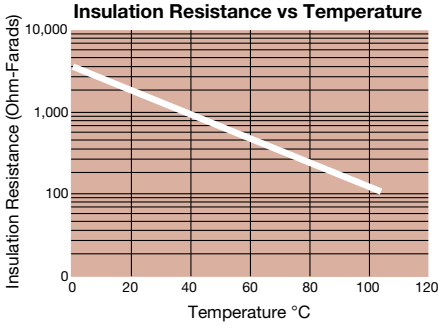
X7R Dielectric
Typical Temperature Coefficient



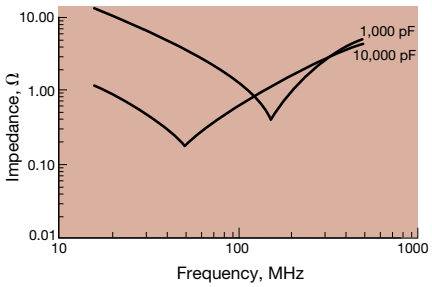
Δ Capacitance vs. Frequency



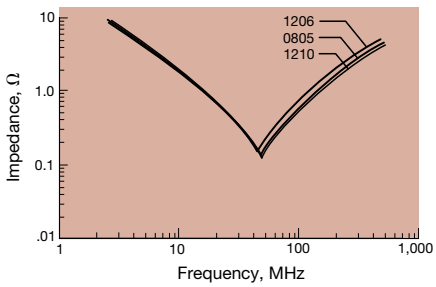
Insulation Resistance vs Temperature



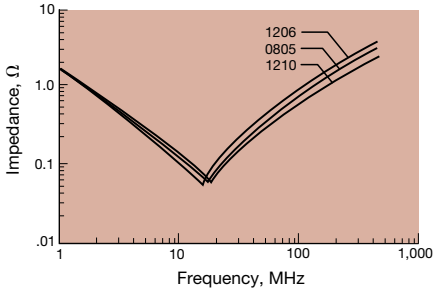
Variation of Impedance with Cap Value
Impedance vs. Frequency
1,000 pF vs. 10,000 pF - X7R
0805



Variation of Impedance with Chip Size
Impedance vs. Frequency
10,000 pF - X7R

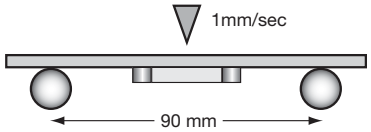


Variation of Impedance with Chip Size
Impedance vs. Frequency
100,000 pF - X7R



X7R Dielectric

Specifications and Test Methods

Parameter/Test		X7R Specification Limits	Measuring Conditions	
Operating Temperature Range		-55ºC to +125ºC	Temperature Cycle Chamber	
Capacitance		Within specified tolerance	Freq.: 1.0 kHz ± 10% Voltage: 1.0Vrms ± .2V	
Dissipation Factor		≤ 10% for ≥ 50V DC rating ≤ 12.5% for 25V DC rating ≤ 12.5% for 25V and 16V DC rating ≤ 12.5% for ≤ 10V DC rating		
Insulation Resistance		100,000MΩ or 1000MΩ - µF, whichever is less	Charge device with rated voltage for 120 ± 5 secs @ room temp/humidity	
Dielectric Strength		No breakdown or visual defects	Charge device with 250% of rated voltage for 1-5 seconds, w/charge and discharge current limited to 50 mA (max) Note: Charge device with 150% of rated voltage for 500V devices.	
Resistance to Flexure Stresses	Appearance	No defects	Deflection: 2mm Test Time: 30 seconds 	
	Capacitance Variation	≤ ±12%		
	Dissipation Factor	Meets Initial Values (As Above)		
	Insulation Resistance	≥ Initial Value x 0.3		
Solderability		≥ 95% of each terminal should be covered with fresh solder	Dip device in eutectic solder at 230 ± 5ºC for 5.0 ± 0.5 seconds	
Resistance to Solder Heat	Appearance	No defects, <25% leaching of either end terminal	Dip device in eutectic solder at 260ºC for 60 seconds. Store at room temperature for 24 ± 2 hours before measuring electrical properties.	
	Capacitance Variation	≤ ±7.5%		
	Dissipation Factor	Meets Initial Values (As Above)		
	Insulation Resistance	Meets Initial Values (As Above)		
	Dielectric Strength	Meets Initial Values (As Above)		
Thermal Shock	Appearance	No visual defects	Step 1: -55ºC ± 2º	30 ± 3 minutes
	Capacitance Variation	≤ ±7.5%	Step 2: Room Temp	≤ 3 minutes
	Dissipation Factor	Meets Initial Values (As Above)	Step 3: +125ºC ± 2º	30 ± 3 minutes
	Insulation Resistance	Meets Initial Values (As Above)	Step 4: Room Temp	≤ 3 minutes
	Dielectric Strength	Meets Initial Values (As Above)	Repeat for 5 cycles and measure after 24 ± 2 hours at room temperature	
Load Life	Appearance	No visual defects	Charge device with 1.5 rated voltage (≤ 10V) in test chamber set at 125ºC ± 2ºC for 1000 hours (+48, -0) Remove from test chamber and stabilize at room temperature for 24 ± 2 hours before measuring.	
	Capacitance Variation	≤ ±12.5%		
	Dissipation Factor	≤ Initial Value x 2.0 (See Above)		
	Insulation Resistance	≥ Initial Value x 0.3 (See Above)		
	Dielectric Strength	Meets Initial Values (As Above)		
Load Humidity	Appearance	No visual defects	Store in a test chamber set at 85ºC ± 2ºC/ 85% ± 5% relative humidity for 1000 hours (+48, -0) with rated voltage applied. Remove from chamber and stabilize at room temperature and humidity for 24 ± 2 hours before measuring.	
	Capacitance Variation	≤ ±12.5%		
	Dissipation Factor	≤ Initial Value x 2.0 (See Above)		
	Insulation Resistance	≥ Initial Value x 0.3 (See Above)		
	Dielectric Strength	Meets Initial Values (As Above)		

X7R Dielectric

Capacitance Range

PREFERRED SIZES ARE SHADED

SIZE			0101*	0201				0402					0603							0805							1206						
Soldering			Reflow Only	Reflow Only				Reflow/Wave					Reflow/Wave							Reflow/Wave							Reflow/Wave						
Packaging			Paper/Embossed	All Paper				All Paper					All Paper							Paper/Embossed							Paper/Embossed						
(L) Length		mm	0.40 ± 0.02	0.60 ± 0.09				1.00 ± 0.10					1.60 ± 0.15							2.01 ± 0.20							3.20 ± 0.20						
		(in.)	(0.016 ± 0.0008)	(0.024 ± 0.004)				(0.040 ± 0.004)					(0.063 ± 0.006)							(0.079 ± 0.008)							(0.126 ± 0.008)						
(W) Width		mm	0.20 ± 0.02	0.30 ± 0.09				0.50 ± 0.10					0.81 ± 0.15							1.25 ± 0.20							1.60 ± 0.20						
		(in.)	(0.008 ± 0.0008)	(0.011 ± 0.004)				(0.020 ± 0.004)					(0.032 ± 0.006)							(0.049 ± 0.008)							(0.063 ± 0.008)						
(t) Terminal		mm	0.10± 0.04	0.15 ± 0.05				0.25 ± 0.15					0.35 ± 0.15							0.50 ± 0.25							0.50 ± 0.25						
		(in.)	(0.004 ± 0.0016)	(0.006 ± 0.002)				(0.010 ± 0.006)					(0.014 ± 0.006)							(0.020 ± 0.010)							(0.020 ± 0.010)						
		WVDC	16	10	16	25	50	6.3	10	16	25	50	6.3	10	16	25	50	100	200	6.3	10	16	25	50	100	200	6.3	10	16	25	50	100	200	500
Cap	100	101	B	A	A	A	A			C	C	C					G	G	G														
(pF)	150	151	B	A	A	A	A			C	C	C					G	G	G														
	220	221	B	A	A	A	A			C	C	C					G	G	G														
	330	331	B	A	A	A	A			C	C	C					G	G	G		J	J	J	J	J	J							K
	470	471	B	A	A	A	A			C	C	C					G	G	G		J	J	J	J	J	J							K
	680	681	B	A	A	A				C	C	C					G	G	G		J	J	J	J	J	J							K
	1000	102	B	A	A	A			C	C	C	C					G	G	G		J	J	J	J	J	J							K
	1500	152	B	A	A	A			C	C	C	C					G	G			J	J	J	J	J	J		J	J	J	J	J	M
	2200	222	B	A	A	A			C	C	C	C					G	G			J	J	J	J	J	J		J	J	J	J	J	M
	3300	332		A	A	A			C	C	C	C					G	G			J	J	J	J	J	J		J	J	J	J	J	M
	4700	472		A	A	A			C	C	C	C					G	G			J	J	J	J	J	J		J	J	J	J	J	M
	6800	682		A	A	A			C	C	C	C					G	G			J	J	J	J	J	J		J	J	J	J	J	P
Cap	0.01	103		A	A	A			C	C	C	C				G	G	G			J	J	J	J	J	J		J	J	J	J	J	P
(µF)	0.015	153							C	C	C	C				G	G	G			J	J	J	J	J	J		J	J	J	J	M	P
	0.022	223							C	C	C	C				G	G	G			J	J	J	J	J	N		J	J	J	J	M	X
	0.033	333							C	C	C	C				G	G	J			J	J	J	J	N			J	J	J	J	M	X
	0.047	473							C	C	C	C			G	G	G	J			J	J	J	J	N			J	J	J	J	M	
	0.068	683							C	C	C	C			G	G	G	J			J	J	J	J	N			J	J	J	J	P	
	0.1	104							C	C	C	C		G	G	G	G	J			J	J	J	J	N			J	J	J	P	P	
	0.15	154											G	G	G	G					J	J	J	N	N			J	J	J	J	Q	
	0.22	224							C				G	G	J	J	J				J	J	N	N	N			J	J	J	J	Q	
	0.33	334											J	J	J	J					N	N	N	N	N			J	J	M	P	Q	
	0.47	474						C					J	J	J	J	J				N	N	N	N	N			M	M	M	P	Q	
	0.68	684											J	J	J						N	N	N					M	M	Q	Q	Q	
	1.0	105						C					J	J	J	J					N	N	N	N				M	M	Q	Q	Q	
	2.2	225											J	J	J						P	P	P	P**				Q	Q	Q	Q	Q**	
	4.7	475																			P	P	P					Q	Q	Q	Q		
	10	106																		P	P							Q	Q	Q			
	22	226																									Q	Q					
	47	476																															
	100	107																															
		WVDC	16	10	16	25	50	6.3	10	16	25	50	6.3	10	16	25	50	100	200	6.3	10	16	25	50	100	200	6.3	10	16	25	50	100	200	500
		SIZE	0101	0201				0402					0603							0805							1206						

Letter	A	B	C	E	G	J	K	M	N	P	Q	X	Y	Z
Max. Thickness	0.33 (0.013)	0.22 (0.009)	0.56 (0.022)	0.71 (0.028)	0.90 (0.035)	0.94 (0.037)	1.02 (0.040)	1.27 (0.050)	1.40 (0.055)	1.52 (0.060)	1.80 (0.071)	2.29 (0.090)	2.54 (0.100)	2.79 (0.110)
	PAPER						EMBOSSED							

PAPER and EMBOSSED available for 01005

NOTE: Contact factory for non-specified capacitance values

*EIA 01005

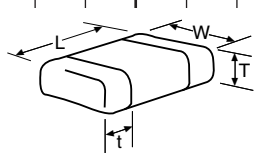
**Contact Factory for Specifications

X7R Dielectric

Capacitance Range

PREFERRED SIZES ARE SHADED

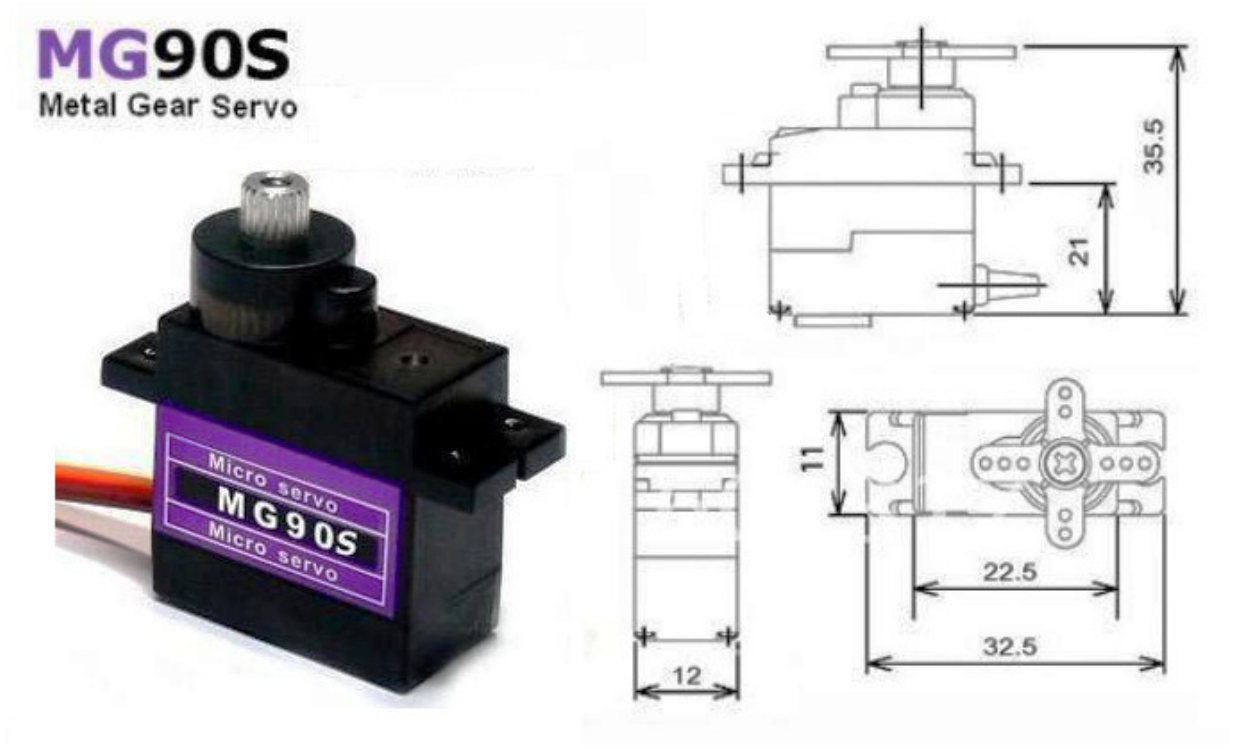
SIZE			1210							1812						1825			2220					2225		
Soldering			Reflow Only							Reflow Only						Reflow Only			Reflow Only					Reflow Only		
Packaging			Paper/Embossed							All Embossed						All Embossed			All Embossed					All Embossed		
(L) Length		mm (in.)	3.30 ± 0.4 (0.130± 0.016)							4.50 ± 0.30 (0.177 ± 0.012)						4.50 ± 0.30 (0.177 ± 0.012)			5.70 ± 0.40 (0.225 ± 0.016)					5.72 ± 0.25 (0.225 ± 0.010)		
(W) Width		mm (in.)	2.50 ± 0.20 (0.098 ± 0.008)							3.20 ± 0.20 (0.126 ± 0.008)						6.40 ± 0.40 (0.252 ± 0.016)			5.00 ± 0.40 (0.197 ± 0.016)					6.35 ± 0.25 (0.250 ± 0.010)		
(t) Terminal		mm (in.)	0.50 ± 0.25 (0.020 ± 0.010)							0.61 ± 0.36 (0.024 ± 0.014)						0.61 ± 0.36 (0.024 ± 0.014)			0.64 ± 0.39 (0.025 ± 0.015)					0.64 ± 0.39 (0.025 ± 0.015)		
		WVDC	10	16	25	50	100	200	500	16	25	50	100	200	500	50	100	200	25	50	100	200	500	50	100	200
Cap	100	101																								
(pF)	150	151																								
	220	221																								
	330	331																								
	470	471																								
	680	681																								
	1000	102																								
	1500	152	J	J	J	J	J	J	M																	
	2200	222	J	J	J	J	J	J	M																	
	3300	332	J	J	J	J	J	J	M																	
	4700	472	J	J	J	J	J	J	M																	
	6800	682	J	J	J	J	J	J	M																	
Cap	0.01	103	J	J	J	J	J	J	M		K	K	K	K	K	M	M	M		X	X	X	X	M	P	P
(µF)	0.015	153	J	J	J	J	J	J	P		K	K	K	K	P	M	M	M		X	X	X	X	M	P	P
	0.022	223	J	J	J	J	J	J	Q		K	K	K	K	P	M	M	M		X	X	X	X	M	P	P
	0.033	333	J	J	J	J	J	J	Q		K	K	K	K	X	M	M	M		X	X	X	X	M	P	P
	0.047	473	J	J	J	J	J	J	Q		K	K	K	K	Z	M	M	M		X	X	X	X	M	P	P
	0.068	683	J	J	J	J	J	M	Q		K	K	K	K	Z	M	M	M		X	X	X	X	M	P	P
	0.1	104	J	J	J	J	J	M	X		K	K	K	K	Z	M	M	M		X	X	X	X	M	P	P
	0.15	154	J	J	J	J	M	Z			K	K	K	P	Z	M	M	M		X	X	X	X	M	P	X
	0.22	224	J	J	J	J	P	Z			K	K	K	P	Z	M	M	M		X	X	X	X	M	P	X
	0.33	334	J	J	J	J	Q				K	K	M	X		M	M			X	X	X	X	M	P	X
	0.47	474	M	M	M	M	Q				K	K	P	X		M	M			X	X	X	X	M	P	X
	0.68	684	M	M	P	X	X				M	M	Q			M	P			X	X			M	P	X
	1.0	105	N	N	P	X	Z				M	M	X	Z		M	P			X	X			M	P	X
	1.5	155	N	N	Z	Z	Z				Z	Z	Z			M				X	X			M	X	Z
	2.2	225	X	X	Z	Z	Z				Z	Z	Z							X	X			M	X	Z
	3.3	335	X	X	Z	Z	Z				Z	Z	Z							X	Z					
	4.7	475	Z	Z	Z	Z					Z	Z								X	Z					
	10	106	Z	Z	Z	Z				Z										Z	Z					
	22	226	Z	Z	Z														Z							
	47	476	Z																							
	100	107																								
		WVDC	10	16	25	50	100	200	500	16	25	50	100	200	500	50	100	200	25	50	100	200	500	50	100	200
SIZE			1210							1812						1825			2220					2225		



Letter	A	B	C	E	G	J	K	M	N	P	Q	X	Y	Z
Max. Thickness	0.33 (0.013)	0.22 (0.009)	0.56 (0.022)	0.71 (0.028)	0.90 (0.035)	0.94 (0.037)	1.02 (0.040)	1.27 (0.050)	1.40 (0.055)	1.52 (0.060)	1.78 (0.070)	2.29 (0.090)	2.54 (0.100)	2.79 (0.110)
	PAPER						EMBOSSED							

NOTE: Contact factory for non-specified capacitance values

2.2.7. Servo



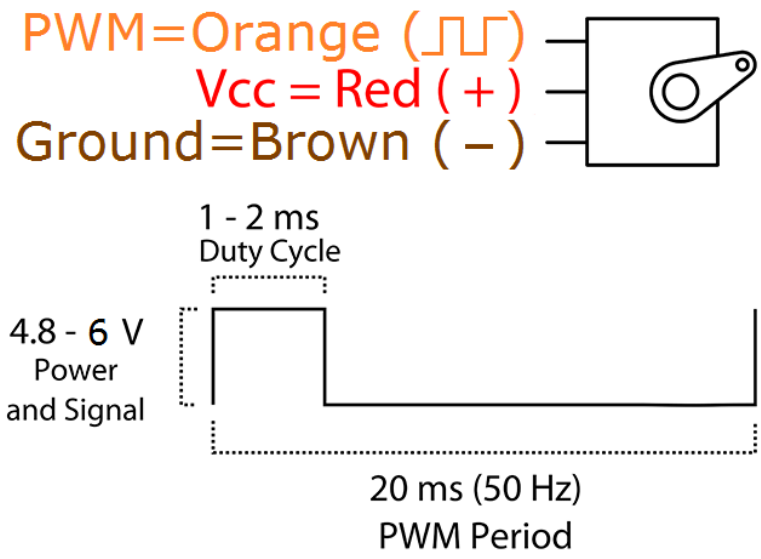
MG90S servo, Metal gear with one bearing

Tiny and lightweight with high output power, this tiny servo is perfect for RC Airplane, Helicopter, Quadcopter or Robot. This servo has *metal gears* for added strength and durability.

Servo can rotate approximately 180 degrees (90 in each direction), and works just like the standard kinds but *smaller*. You can use any servo code, hardware or library to control these servos. Good for beginners who want to make stuff move without building a motor controller with feedback & gear box, especially since it will fit in small places. It comes with a 3 horns (arms) and hardware.

Specifications

- Weight: 13.4 g
- Dimension: 22.5 x 12 x 35.5 mm approx.
- Stall torque: 1.8 kgf·cm (4.8V), 2.2 kgf·cm (6 V)
- Operating speed: 0.1 s/60 degree (4.8 V), 0.08 s/60 degree (6 V)
- Operating voltage: 4.8 V - 6.0 V
- Dead band width: 5 µs



Position "0" (1.5 ms pulse) is middle, "90" (~2 ms pulse) is all the way to the right, "-90" (~1 ms pulse) is all the way to the left.

2.2.8. Cámara

ArduCAM-M-5MP Camera Shield

5MP SPI Camera User Guide

Rev 1.1, Mar 2015

Table of Contents

1 Introduction

ArduCAM-M-5MP is optimized version of ArduCAM shield Rev.C, and is a high definition 5MP SPI camera, which reduce the complexity of the camera control interface. It integrates 5MP CMOS image sensor OV5642, and provides miniature size, as well as the easy to use hardware interface and open source code library. The ArduCAM mini can be used in any platforms like Arduino, Raspberry Pi, Maple, Chipkit, Beaglebone black, as long as they have SPI and I2C interface and can be well mated with standard Arduino boards. ArduCAM mini not only offers the capability to add a camera interface which doesn't have in some low cost microcontrollers, but also provides the capability to add multiple cameras to a single microcontroller.

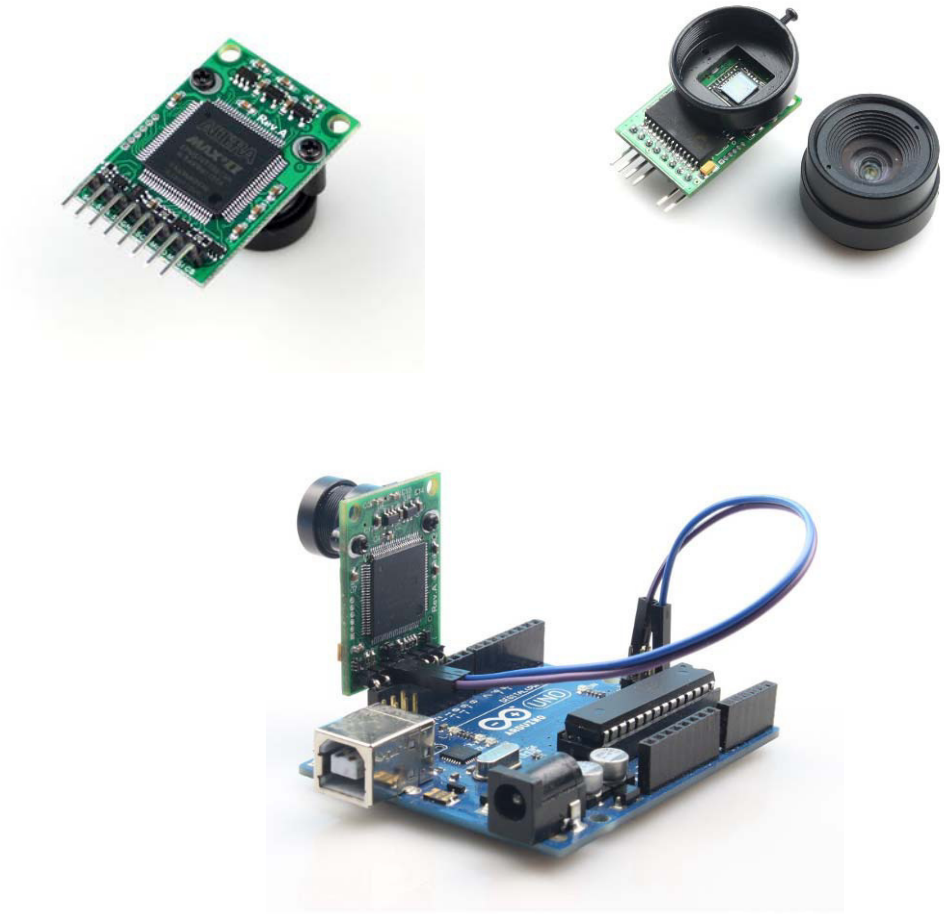


Figure 1 ArduCAM Mini Shield

2 Application

- IoT cameras
- Robot cameras
- Wildlife cameras
- Other battery-powered products
- Can be used in MCU, Raspberry Pi, ARM, DSP, FPGA platforms

3 Features

- 5MP image sensor OV5642
- M12 mount or CS mount lens holder with changeable lens options
- IR sensitive with proper lens combination
- I2C interface for the sensor configuration
- SPI interface for camera commands and data stream
- All IO ports are 5V/3.3V tolerant
- Support JPEG compression mode, single and multiple shoot mode, one time capture multiple read operation, burst read operation, low power mode and etc.
- Well mated with standard Arduino boards
- Provide open source code library for Arduino, STM32, Chipkit, Raspberry Pi, BeagleBone Black
- Small form of factor

4 Key Specifications

- Power supply
  Normal :5V/390mA
  Low power mode: 5V/20mA
- SPI speed: Max 8MHz
- Frame buffer: 512KB
- Size: 34 x 24 mm
- Weight: 20g
- Temperature: -10℃～+55℃
- Active array size: 2592x1944
- Shutter: rolling shutter
- Lens: 1/4 inch
- Resolution support:
  5MP, 1080p, 720p, VGA, QVGA
- Format support: RAW, YUV, RGB, JPEG
- Pixel Size: 1.4μm x 1.4μm

Note：OV5642 sensor consumes too much current when working in full power, onboard LDOs can be very hot due to the high voltage drop. Recommend to enter low power mode after capture, or use lower input power voltage.

5 Pin Definition

Table 1 ArduCAM-M-5MP Pin Definition

Pin No.	PIN NAME	TYPE	DESCRIPTION
1	CS	Input	SPI slave chip select input
2	MOSI	Input	SPI master output slave input
3	MISO	Output	SPI master input slave output
4	SCLK	Input	SPI serial clock
5	GND	Ground	Power ground
6	+5V	POWER	3.3V~5V Power supply
7	SDA	Bi-directional	Two-Wire Serial Interface Data I/O
8	SCL	Input	Two-Wire Serial Interface Clock

6 Block Diagram

Figure 2 shows the block diagram of ArduCAM mini shield which is composed by lens, image sensor and an ArduChip. The lens is changeable and can be mounted by S-mount (M12x0.5) or CS-mount lens holder. The image sensor is 5MP CMOS OV5642 from Omnivision. The ArduChip uses ArduCAM proprietary third generation camera controller technology which handles the complex camera, memory and user interface hardware timing and provides a user friendly SPI interface.

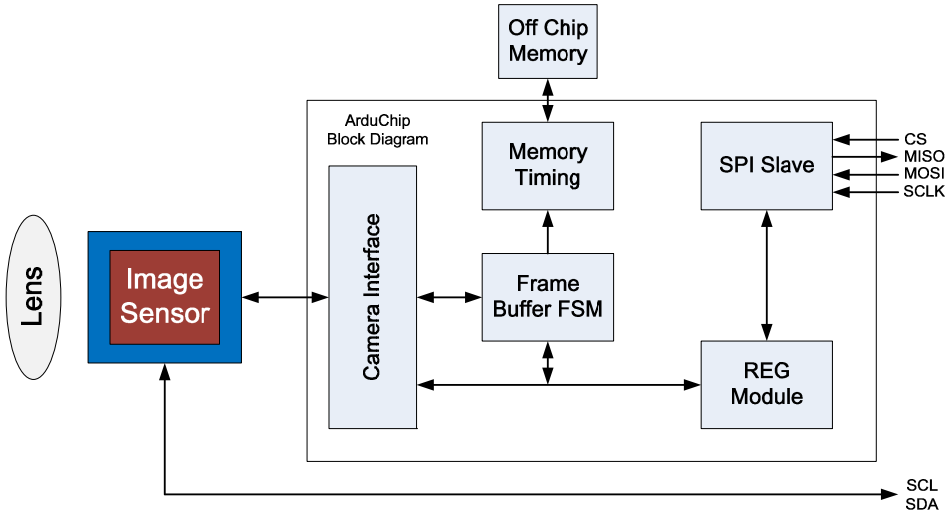


Figure 2 ArduCAM Mini Shield Block Diagram

7 Functions

7.1 Single Capture Mode

Single capture mode is the default capture mode of the camera. After issuing a capture command via SPI port, the ArduCAM will wait for a new frame and buffer the one entire image data to the frame buffer, and then assert the completion flag bit in the register. User only needs to poll the flag bit from the register to check out if the capture is done.

7.2 Multiple Capture Mode

Multiple capture mode is advanced capture mode. By setting the number of frames in the capture register, the ArduCAM will capture consequent frames after issuing capture command. Note that number of frames should be set properly and make sure do not exceed the maximum memory space.

7.3 JPEG Compression

The JPEG compression function is implemented in the image sensor. With proper register settings to the sensor, user can get different resolution with JPEG image stream output. It is recommended to use JPEG output to get higher resolution than RGB mode, due to the limitation of frame buffer.

7.4 Normal Read and Burst Read Operation

Normal read operation reads each image data by sending a read command in one SPI read operation cycle. While burst read operation only need to send a read command then read multiple image data in one SPI read operation cycle. It is recommended to use burst read operation to get better throughput performance.

7.5 Rewind Read Operation

Sometimes user wants to read the same frame of image data multiple times for processing, the rewind read operation is designed for this purpose. By resetting the read pointer to the beginning of the image data, user can read the same image data from the start point again.

7.6 Low Power Mode

Some battery power device need save power when in the idle status, the ArduCAM offers the low power mode to reduce power consumption, by shutdown the sensor and memory circuits.

7.7 Image Sensor Control

Image sensor control function is implemented in the image sensor. By setting proper set of register settings, user can control the exposure, white balance, brightness, contrast, color saturation and etc.

More technical information about ArduCAM mini shield, please read ArduCAM-M-5MP Hardware Application Note.pdf and ArduCAM-M-5MP Software Application Note.pdf for detail.

8 Lens Options

The ArduCAM-M-5MP camera shield is shipped with default LS-40136 (S mount) or LS-6018 (CS mount), lenses specification list as follows.

Please contact us admin@arducam.com for more lens options.

LS-40136 Lens Specification

A. Specification: **LS-40136**

1. sensor size: 1/4"
2. focal length(EFL): **3.2** mm
3. F/NO(infinition): **2.0**
4. back focal length: **1.6** mm

6. Field of view:
   Diagonal, **85°**;
   Horzongtal, **63.7°**;
   Vertical, **70°**;
7. Thread size: **M12*P0.5**
8. Element: **5E+IR**

B. Layout

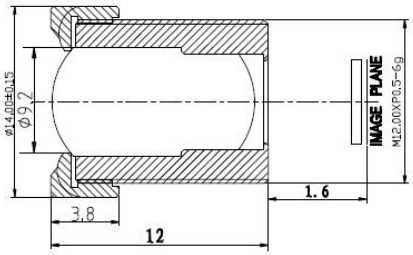


Figure 3 S Mount Lens Specification

LS-6018 Lens Specification

技 术 参 数

Technical parameters

型号 Model No.	LS-6018CS	视 场 角 Field of View	68°
焦距 Focal Length	6.0MM	外型尺寸 Dimensions	Φ28*24.2㎜
通光口径 Aperture(F)	1.4	近摄距离 M.O.D(m)	0.1
接口 Mount	CS	净 重 Weight(g)	29.0
靶面尺寸 Format	1/2.7"	备 注 Remarks	Metal

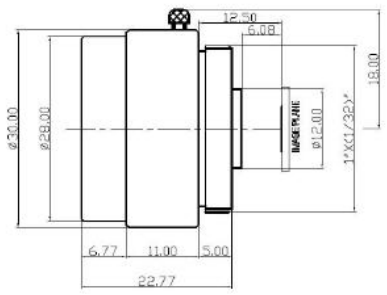
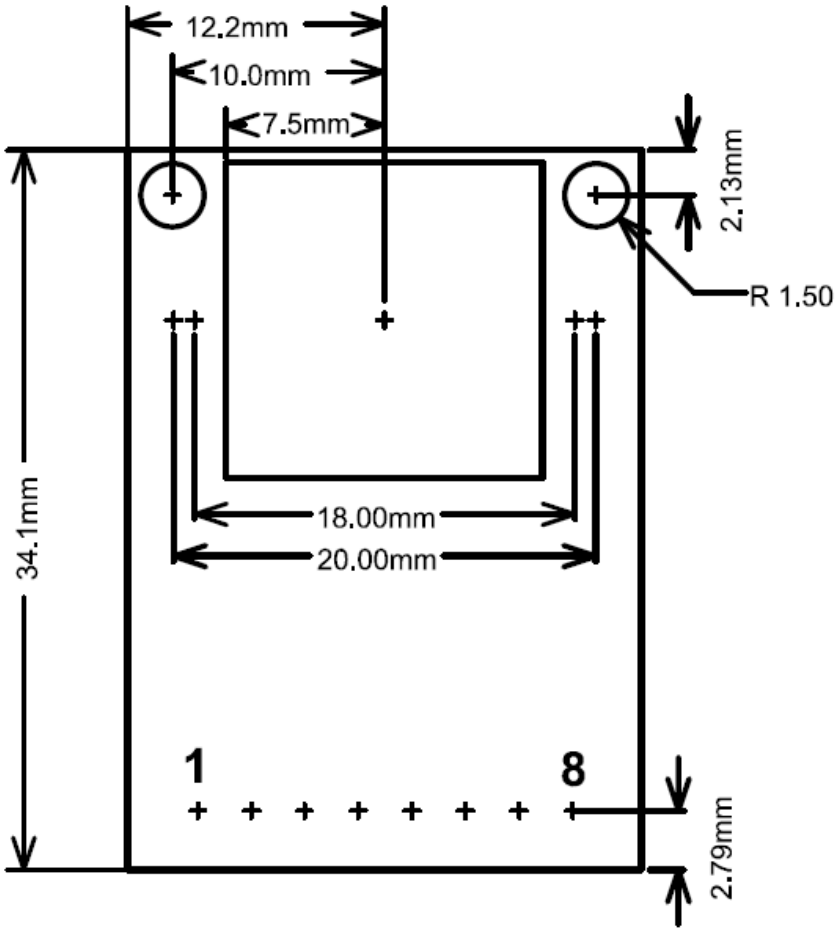


Figure 4 CS Mount Lens Specification

9 Mechanical Dimension



10 Order Information

Part Number	Description
ArduCAM-M-5MP-SM01	S Mount Preinstalled Pin Header
ArduCAM-M-5MP-SM02	S Mount Without Preinstalled Pin Header
ArduCAM-M-5MP-CSM01	CS Mount Preinstalled Pin Header
ArduCAM-M-5MP-CSM02	CS Mount Without Preinstalled Pin Header

2.2.9. Sensores Ultrasonidos

Ultrasonic Ranging Module HC - SR04

Product features:

Ultrasonic ranging module HC - SR04 provides 2cm - 400cm non-contact measurement function, the ranging accuracy can reach to 3mm. The modules includes ultrasonic transmitters, receiver and control circuit. The basic principle of work:
(1) Using IO trigger for at least 10us high level signal,
(2) The Module automatically sends eight 40 kHz and detect whether there is a pulse signal back.
(3) IF the signal back, through high level , time of high output IO duration is the time from sending ultrasonic to returning.
Test distance = (high level time×velocity of sound (340M/S) / 2,

Wire connecting direct as following:

- 5V Supply
- Trigger Pulse Input
- Echo Pulse Output
- 0V Ground

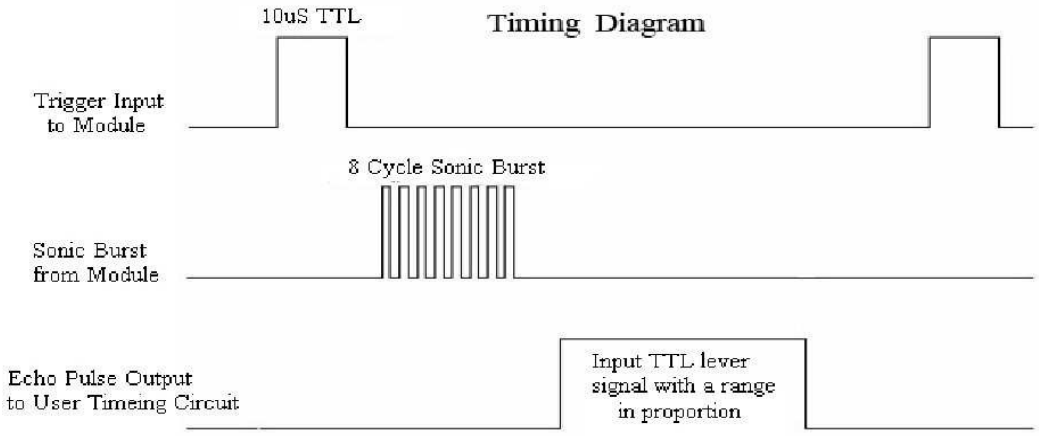
Electric Parameter

Working Voltage	**DC 5 V**
Working Current	**15mA**
Working Frequency	**40Hz**
Max Range	**4m**
Min Range	**2cm**
MeasuringAngle	**15 degree**
Trigger Input Signal	**10uS TTL pulse**
Echo Output Signal	**Input TTL lever signal and the range in proportion**
Dimension	**45*20*15mm**

Vcc Trig Echo GND

Timing diagram

The Timing diagram is shown below. You only need to supply a short 10uS pulse to the trigger input to start the ranging, and then the module will send out an 8 cycle burst of ultrasound at 40 kHz and raise its echo. The Echo is a distance object that is pulse width and the range in proportion .You can calculate the range through the time interval between sending trigger signal and receiving echo signal. Formula: uS / 58 = centimeters or uS / 148 =inch; or: the range = high level time * velocity (340M/S) / 2; we suggest to use over 60ms measurement cycle, in order to prevent trigger signal to the echo signal.



Attention:

- The module is not suggested to connect directly to electric, if connected electric, the GND terminal should be connected the module first, otherwise, it will affect the normal work of the module.
- When tested objects, the range of area is not less than 0.5 square meters and the plane requests as smooth as possible, otherwise ,it will affect the results of measuring.

www.Elecfreaks.com

2.2.10. Chip Cargador de batería

19-2099; Rev 0; 7/01

EVALUATION KIT AVAILABLE

MAXIM

Simple Current-Limited Switch-Mode Li+ Charger Controller

General Description

The low-cost MAX1873R/S/T provides all functions needed to simply and efficiently charge 2-, 3-, or 4-series lithium-ion cells at up to 4A or more. It provides a regulated charging current and voltage with less than ±0.75% total voltage error at the battery terminals. An external P-channel MOSFET operates in a step-down DC-DC configuration to efficiently charge batteries in low-cost designs.

The MAX1873R/S/T regulates the battery voltage and charging current using two control loops that work together to transition smoothly between voltage and current regulation. An additional control loop limits current drawn from the input source so that AC adapter size and cost can be minimized. An analog voltage output proportional to charging current is also supplied so that an ADC or microcontroller can monitor charging current.

The MAX1873 may also be used as an efficient current-limited source to charge NiCd or NiMH batteries in multichemistry charger designs. The MAX1873R/S/T is available in a space-saving 16-pin QSOP package. Use the evaluation kit (MAX1873EVKIT) to help reduce design time.

Applications

Notebook Computers

Portable Internet Tablets

2-, 3-, or 4-cell Li+ Battery Pack Chargers

6-, 9-, or 10-cell Ni Battery Pack Chargers

Hand-Held Instruments

Portable Desktop Assistants (PDAs)

Desktop Cradle Chargers

Selector Guide

PART	SERIES CELLS TO CHARGE
MAX1873REEE	2-Cell Li+ or 5- or 6-cell Ni Battery
MAX1873SEEE	3-Cell Li+ or 7- or 9-cell Ni Battery
MAX1873TEEE	4-Cell Li+ 10-cell Ni Battery Packs

Pin Configuration appears at end of data sheet.

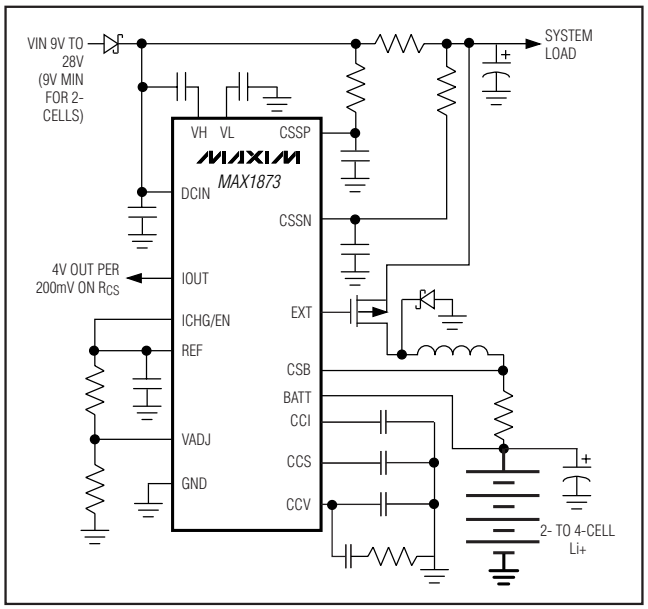
Features

- ♦ **Low-Cost and Simple Circuit**
- ♦ **Charges 2-, 3-, or 4-Series Lithium-Ion Cells**
- ♦ **AC Adapter Input-Current-Limit Loop**
- ♦ **Also Charges Ni-Based Batteries**
- ♦ **Analog Output Monitors Charge Current**
- ♦ **±0.75% Battery-Regulation Voltage**
- ♦ **5µA Shutdown Battery Current**
- ♦ **Input Voltage Up to 28V**
- ♦ **200mV Dropout Voltage/100% Duty Cycle**
- ♦ **Adjustable Charging Current**
- ♦ **300kHz PWM Oscillator Reduces Noise**
- ♦ **Space-Saving 16-Pin QSOP**
- ♦ **MAX1873 Evaluation Kit Available to Speed Designs**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1873REEE	-40°C to +85°C	16 QSOP
MAX1873SEEE	-40°C to +85°C	16 QSOP
MAX1873TEEE	-40°C to +85°C	16 QSOP

Typical Operating Circuit



Simple Current-Limited Switch-Mode Li+ Charger Controller

ABSOLUTE MAXIMUM RATINGS

CSSP, CSSN, DCIN to GND .....-0.3V to +30V
VL, ICHG/EN to GND.....-0.3V to +6V
VH, EXT to DCIN.....-6V to +0.3V
VH, EXT to GND .....(V_{DCIN} + 0.3V) to -0.3V
EXT to VH .....+6V to -0.3V
DCIN to VL.....+30V to -0.3V
VADJ, REF, CCI, CCV, CCS, IOUT to GND.....-0.3V to (VL + 0.3V)
BATT, CSB to GND.....-0.3V to +20V
CSSP to CSSN.....-0.3V to +0.6V
CSB to BATT.....-0.3V to +0.6V
VL Source Current .....+50mA
VH Sink Current .....+40mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C.....+667mW
Operating Temperature Range
MAX1873_EEE.....-40°C to +85°C
Junction Temperature..... +150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, $V_{ICHG/EN}$ = V_{REF}, V_{VADJ} = V_{REF}/2. MAX1873R: V_{BATT} = V_{CSB} = 8.4V; MAX1873S: V_{BATT} = V_{CSB} = 12.6V; MAX1873T: V_{BATT} = V_{CSB} = 16.8V; **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY AND REFERENCE					
DCIN Input Voltage Range		6		28	V
DCIN Quiescent Supply Current	6.0V < V_{DCIN} < 28V		4	7	mA
	DCIN ≤ BATT		0.1	10	µA
DCIN to BATT Undervoltage Threshold	CSSP = DCIN, input falling	0.05		0.175	V
DCIN to BATT Undervoltage Threshold	CSSP = DCIN, input rising	0.22		0.38	V
VL Output Voltage	6.0V < V_{DCIN} < 28V	5.15	5.40	5.65	V
VL Output Load Regulation	I_{VL} = 0 to 3mA		15	50	mV
REF Output Voltage	I_{REF} = 21µA (200kΩ load)	4.179	4.20	4.221	V
REF Line Regulation	6.0V < V_{DCIN} < 28V		2	6	mV
			22	65	ppm/V
REF Load Regulation	I_{REF} = 0 to 1mA		6	13	mV
SWITCHING REGULATOR					
PWM Oscillator Frequency		270	300	330	kHz
EXT Driver Source On-Resistance			4	7	Ω
EXT Driver Sink On-Resistance			2.5	4.5	Ω
VH Output Voltage	DCIN - VH, 6V < V_{DCIN} <28V, I_{VH} = 0 to 20mA	4.75		5.75	V
CSSN/CSSP Input Current	V_{CSSN}/V_{CSSP} = 28V, V_{DCIN} = 28V		70	200	µA
CSSN/CSSP Off-State Leakage	V_{DCIN} = V_{SSN}/V_{CSSP} = 18V, V_{BATT} = V_{CSB} = 18V		1.5	5	µA
BATT, CSB Input Current	ICHG/EN = 0 (charger disabled)		0.2	1	µA
	ICHG/EN = REF (charger enabled)		250	500	
BATT, CSB Input Current	DCIN ≤ BATT (input power removed)		1.5	5	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, $V_{ICHG/EN}$ = V_{REF}, V_{VADJ} = V_{REF}/2. MAX1873R: V_{BATT} = V_{CSB} = 8.4V; MAX1873S: V_{BATT} = V_{CSB} = 12.6V; MAX1873T: V_{BATT} = V_{CSB} = 16.8V; **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BATT Overvoltage Cutoff Threshold	2-cell version MAX1873R		10.45	11	11.55	V
	3-cell version MAX1873S		15.675	16.5	17.325	
	4-cell version MAX1873T (Note 1)		17.575	18.5	19.425	
Battery Regulation Voltage	MAX1873R (2 Li+ cells)	V_{VADJ} = 0	7.898	7.958	8.018	V
		V_{VADJ} = V_{REF}/2	8.337	8.4	8.463	
		V_{VADJ} = V_{REF} (Note 1)	8.775	8.842	8.909	
	MAX1873S (3 Li+ cells)	V_{VADJ} = 0	11.847	11.937	12.027	
		V_{VADJ} = V_{REF}/2	12.505	12.6	12.695	
		V_{VADJ} = V_{REF} (Note 1)	13.163	13.263	13.363	
	MAX1873T (4 Li+ cells)	V_{VADJ} = 0	15.796	15.916	16.036	
		V_{VADJ} = V_{REF}/2	16.674	16.8	16.926	
		V_{VADJ} = V_{REF} (Note 1)	17.551	17.684	17.817	
BATT Undervoltage Threshold	For I_{CHG}/20 trickle charge	MAX1873R	4.8	5.0	5.2	V
		MAX1873S	7.2	7.5	7.8	
		MAX1873T	9.6	10	10.4	
CURRENT SENSE						
CSB to BATT Battery Current-Sense Voltage	$V_{ICHG/EN}$ = V_{REF}		190	200	210	mV
	$V_{ICHG/EN}$ = V_{REF}/4		40	50	60	
CSB to BATT Current-Sense Voltage when V_{BATT} < 2.5V per Cell			5	10	15	mV
CSSP to CSSN Current-Sense Voltage	6V < V_{CSSP} < 28V		90	100	110	mV
CONTROL INPUTS/OUTPUTS						
ICHG/EN Input Threshold	Includes 50mV of hysteresis		500	600	700	mV
ICHG/EN Input Voltage Range For Charge Current Adjustment			700		V_{REF}	mV
VADJ Input Current	V_{VADJ} = V_{REF}/2		-100		100	nA
ICHG/EN Input Current	$V_{ICHG/EN}$ = V_{REF}		-100		100	nA
VADJ Input Voltage Range			0		V_{REF}	V
IOUT Voltage	Full scale	V_{CSB} - V_{BATT} = 200mV, 0 < I_{OUT} < 500µA	3.6	4.0	4.4	V
	25% scale	V_{CSB} - V_{BATT} = 50mV, 0 < I_{OUT} < 500µA	0.9	1.0	1.1	
	Trickle charge	V_{CSB} - V_{BATT} = 10mV	75	200	325	mV
	No charge current	V_{CSB} - V_{BATT} = 0, I_{IOUT} = sinking 20µA	40	70	90	

Simple Current-Limited Switch-Mode Li+ Charger Controller

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, $V_{ICHG/EN}$ = V_{REF}, V_{VADJ} = V_{REF}/2. MAX1873R: V_{BATT} = V_{CSB} = 8.4V; MAX1873S: V_{BATT} = V_{CSB} = 12.6V; MAX1873T: V_{BATT} = V_{CSB} = 16.8V; **T_A = -40°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	MAX	UNITS
INPUT SUPPLY AND REFERENCE					
DCIN Input Voltage Range			6	28	V
DCIN Quiescent Supply Current	6.0V < V_{DCIN} < 28V			7	mA
	DCIN ≤ BATT			10	µA
DCIN to BATT Undervoltage Threshold	CSSP = DCIN, input falling		0.05	0.2	V
DCIN to BATT Undervoltage Threshold	CSSP = DCIN, input rising		0.22	0.38	V
VL Output Voltage	6.0V < V_{DCIN} < 28V		5.15	5.65	V
VL Output Load Regulation	I_{VL} = 0 to 3mA			50	mV
REF Output Voltage	I_{REF} = 21µA (200kΩ load)		4.179	4.221	V
REF Line Regulation	6.0V < V_{DCIN} < 28V			6	mV
				65	ppm/V
REF Load Regulation	I_{REF} = 0 to 1mA			13	mV
SWITCHING REGULATOR					
PWM Oscillator Frequency			270	330	kHz
EXT Driver Source On-Resistance				7	Ω
EXT Driver Sink On-Resistance				4.5	Ω
VH Output Voltage	DCIN - VH, 6V < V_{DCIN} <28V, I_{VH} = 0 to 20mA		4.75	5.75	V
CSSN/CSSP Input Current	V_{CSSN}/V_{CSSP} = 28V, V_{DCIN} = 28V			200	µA
CSSN/CSSP Off-State Leakage	V_{DCIN} = V_{SSN}/V_{CSSP} = 18V V_{BATT} = V_{CSB} = 18V			5	µA
BATT, CSB Input Current	ICHG/EN = 0 (charger disabled)			1	µA
	ICHG/EN = REF (charger enabled)			500	
BATT, CSB Input Current	DCIN ≤ BATT (input power removed)			5	µA
BATT Overvoltage Cutoff Threshold	2-cell version MAX1873R		10.45	11.55	V
	3-cell version MAX1873S		15.675	17.325	
	4-cell version MAX1873T (Note 1)		17.575	19.425	
Battery Regulation Voltage	MAX1873R (2 Li+ cells)	V_{VADJ} = 0	7.898	8.018	V
		V_{VADJ} = V_{REF}/2	8.337	8.463	
		V_{VADJ} = V_{REF} (Note 1)	8.775	8.909	
	MAX1873S (3 Li+ cells)	V_{VADJ} = 0	11.847	12.027	
		V_{VADJ} = V_{REF}/2	12.505	12.695	
		V_{VADJ} = V_{REF} (Note 1)	13.163	13.363	
	MAX1873T (4 Li+ cells)	V_{VADJ} = 0	15.796	16.036	
		V_{VADJ} = V_{REF}/2	16.674	16.926	
		V_{VADJ} = V_{REF} (Note 1)	17.551	17.817	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, $V_{ICHG/EN}$ = V_{REF}, V_{VADJ} = V_{REF}/2. MAX1873R: V_{BATT} = V_{CSB} = 8.4V; MAX1873S: V_{BATT} = V_{CSB} = 12.6V; MAX1873T: V_{BATT} = V_{CSB} = 16.8V; **T_A = -40°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	MAX	UNITS
BATT Undervoltage Threshold	For I_{CHG}/20 trickle charge	MAX1873R	4.8	5.2	V
		MAX1873S	7.2	7.8	
		MAX1873T	9.6	10.4	
CURRENT SENSE					
CSB to BATT Battery Current-Sense Voltage	$V_{ICHG/EN}$ = V_{REF}		190	210	mV
	$V_{ICHG/EN}$ = V_{REF}/4		40	60	mV
CSB to BATT Current-Sense Voltage when V_{BATT} < 2.5V per Cell			5	15	mV
CSSP to CSSN Current-Sense Voltage	6V < V_{CSSP} < 28V		90	110	mV
CONTROL INPUTS/OUTPUTS					
ICHG/EN Input Threshold	Includes 50mV of hysteresis		500	700	mV
ICHG/EN Input Voltage Range for Charge Current Adjustment			700	V_{REF}	mV
VADJ Input Current	V_{VADJ} = V_{REF}/2		-100	100	nA
ICHG/EN Input Current	$V_{ICHG/EN}$ = V_{REF}		-100	100	nA
VADJ Input Voltage Range			0	V_{REF}	V
IOUT Voltage	Full scale	V_{CSB} - V_{BATT} = 200mV, 0 < I_{OUT} < 500µA	3.6	4.4	V
	25% scale	V_{CSB} - V_{BATT} = 50mV, 0 < I_{OUT} < 500µA	0.9	1.1	
	Trickle charge	V_{CSB} - V_{BATT} = 10mV	75	325	mV
	No charge current	V_{CSB} - V_{BATT} = 0, I_{IOUT} = sinking 20µA	40	90	

Note 1: While it may appear possible to set the Battery Regulation Voltage higher than the Battery Overvoltage Cutoff Threshold, this cannot happen because both parameters are derived from the same reference and track each other.

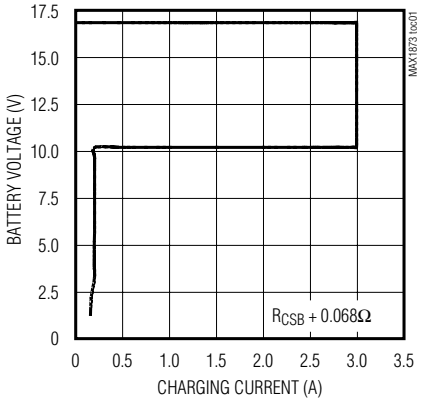
Note 2: Specifications to -40°C are guaranteed by design, not production tested.

Simple Current-Limited Switch-Mode Li+ Charger Controller

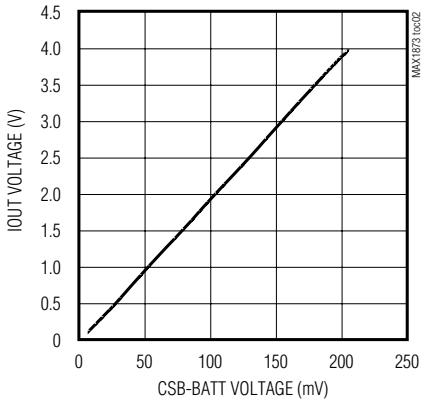
Typical Operating Characteristics

(Circuit of Figure 1, V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, $V_{ICHG/EN}$ = V_{REF}, V_{VADJ} = V_{REF}/2. MAX1873R: V_{BATT} = V_{CSB} = 8.4V; MAX1873S: V_{BATT} = V_{CSB} = 12.6V; MAX1873T: V_{BATT} = V_{CSB} = 16.8V; T_A = +25°C, unless otherwise noted).

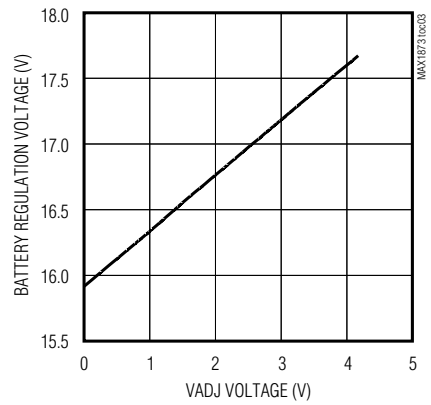
MAX1873T (4-CELL)
BATTERY VOLTAGE vs. CHARGING CURRENT



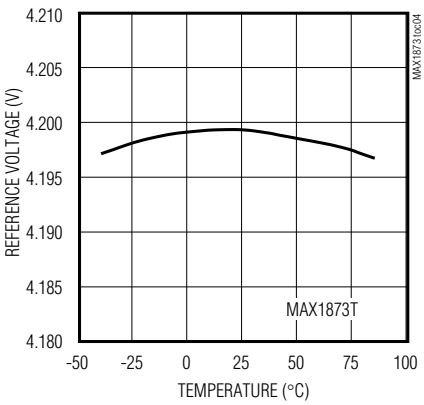
IOUT VOLTAGE
vs. CSB-BATT VOLTAGE



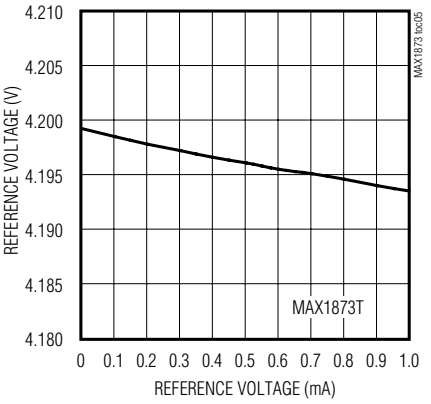
MAX1873T (4-CELL)
BATTERY REGULATION VOLTAGE
vs. VADJ VOLTAGE



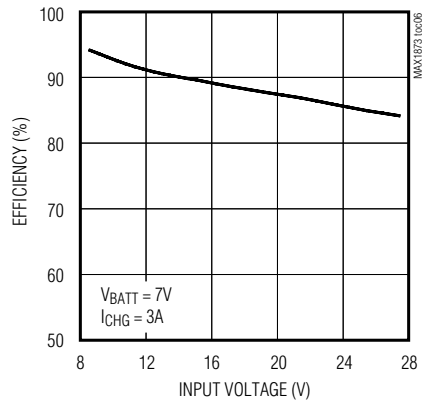
RECENT VOLTAGE vs. TEMPERATURE



RECENT VOLTAGE
vs. REFERENCE CURRENT



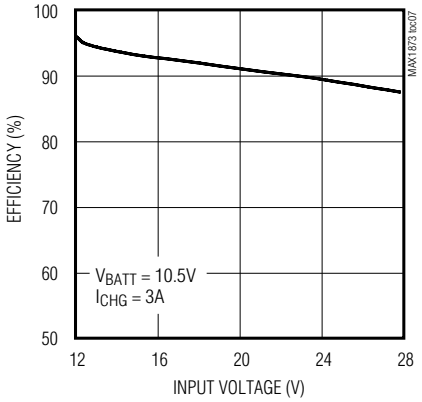
MAX1873R (2-CELL)
EFFICIENCY vs. INPUT VOLTAGE



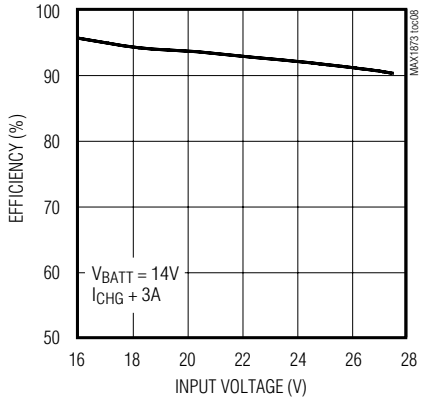
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{DCIN} = V_{CSSP} = V_{CSSN} = 18V, $V_{ICHG/EN}$ = V_{REF}, V_{VADJ} = V_{REF}/2. MAX1873R: V_{BATT} = V_{CSB} = 8.4V; MAX1873S: V_{BATT} = V_{CSB} = 12.6V; MAX1873T: V_{BATT} = V_{CSB} = 16.8V; T_A = +25°C, unless otherwise noted).

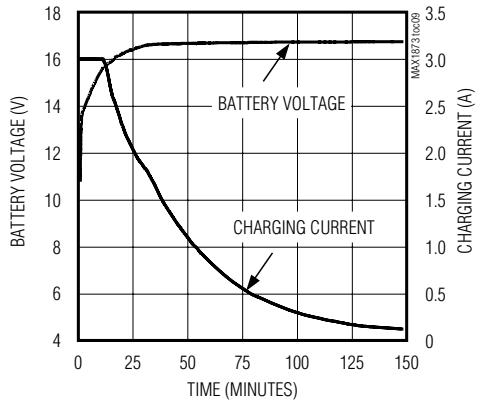
**MAX1873S (3-CELL)
EFFICIENCY vs. INPUT VOLTAGE**



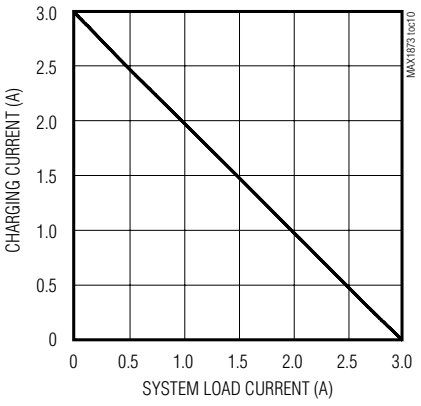
**MAX1873T (4-CELL)
EFFICIENCY vs. INPUT VOLTAGE**



**4-CELL BATTERY VOLTAGE AND
CHARGING CURRENT vs. TIME**



**CHARGING CURRENT
vs. SYSTEM LOAD CURRENT**



Simple Current-Limited Switch-Mode Li+ Charger Controller

Pin Description

PIN	NAME	FUNCTION
1	CSSN	Source Current-Sense Negative Input. Connect a current-sense resistor between CSSP and CSSN to limit total current drawn from the input source. To disable input current sensing, connect CSSN to CSSP.
2	CSSP	Source Current-Sense Positive Input. Also used for input source undervoltage sensing.
3	CCS	Input-Source-Current Regulation Loop Compensation Point
4	CCV	Battery Regulation Voltage Control-Loop Compensation Point. Pulling CCV high (to VL) through a 1.5kΩ resistor disables the voltage control loop for charging NiCd or NiMH batteries.
5	CCI	Battery Charge Current Control-Loop Compensation Point
6	ICHG/EN	Battery Charging Current Adjust/Shutdown Input. This pin can be connected to a resistive-divider between REF and GND to adjust the charge current sense threshold between CSB and BATT. When ICHG/EN is connected to REF, the CSB-BATT threshold is 200mV. Pull ICHG/EN low (below 500mV) to disable charging and reduce the supply current to 5µA.
7	IOUT	Charge Current Monitor Output. Analog Voltage Output that is proportional to charging current. V_{IOUT} = 20 (V_{CSB} - V_{BATT}) or 4V for a 200mV current-sense voltage (maximum load capacitance = 5nF).
8	VADJ	Battery Regulation Voltage Adjust. Set the battery regulation voltage from 3.979V per cell to 4.421V per cell with 1% resistors. Output accuracy remains better than 0.75% even with 1% adjusting resistors due to reduced adjustment range. For 4.2V, the voltage-divider resistors must be equal value (nominally 100kΩ each).
9	REF	4.2V Reference Voltage Output. Bypass to GND with a 1µF ceramic capacitor.
10	BATT	Battery Voltage-Sense Input and Battery Current-Sense Negative Input. Bypass to GND with a 68µF for MAX1873R, 47µF for MAX1873S, and 33µF for MAX1873T. Use capacitors with ESR < 1Ω.
11	CSB	Battery Current-Sense Positive Input
12	GND	Ground
13	VH	Internal VH Regulator. VH internally supplies power to the EXT driver. Connect a 0.22µF ceramic capacitor between VH and DCIN.
14	EXT	Drive Output for External PFET. EXT swings from V_{DCIN} to V_{DCIN} - 5V.
15	DCIN	Power-Supply Input. DCIN is the input supply for charger IC. Bypass to GND with a 0.22µF ceramic capacitor.
16	VL	Internal VL Regulator. VL powers the MAX1873's control logic at 5.4V. Bypass to GND with a 2.2µF or larger ceramic capacitor.

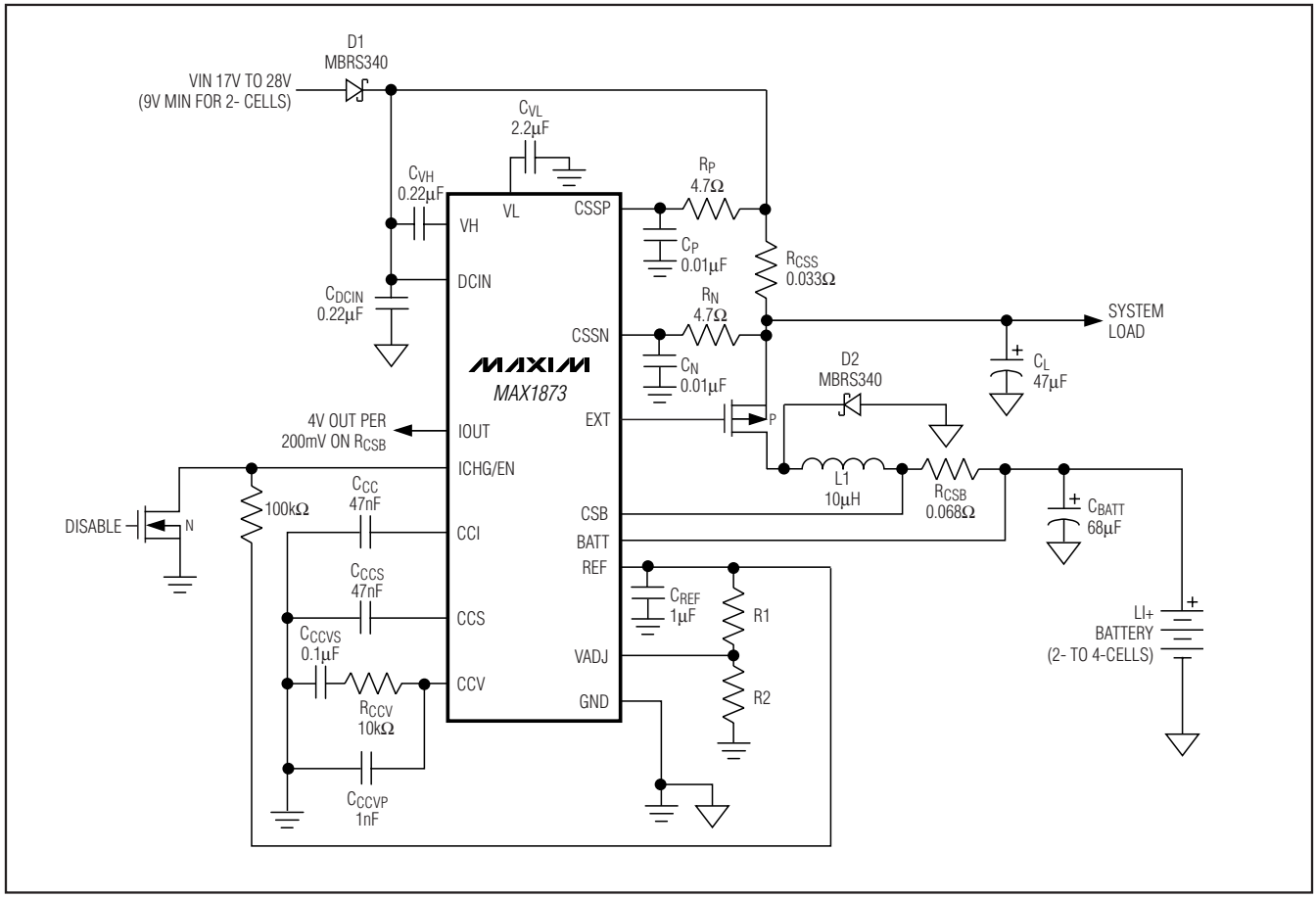


Figure 1. Typical Application Circuit

Detailed Description

The MAX1873 includes all of the functions necessary to charge 2-, 3-, or 4-series cell lithium-ion (Li+) battery packs. It includes a high-efficiency step-down DC-DC converter that controls charging voltage and current. It also features input source current limiting so that an AC adapter that supplies less than the total system current in addition to charging current can be used without fear of overload.

The DC-DC converter uses an external P-channel MOSFET switch, inductor, and diode to convert the input voltage to charging current or charging voltage. The typical application circuit is shown in Figure 1. Charging current is set by R_{CSB}, while the battery voltage is measured at BATT. The battery regulation voltage limit is nominally set to 8.4V for the R version (2-cells), 12.6V for the S version (3-cells), and 16.8V for the T version (4-cells), but it can also be adjusted to other voltages for different Li+ chemistries.

Voltage Regulator

Li+ batteries require a high-accuracy voltage limit while charging. The battery regulation voltage is nominally set to 4.2V per cell and can be adjusted ±5.25% by setting the voltage at VADJ between REF and ground. By limiting the adjust range of the regulation voltage, an overall voltage accuracy of better than ±0.75% is maintained while using 1% resistors.

An internal error amplifier maintains voltage regulation to within ±0.75%. The amplifier is compensated at CCV (see Figure 1). Individual compensation of the voltage regulation and current regulation loops allows for optimal compensation of each. A typical CCV compensation network is shown in Figure 1 and will suffice for most designs.

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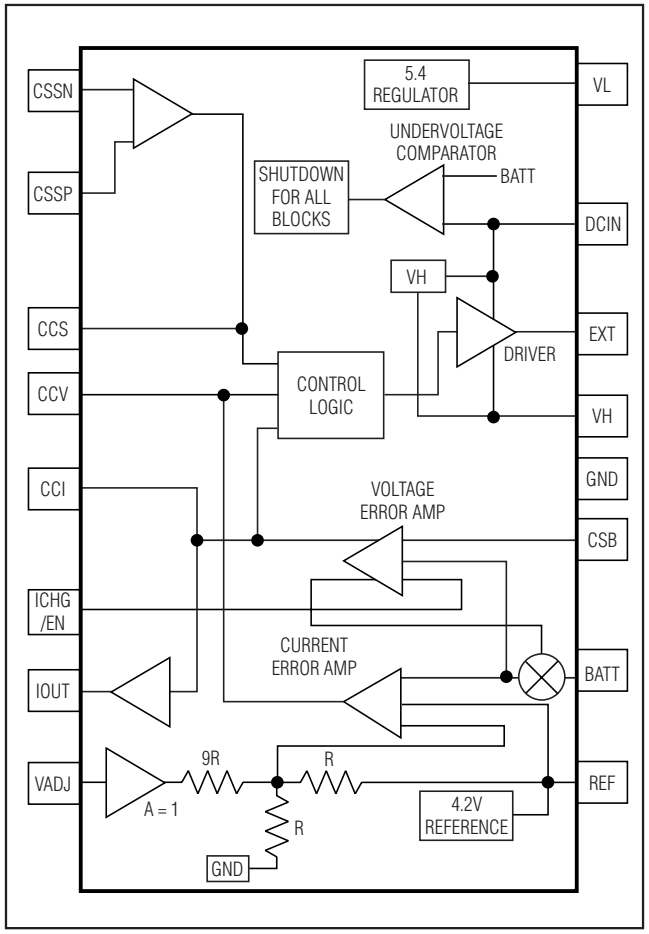

Figure 2. Functional Block Diagram

Charging-Current Regulator

The charging-current regulator limits the battery charging current. Current is sensed by the current-sense resistor (R_{CSB} in Figure 1) connected between BATT and CSB. The voltage on ICHG/EN can also adjust the charging current. Full-scale charging current (I_{CHG} = 0.2V / RCSB) is achieved by connecting ICHG/EN to REF. See *Setting the Charging-Current Limit* section for more details.

The charging-current error amplifier is compensated at CCI (Figure 1). A 47nF capacitor from CCI to GND provides suitable performance for most applications.

Input-Current Regulator

The input-current regulator limits the source current by reducing charging current when the input current reaches the set input-current limit. In a typical portable design, system load current will normally fluctuate as portions of the system are powered up or put to sleep. Without the benefit of input-current regulation, the input source would have to be able to supply the maximum system current plus the maximum charger-input current. The MAX1873 input-current loop ensures that the system always gets adequate power by reducing charging current as needed. By using the input-current limiter, the size and cost of the AC adapter can be reduced. See *Setting the Input-Current Limit* section for design details.

Input current is measured through an external sense resistor, R_{CSS}, between CSSP and CSSN. The input-current limit feature may be bypassed by connecting CSSP to CSSN.

The input-current error amplifier is compensated at CCS. A 47nF capacitor from CCS to GND provides suitable performance for most applications.

PWM Controller

The pulse-width modulation (PWM) controller drives the external MOSFET at a constant 300kHz to regulate the charging current and voltage while maintaining low noise. The controller accepts inputs from the CCI, CCV, and CCS error amplifiers. The lowest signal of these three drives the PWM controller. An internal clamp limits the noncontrolling signals to within 200mV of the controlling signal to prevent delay when switching between the battery-voltage control, charging-current control, and input-current regulation loops.

Shutdown

The MAX1873 stops charging when ICHG/EN is pulled low (below 0.5V) and shuts down when the voltage at DCIN falls below the voltage at BATT. In shutdown, the internal resistive voltage-divider is disconnected from BATT to reduce the battery drain. When AC-adapter power is removed, or when the part is shut down, the MAX1873 typically draws 1.5µA from the battery.

Source Undervoltage Shutdown (Dropout)

The DCIN voltage is compared to the voltage at BATT. When the voltage at DCIN drops below BATT + 50mV, the charger turns off, preventing drain on the battery when the input source is not present or is below the battery voltage.

A diode is typically connected between the input source and the charger input. This diode prevents the battery from discharging through the body diode of the high-side MOSFET should the input be shorted to GND. It also protects the charger, battery, and systems from reversed polarity adapters and negative input voltages.

Charge-Current Monitor Output

IOUT is an analog voltage output that is proportional to the actual charge current. With the aid of a microcontroller, the IOUT signal can facilitate gas-gauging, indicate percent of charge, or charge-time remaining. The equation governing this output is:

$$V_{IOUT} = 20(V_{CSB} - V_{BATT}) \text{ or}$$
$$V_{OUT} = 20(R_{CSB} \times I_{CHG})$$

where V_{CSB} and V_{BATT} are the voltages at the CSB and BATT pins, and ICHG is the charging current. IOUT can drive a load capacitance of 5nF.

Design Procedure

Setting the Battery-Regulation Voltage

For Li+ batteries, VADJ sets the per-cell battery-regulation voltage limit. To set the VADJ voltage, use a resistive-divider from REF to GND (Figure 1). For a battery voltage of 4.2V per cell, use resistors of equal value (100kΩ each) in the VADJ voltage-divider. To set other battery-regulation voltages, see the remainder of this section.

The per-cell battery regulation voltage is a function of Li+ battery chemistry and construction and is usually clearly specified by the manufacturer. If this is not clearly specified, be sure to consult the battery manufacturer to determine this voltage before charging any Li+ battery. Once the per-cell voltage is determined, the VADJ voltage is calculated by the equation:

$$V_{VADJ} = \left[9.5(V_{BATTR})/N\right] - (9V_{REF})$$

where V_{BATTR} is the desired battery-regulation voltage (for the total series-cell stack), N is the number of Li+ battery cells, and V_{REF} is the reference voltage (4.2V).

Set V_{VADJ} by choosing R1. R1 should be selected so that the total divider resistance (R1+ R2) is near 200kΩ. R2 can then be calculated as follows:

$$R2 = \left[V_{VADJ}/(V_{REF} - V_{VADJ})\right] \times R1$$

Since the full range of VADJ (from 0 to VREF) results in a ±5.263% adjustment of the battery-regulation limit (3.979V to 4.421V), the resistive-divider's accuracy need not be as tight as the output-voltage accuracy. Using 1% resistors for the voltage-divider still provides ±0.75% battery-voltage-regulation accuracy.

Setting the Charging-Current Limit

The charging current ICHG is sensed by the current-sense resistor R_{CSB} between CSB and BATT, and is also adjusted by the voltage at ICHG/EN. If ICHG/EN is connected to REF (the standard connection), the charge current is given by:

$$I_{CHG} = 0.2V/R_{CSB}$$

In some cases, common values for R_{CSB} may not allow the desired charge-current value. It may also be desirable to reduce the 0.2V CSB-to-BATT sense threshold to reduce power dissipation. In such cases, the ICHG/EN input may be used to reduce the charge-current-sense threshold. In those cases the equation for charge current becomes:

$$I_{CHG} = 0.2V(V_{ICH/EN}/V_{REF})/R_{CSB}$$

Setting the Input-Current Limit

The input-source current limit, I_{IN}, is set by the input-current sense resistor, R_{CSS}, (Figure 1) connected between CSSP and CSSN. The equation for the source current is:

$$I_{IN} = 0.1V/R_{CSS}$$

This limit is typically set to the current rating of the input power source or AC adapter to protect the input source from overload. Short CSSP and CSSN to DCIN if the input-source current-limit feature is not used.

Inductor Selection

The inductor value may be selected for more or less ripple current. The greater the inductance, the lower the ripple current. However, as the physical size is kept the same, larger inductance value typically results in higher inductor series resistance and lower inductor saturation current. Typically, a good tradeoff is to choose the inductor such that the ripple current is approximately 30% to 50% of the DC average charging current. The ratio of ripple current to DC charging current (LIR) can be used to calculate the inductor value:

$$L = \left\{V_{BATT}\left[V_{DCIN(MAX)} - V_{BATT}\right]\right\} / \left[V_{DCIN(MAX)} \times f_{SW} \times I_{CHG} \times LIR\right]$$

where f_{SW} is the switching frequency (nominally 300kHz) and I_{CHG} is the charging current. The peak inductor current is given by:

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$$I_{PEAK} = I_{CHG}(1+LIR/2)$$

For example, for a 4-cell charging current of 3A, a $V_{DCIN(MAX)}$ of 24V, and an LIR of 0.5, L is calculated to be 11.2µH with a peak current of 3.75A. Therefore a 10µH inductor would be satisfactory.

MOSFET Selection

The MAX1873 uses a P-channel power MOSFET switch. The MOSFET must be selected to meet the efficiency or power dissipation requirements of the charging circuit as well as the maximum temperature of the MOSFET. Characteristics that affect MOSFET power dissipation are drain-source on-resistance ($R_{DS(ON)}$) and gate charge. Generally these are inversely proportional.

To determine MOSFET power dissipation, the operating duty cycle must first be calculated. When the charger is operating at higher currents, the inductor current will be continuous (the inductor current will not drop to 0). In this case, the high-side MOSFET duty cycle (D) can be approximated by the equation:

$$D \approx \frac{V_{BATT}}{V_{DCIN}}$$

And the catch-diode duty cycle (D') will be 1 - D or:

$$D' \approx \frac{V_{DCIN} - V_{BATT}}{V_{DCIN}}$$

where V_{BATT} is the battery-regulation voltage (typically 4.2V per cell) and V_{DCIN} is the source-input voltage.

For MOSFETs, the worst-case power dissipation due to on-resistance (P_R) occurs at the maximum duty cycle, where the operating conditions are minimum source-voltage and maximum battery voltage. P_R can be approximated by the equation:

$$P_R = \frac{V_{BATT(MAX)}}{V_{DCIN(MIN)}} \times R_{DS(ON)} \times I_{CHG}^2$$

Transition losses (P_T) can be approximated by the equation:

$$P_T = \frac{V_{DCIN} \times I_{CHG} \times f_{SW} \times t_{TR}}{3}$$

where t_{TR} is the MOSFET transition time and f_{SW} is the switching frequency. The total power dissipation of the MOSFET is then:

$$P_{TOT} = P_R + P_T$$

Diode Selection

A Schottky rectifier with a current rating of at least the charge current limit must be connected from the MOSFET drain to GND. The voltage rating of the diode must exceed the maximum expected input voltage.

Capacitor Selection

The input capacitor shunts the switching current from the charger input and prevents that current from circulating through the source, typically an AC wall cube. Thus the input capacitor must be able to handle the input RMS current. At high charging currents, the converter will typically operate in continuous conduction. In this case, the RMS current of the input capacitor can be approximated with the equation:

$$I_{CIN} \approx I_{CHG}\sqrt{D - D^2}$$

where I_{CIN} is the input capacitor RMS current, D is the PWM converter duty cycle (typically V_{BATT}/V_{DCIN}), and I_{CHG} is the battery-charging current.

The maximum RMS input current occurs at 50% duty cycle, so the worst-case input-ripple current is 0.5 x I_{CHG}. If the input-to-output voltage ratio is such that the PWM controller will never work at 50% duty cycle, then the worst-case capacitor current will occur where the duty cycle is nearest 50%.

The impedance of the input capacitor is critical to preventing AC currents from flowing back into the wall cube. This requirement varies depending on the wall cube's impedance and the requirements of any conducted or radiated EMI specifications that must be met. Low ESR aluminum electrolytic capacitors may be used, however, tantalum or high-value ceramic capacitors generally provide better performance.

The output filter capacitor absorbs the inductor-ripple current. The output-capacitor impedance must be significantly less than that of the battery to ensure that it will absorb the ripple current. Both the capacitance and the ESR rating of the capacitor are important for its effectiveness as a filter and to ensure stability of the PWM circuit. The minimum output capacitance for stability is:

$$C_{OUT} > \frac{V_{REF}\left(1 + \frac{V_{BATT}}{V_{DCIN(MIN)}}\right)}{V_{BATT} \times f_{SW} \times R_{CSB}}$$

where C_{OUT} is the total output capacitance, V_{REF} is the reference voltage (4.2V), V_{BATT} is the maximum battery regulation voltage (typically 4.2V per cell), $V_{DCIN\ (MIN)}$ is the minimum source-input voltage, and R_{CSB} is the current-sense resistor (68mΩ for 3A charging current) from CSB to BATT.

The maximum output capacitor ESR allowed for stability is:

$$R_{ESR} < \frac{R_{CSB} \times V_{BATT}}{V_{REF}}$$

where R_{ESR} is the output capacitor ESR.

Compensation Components

The three regulation loops: input current limit, charging current limit, and charging voltage limit are compensated separately using the CCS, CCI, and CCV pins, respectively.

The charge-current loop error-amplifier output is brought out at CCI. Likewise, the source-current error-amplifier output is brought out at CCS. 47nF capacitors to ground at CCI and CCS compensate the current loops in most charger designs. Raising the value of these capacitors reduces the bandwidth of these loops.

The voltage-regulating loop error-amplifier output is brought out at CCV. Compensate this loop by connecting a capacitor in parallel with a series resistor-capacitor from CCV to GND. Recommended values are shown in Figure 1.

Applications Information

VL, VH, and REF Bypassing

The MAX1873 uses two internal linear regulators to power internal circuitry. The outputs of the linear regulators are at VL and VH. VL powers the internal control circuitry while VH powers the MOSFET gate driver. VL may also power a limited amount of external circuitry, as long as its maximum current (3mA) is not exceeded.

A 2.2µF bypass capacitor is required from VL to GND to ensure stability. A 0.22µF capacitor is required from VH to DCIN. A 1µF bypass capacitor is required between REF and GND to ensure that the internal 4.2V reference is stable. In all cases, use low-ESR ceramic capacitors.

Charging NiMH and NiCd Cells

The MAX1873 may be used in multichemistry chargers. When charging NiMH or NiCd cells, pull CCV high (to VL) with a 1.5 kΩ resistor. This disables the voltage control loop so the Li+ battery-regulation voltage settings do not interfere with charging. However, the battery undervoltage-protection features remain active so charging current is reduced when V_{BATT} is less than the levels stated in the BATT Undervoltage Threshold line in the *Electrical Characteristics Table.* 5- or 6-series Ni cells may be charged with the R version device, 7- to 9-cells with the S version, and 10-cells with the T version.

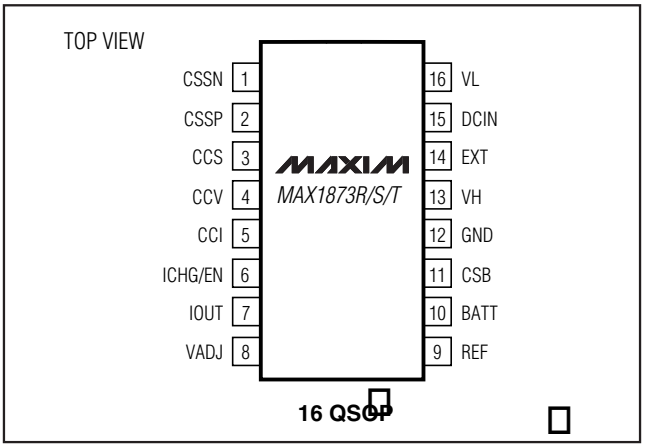
The MAX1873 contains no charge-termination algorithms for Ni cells; it acts only as a current source. A separate microcontroller or Ni-cell charge controller must instruct the MAX1873 to terminate charging.

Chip Information

PROCESS: BiCMOS

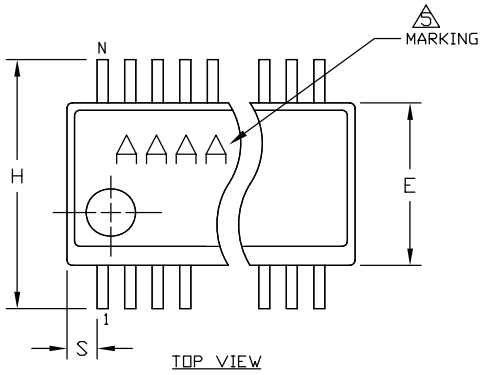
TRANSISTOR COUNT: 1397

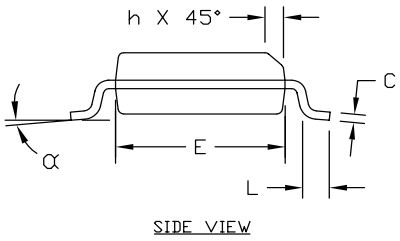
Pin Configuration



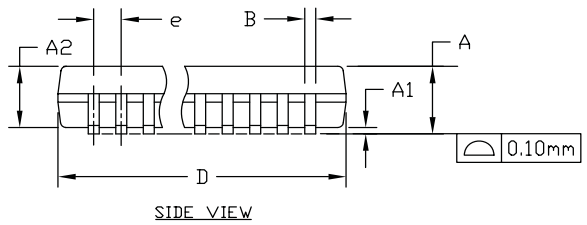
Simple Current-Limited Switch-Mode Li+ Charger Controller

Package Information





	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.053	.069	1.35	1.75
A1	.004	.010	.102	.254
A2	.049	.065	1.245	1.651
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	PKG CODES
D	.189	.196	4.80	4.98	16	E16-1, E16M-1, E16-4, E16-5, E16-8F
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	E20-1, E20-2, E20-3
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	E24-1, E24-2, E24-3
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	E28-1, E28M-1, E28-2
S	.0250	.0300	0.635	0.762		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. CONTROLLING DIMENSIONS: INCHES.
4. MEETS JEDEC MO137.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

—DRAWING NOT TO SCALE—

maxim integrated

TITLE:
PACKAGE OUTLINE
QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	J	1/1

2.2.11. Fuente Conmutada

17V, 1A Synchronous Step-Down Regulator with 3.5µA Quiescent Current

FEATURES

- **Wide V_{IN} Range: 2.7V to 17V**
- **Wide V_{OUT} Range: 0.6V to V_{IN}**
- **95% Max Efficiency**
- **Low I_Q < 3.5µA, Zero-Current Shutdown**
- **Constant Frequency (1MHz/2.25MHz)**
- Full Dropout Operation with Low I_Q
- 1A Rated Output Current
- ±1% Output Voltage Accuracy
- Current Mode Operation for Excellent Line and Load Transient Response
- Synchronizable to External Clock
- Pulse-Skipping, Forced Continuous, Burst Mode® Operation
- Internal Compensation and Soft-Start
- Overtemperature Protection
- Compact 6-Lead DFN (2mm × 3mm) Package or Thermally-Enhanced MS8E Package with Power Good Output and Independent SGND Pin

APPLICATIONS

- Portable-Handheld Scanners
- Industrial and Embedded Computing
- Automotive Applications
- Emergency Radio

DESCRIPTION

The LTC®3621/LTC3621-2 is a high efficiency 17V, 1A synchronous monolithic step-down regulator. The switching frequency is fixed to 1MHz or 2.25MHz with a ±40% synchronizing range. The regulator features ultralow quiescent current and high efficiencies over a wide V_{OUT} range.

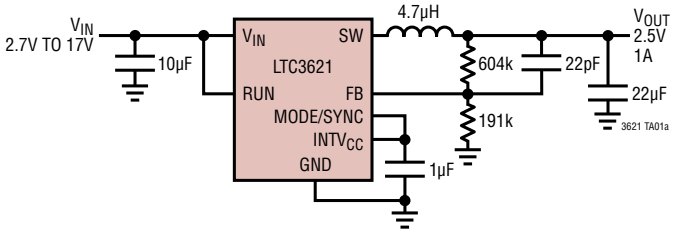
The step-down regulator operates from an input voltage range of 2.7V to 17V and provides an adjustable output range from 0.6V to V_{IN} while delivering up to 1A of output current. A user-selectable mode input is provided to allow the user to trade off ripple noise for light load efficiency; Burst Mode operation provides the highest efficiency at light loads, while pulse-skipping mode provides the lowest voltage ripple. The MODE pin can also be used to allow the user to sync the switching frequency to an external clock.

LTC3621 Options

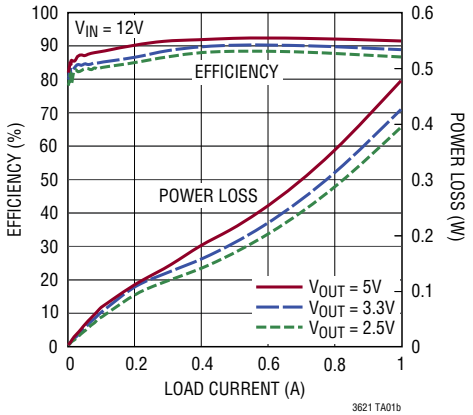
PART NAME	FREQUENCY	V_{OUT}
LTC3621	1.00MHz	Adjustable
LTC3621-3.3	1.00MHz	3.3V
LTC3621-5	1.00MHz	5V
LTC3621-2	2.25MHz	Adjustable
LTC3621-23.3	2.25MHz	3.3V
LTC3621-25	2.25MHz	5V

TYPICAL APPLICATION

2.5V V_{OUT} with 400mA Burst Clamp, f_{SW} = 1MHz



Efficiency and Power Loss vs Load at 1MHz

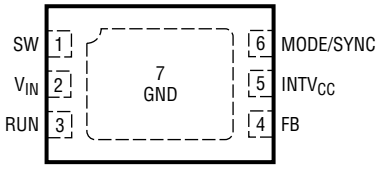


ABSOLUTE MAXIMUM RATINGS (Note 1)

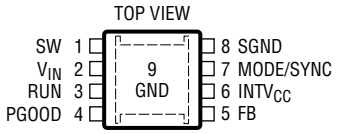
V_{IN} Voltage ..... 17V to –0.3V
RUN Voltage ..... V_{IN} to –0.3V
MODE/SYNC, FB Voltages ..... 6V to –0.3V
PGOOD Voltages ..... 6V to –0.3V

Operating Junction Temperature Range (Notes 3, 6, 7)
LTC3621E, LTC3621I ..... –40°C to 125°C
LTC3621H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DCB PACKAGE
6-LEAD (2mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 64°C/W, θ_{JC} = 9.6°C/W
EXPOSED PAD (PIN 7) IS GND, MUST BE SOLDERED TO PCB



MS8E PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3621EDCB#PBF	LTC3621EDCB#TRPBF	LGDG	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3621IDCB#PBF	LTC3621IDCB#TRPBF	LGDG	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3621EDCB-3.3#PBF	LTC3621EDCB-3.3#TRPBF	LGQF	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3621IDCB-3.3#PBF	LTC3621IDCB-3.3#TRPBF	LGQF	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3621EDCB-5#PBF	LTC3621EDCB-5#TRPBF	LGQC	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3621IDCB-5#PBF	LTC3621IDCB-5#TRPBF	LGQC	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3621EMS8E#PBF	LTC3621EMS8E#TRPBF	LTGDH	8-Lead Plastic MSOP	–40°C to 125°C
LTC3621IMS8E#PBF	LTC3621IMS8E#TRPBF	LTGDH	8-Lead Plastic MSOP	–40°C to 125°C
LTC3621HMS8E#PBF	LTC3621HMS8E#TRPBF	LTGDH	8-Lead Plastic MSOP	–40°C to 150°C
LTC3621EMS8E-3.3#PBF	LTC3621EMS8E-3.3#TRPBF	LTGNY	8-Lead Plastic MSOP	–40°C to 125°C
LTC3621IMS8E-3.3#PBF	LTC3621IMS8E-3.3#TRPBF	LTGNY	8-Lead Plastic MSOP	–40°C to 125°C
LTC3621HMS8E-3.3#PBF	LTC3621HMS8E-3.3#TRPBF	LTGNY	8-Lead Plastic MSOP	–40°C to 150°C
LTC3621EMS8E-5#PBF	LTC3621EMS8E-5#TRPBF	LTGNX	8-Lead Plastic MSOP	–40°C to 125°C
LTC3621IMS8E-5#PBF	LTC3621IMS8E-5#TRPBF	LTGNX	8-Lead Plastic MSOP	–40°C to 125°C
LTC3621HMS8E-5#PBF	LTC3621HMS8E-5#TRPBF	LTGNX	8-Lead Plastic MSOP	–40°C to 150°C
LTC3621EDCB-2#PBF	LTC3621EDCB-2#TRPBF	LGHY	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3621IDCB-2#PBF	LTC3621IDCB-2#TRPBF	LGHY	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3621EDCB-23.3#PBF	LTC3621EDCB-23.3#TRPBF	LGQG	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3621IDCB-23.3#PBF	LTC3621IDCB-23.3#TRPBF	LGQG	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3621EDCB-25#PBF	LTC3621EDCB-25#TRPBF	LGQD	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3621IDCB-25#PBF	LTC3621IDCB-25#TRPBF	LGQD	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3621EMS8E-2#PBF	LTC3621EMS8E-2#TRPBF	LTGHZ	8-Lead Plastic MSOP	–40°C to 125°C
LTC3621IMS8E-2#PBF	LTC3621IMS8E-2#TRPBF	LTGHZ	8-Lead Plastic MSOP	–40°C to 125°C
LTC3621HMS8E-2#PBF	LTC3621HMS8E-2#TRPBF	LTGHZ	8-Lead Plastic MSOP	–40°C to 150°C
LTC3621EMS8E-23.3#PBF	LTC3621EMS8E-23.3#TRPBF	LTGNZ	8-Lead Plastic MSOP	–40°C to 125°C
LTC3621IMS8E-23.3#PBF	LTC3621IMS8E-23.3#TRPBF	LTGNZ	8-Lead Plastic MSOP	–40°C to 125°C
LTC3621HMS8E-23.3#PBF	LTC3621HMS8E-23.3#TRPBF	LTGNZ	8-Lead Plastic MSOP	–40°C to 150°C
LTC3621EMS8E-25#PBF	LTC3621EMS8E-25#TRPBF	LTGQB	8-Lead Plastic MSOP	–40°C to 125°C
LTC3621IMS8E-25#PBF	LTC3621IMS8E-25#TRPBF	LTGQB	8-Lead Plastic MSOP	–40°C to 125°C
LTC3621HMS8E-25#PBF	LTC3621HMS8E-25#TRPBF	LTGQB	8-Lead Plastic MSOP	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C. (Note 3) V_{IN} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Voltage			2.7		17	V
V_{OUT}	Operating Voltage			0.6		V_{IN}	V
I_{VIN}	Input Quiescent Current	Shutdown Mode, V_{RUN} = 0V Burst Mode Operation Forced Continuous Mode (Note 4), V_{FB} < 0.6V			0.1 3.5 1.5	1.0 7	µA µA mA
V_{FB}	Regulated Feedback Voltage	LTC3621/LTC3621-2	 ●	0.594 0.591	0.6 0.6	0.606 0.609	V V
I_{FB}	FB Input Current	LTC3621/LTC3621-2				10	nA
V_{OUT}	Regulated Fixed Output Voltage	LTC3621-3.3/LTC3621-23.3	 ●	3.267 3.250	3.3 3.3	3.333 3.350	V V
		LTC3621-5/LTC3621-25	 ●	4.950 4.925	5.0 5.0	5.050 5.075	V V
$I_{FB(VOUT)}$	Feedback Input Leakage Current	Fixed Output Versions			2	10	µA
$\Delta V_{LINE(REG)}$	Reference Voltage Line Regulation	V_{IN} = 2.7V to 17V (Note 5)			0.01	0.015	%/V
$\Delta V_{LOAD(REG)}$	Output Voltage Load Regulation	(Note 5)			0.1		%
I_{LSW}	NMOS Switch Leakage PMOS Switch Leakage				0.1 0.1	1 1	µA µA
$R_{DS(ON)}$	NMOS On-Resistance (Bottom FET)	V_{IN} = 5V			0.15		Ω
	PMOS On-Resistance (Top FET)				0.37		Ω
D_{MAX}	Maximum Duty Cycle	V_{FB} = 0.5V, $V_{MODE/SYNC}$ = 1.5V	●		100		%
$t_{ON(MIN)}$	Minimum On-Time				60		ns
V_{RUN}	RUN Input High Threshold RUN Input Low Threshold			 0.3		1.0	V V
I_{RUN}	RUN Input Current	V_{RUN} = 12V			0	20	nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C. (Note 3) V_{IN} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{MODE/SYNC}$	Pulse-Skipping Mode Burst Mode Operation Forced Continuous Mode			 V_{INTVCC} – 0.4 1.0		0.3 V_{INTVCC} – 1.2	V V V
$I_{MODE/SYNC}$	MODE/SYNC Input Current				0	20	nA
t_{SS}	Internal Soft-Start Time				0.8		ms
I_{LIM}	Peak Current Limit	 (E/I-Grade) (H-Grade)	 ● ●	1.44 1.30 1.2	1.60	1.76 1.80 1.80	A A A
V_{UVLO}	V_{INTVCC} Undervoltage Lockout	V_{IN} Ramping Up		2.4	2.6	2.7	V
$V_{UVLO(HYS)}$	V_{INTVCC} Undervoltage Lockout Hysteresis				250		mV
V_{OVLO}	V_{IN} Overvoltage Lockout Rising		●	18	19	20	V
$V_{OVLO(HYS)}$	V_{IN} Overvoltage Lockout Hysteresis				300		mV
f_{OSC}	Oscillator Frequency	LTC3621/LTC3621-3.3/LTC3621-5 (E/I-Grade) (H-Grade)	 ● ●	0.92 0.82 0.78	1.00	1.08 1.16 1.16	MHz MHz MHz
		LTC3621-2/LTC3621-23.3/LTC3621-25 (E/I-Grade) (H-Grade)	 ● ●	2.05 1.8 1.7	2.25	2.45 2.6 2.6	MHz MHz MHz
f_{SYNC}	SYNC Capture Range			60		140	%
V_{INTVCC}	V_{INTVCC} LDO Output Voltage	V_{IN} > 4V			3.6		V
ΔV_{PGOOD}	Power Good Range				±7.5	±12.5	%
R_{PGOOD}	Power Good Resistance	PGOOD $R_{DS(ON)}$ at 500µA			275	350	Ω
t_{PGOOD}	PGOOD Delay	PGOOD Low to High PGOOD High to Low			0 32		Cycles Cycles
I_{PGOOD}	PGOOD Leakage Current					100	nA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Transient absolute maximum voltages should not be applied for more than 4% of the switching duty cycle.

Note 3: The LTC3621 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3621E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3621I is guaranteed over the –40°C to 125°C operating junction temperature range, and the LTC3621H is guaranteed over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 4: The quiescent current in forced continuous mode does not include switching loss of the power FETs.

Note 5: The LTC3621 is tested in a proprietary test mode that connects V_{FB} to the output of error amplifier.

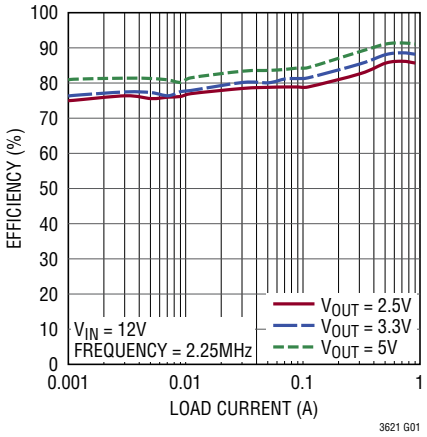
Note 6: T_J is calculated from the ambient, T_A, and power dissipation, P_D, according to the following formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

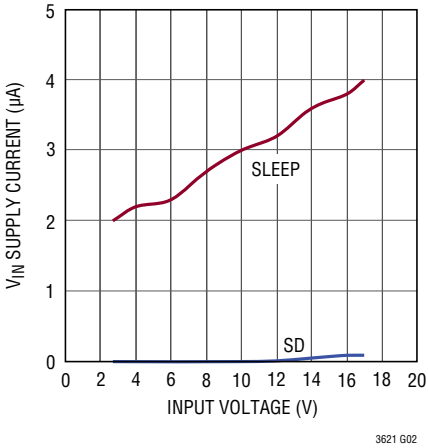
Note 7: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

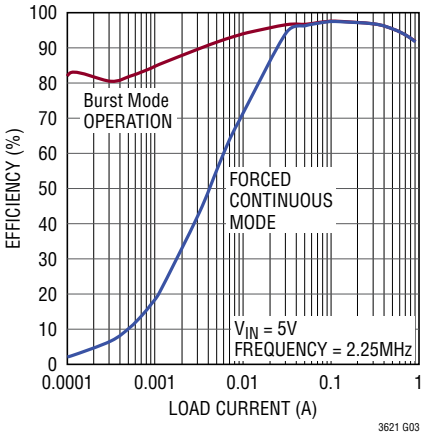
Efficiency vs Load Current (Burst Mode Operation)



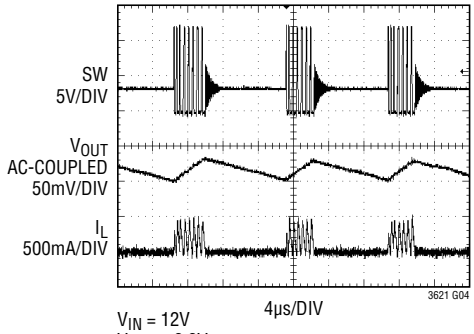
V_{IN} Supply Current vs Input Voltage



Efficiency vs Load at Dropout Operation

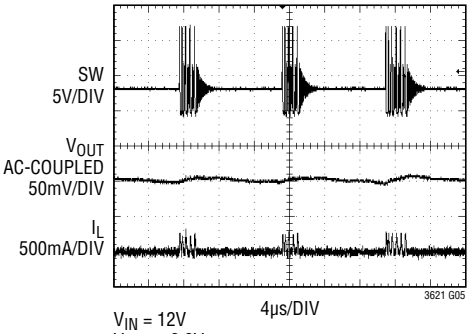


Burst Mode Operation



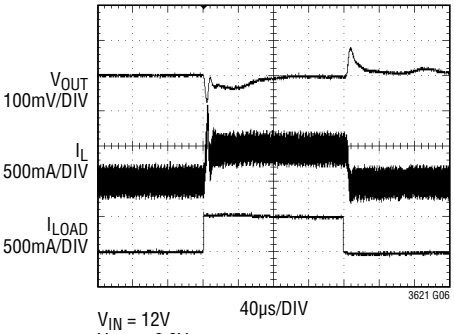
V_{IN} = 12V
V_{OUT} = 3.3V
Burst Mode OPERATION
I_{OUT} = 50mA
L = 2.2µH

Pulse-Skipping Mode Operation



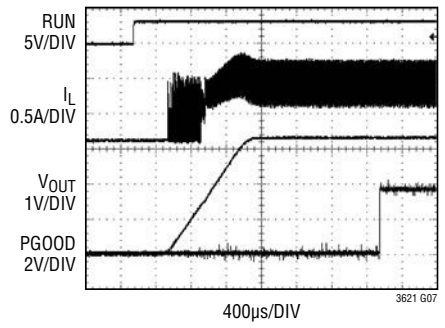
V_{IN} = 12V
V_{OUT} = 3.3V
PULSE SKIP MODE
I_{OUT} = 10mA
L = 2.2µH

Load Step

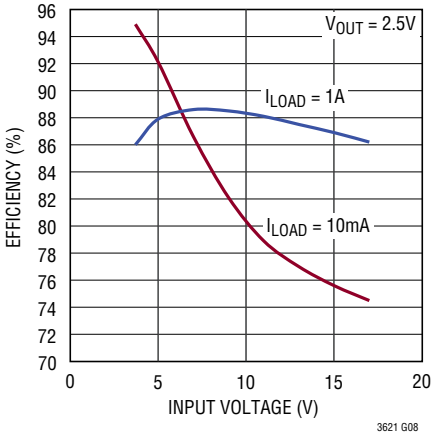


V_{IN} = 12V
V_{OUT} = 3.3V
I_{LOAD} = 0.05A

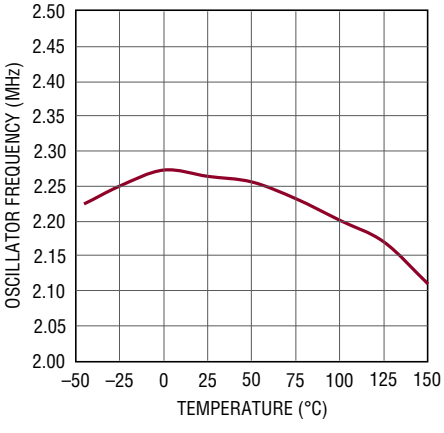
Soft-Start Operation



Efficiency vs Input Voltage

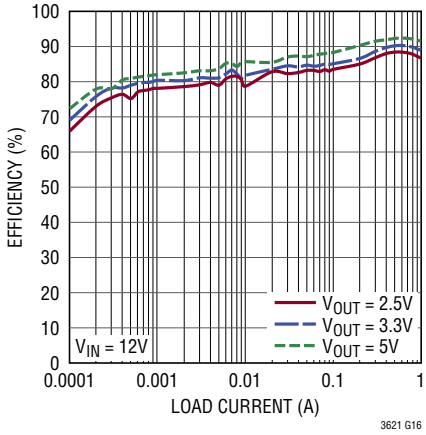


Oscillator Frequency vs Temperature

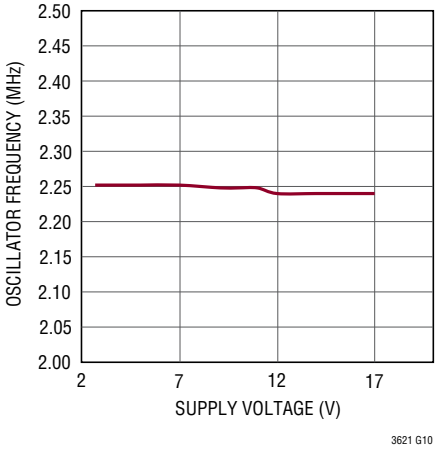


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

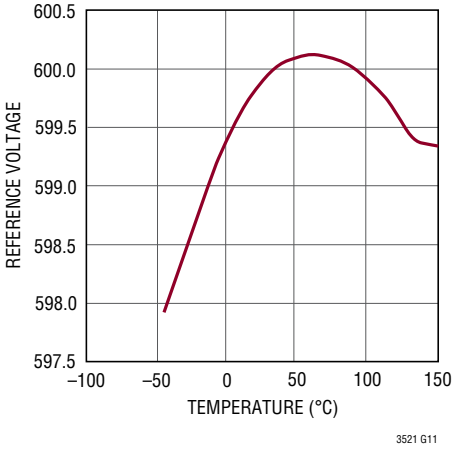
Efficiency vs Load at 1MHz



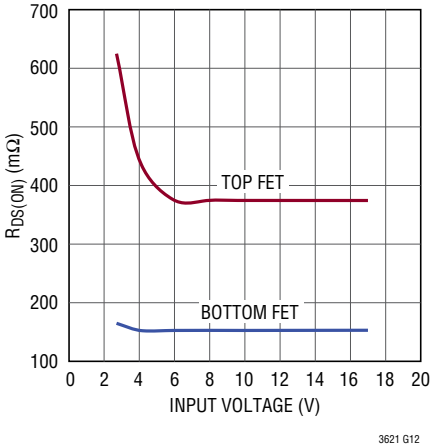
Oscillator Frequency vs Supply Voltage



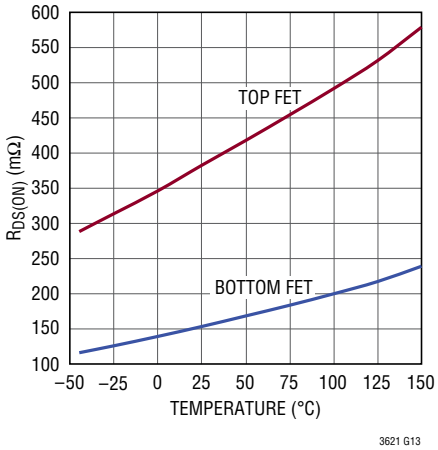
Reference Voltage vs Temperature



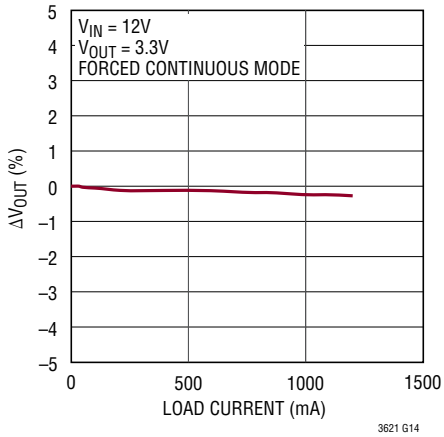
$R_{DS(ON)}$ vs Input Voltage



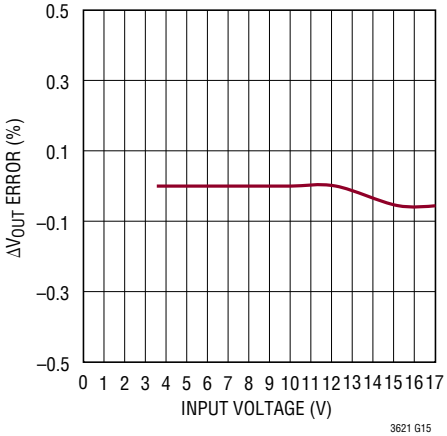
$R_{DS(ON)}$ vs Temperature



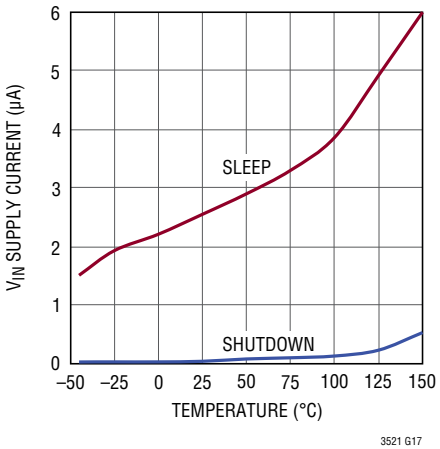
Load Regulation



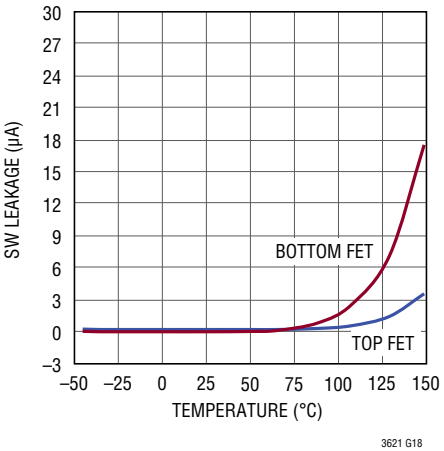
Line Regulation



V_{IN} Supply Current vs Temperature



Switch Leakage vs Temperature



PIN FUNCTIONS (DFN/MSOP)

SW (Pin 1/Pin 1): Switch Node Connection to the Inductor of the Step-Down Regulator.

V_{IN} (Pin 2/Pin 2): Input Voltage of the Step-Down Regulator.

RUN (Pin 3/Pin 3): Logic Controlled RUN Input. Do not leave this pin floating. Logic high activates the step-down regulator.

FB (Pin 4/Pin 5): Feedback Input to the Error Amplifier of the Step-Down Regulator. Connect a resistor divider tap to this pin. The output voltage can be adjusted from 0.6V to V_{IN} by:

$$V_{OUT} = 0.6V \bullet [1 + (R2/R1)]$$

For Fixed V_{OUT} options, connect the FB pin directly to V_{OUT}.

PGOOD (Pin 4, MSOP Package Only): V_{OUT} within Regulation Indicator.

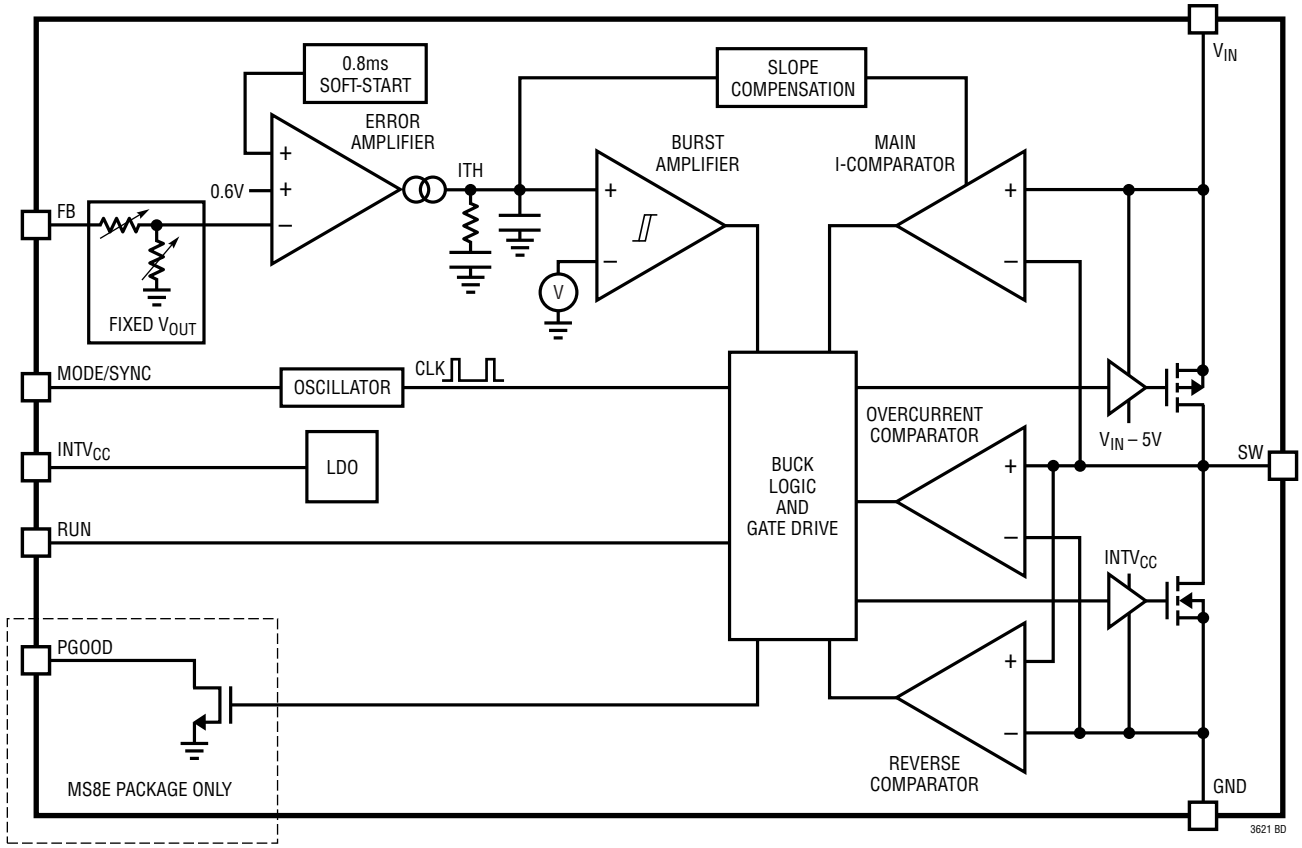
$INTV_{CC}$ (Pin 5/Pin 6): Low Dropout Regulator. Bypass with at least 1µF to Ground.

MODE/SYNC (Pin 6/Pin 7): Burst Mode Select and External Clock Synchronization of the Step-Down Regulator. Tie MODE/SYNC to $INTV_{CC}$ for Burst Mode operation with a 400mA peak current clamp, tie MODE/SYNC to GND for pulse skipping operation, and tie MODE/SYNC to a voltage between 1V and V_{INTVCC} – 1.2V for forced continuous mode. Furthermore, connecting MODE/SYNC to an external clock will sync the system clock to the external clock and put the part in forced continuous mode.

GND (Exposed Pad Pin 7/Pin 9): Ground Backplane for Power and Signal Ground. Must be soldered to PCB ground.

SGND (Pin 8, MSOP Package Only): Signal Ground.

BLOCK DIAGRAM



OPERATION

The LTC3621 uses a constant-frequency, peak current mode architecture. It operates through a wide V_{IN} range and regulates with ultralow quiescent current. The operation frequency is set at either 2.25MHz or 1MHz and can be synchronized to an external oscillator ±40% of the inherent frequency. To suit a variety of applications, the selectable MODE/SYNC pin allows the user to trade off output ripple for efficiency.

The output voltage is set by an external divider returned to the FB pin. An error amplifier compares the divided output voltage with a reference voltage of 0.6V and adjusts the peak inductor current accordingly. In the MS8E package, overvoltage and undervoltage comparators will pull the PGOOD output low if the output voltage is not within 7.5% of the programmed value. The PGOOD output will go high immediately after achieving regulation and will go low 32 clock cycles after falling out of regulation.

Main Control Loop

During normal operation, the top power switch (P-channel MOSFET) is turned on at the beginning of a clock cycle. The inductor current is allowed to ramp up to a peak level. Once that level is reached, the top power switch is turned off and the bottom switch (N-channel MOSFET) is turned on until the next clock cycle. The peak current level is controlled by the internally compensated ITH voltage, which is the output of the error amplifier. This amplifier compares the FB voltage to the 0.6V internal reference. When the load current increases, the FB voltage decreases slightly below the reference, which causes the error amplifier to increase the ITH voltage until the average inductor current matches the new load current.

The main control loop is shut down by pulling the RUN pin to ground.

Low Current Operation

Two discontinuous-conduction modes (DCMs) are available to control the operation of the LTC3621 at low currents. Both modes, Burst Mode operation and pulse-skipping, automatically switch from continuous operation to the selected mode when the load current is low.

To optimize efficiency, Burst Mode operation can be selected by tying the MODE/SYNC pin to $INTV_{CC}$. In Burst Mode operation, the peak inductor current is set to be at least 400mA, even if the output of the error amplifier demands less. Thus, when the switcher is on at relatively light output loads, FB voltage will rise and cause the ITH voltage to drop. Once the ITH voltage goes below 0.2V, the switcher goes into its sleep mode with both power switches off. The switcher remains in this sleep state until the external load pulls the output voltage below its regulation point. During sleep mode, the part draws an ultralow 3.5µA of quiescent current from V_{IN}.

To minimize V_{OUT} ripple, pulse-skipping mode can be selected by grounding the MODE/SYNC pin. In the LTC3621, pulse-skipping mode is implemented similarly to Burst Mode operation with the peak inductor current set to be at about 66mA. This results in lower output voltage ripple than in Burst Mode operation with the trade-off being slightly lower efficiency.

Forced Continuous Mode Operation

Aside from the two discontinuous-conduction modes, the LTC3621 also has the ability to operate in the forced continuous mode by setting the MODE/SYNC voltage between 1V and V_{INTVCC} – 1V. In forced continuous mode, the switcher will switch cycle by cycle regardless of what the output load current is. If forced continuous mode is selected, the minimum peak current is set to be –133mA in order to ensure that the part can operate continuously at zero output load.

High Duty Cycle/Dropout Operation

When the input supply voltage decreases towards the output voltage, the duty cycle increases and slope compensation is required to maintain the fixed switching frequency. The LTC3621 has internal circuitry to accurately maintain the peak current limit (I_{LIM}) of 1.6A even at high duty cycles.

As the duty cycle approaches 100%, the LTC3621 enters dropout operation. During dropout, if force continuous mode is selected, the top PMOS switch is turned on continuously, and all active circuitry is kept alive. However, if Burst Mode operation or pulse-skipping mode is

OPERATION

selected, the part will transition in and out of sleep mode depending on the output load current. This significantly reduces the quiescent current, thus prolonging the use of the input supply.

V_{IN} Overvoltage Protection

In order to protect the internal power MOSFET devices against transient voltage spikes, the LTC3621 constantly monitors the V_{IN} pin for an overvoltage condition. When V_{IN} rises above 19V, the regulator suspends operation by shutting off both power MOSFETs. Once V_{IN} drops below 18.7V, the regulator immediately resumes normal operation. The regulator executes its soft-start function when exiting an overvoltage condition.

Low Supply Operation

The LTC3621 incorporates an undervoltage lockout circuit which shuts down the part when the input voltage drops below 2.7V. As the input voltage rises slightly above the undervoltage threshold, the switcher will begin its basic operation. However, the $R_{DS(ON)}$ of the top and bottom switch will be slightly higher than that specified in the electrical characteristics due to lack of gate drive. Refer to graph of $R_{DS(ON)}$ versus V_{IN} for more details.

Soft-Start

The LTC3621 has an internal 800µs soft-start ramp. During start-up soft-start operation, the switcher will operate in pulse-skipping mode.

APPLICATIONS INFORMATION

Output Voltage Programming

For non-fixed output voltage parts, the output voltage is set by external resistive divider according to the following equation:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R2}{R1}\right)$$

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 1.

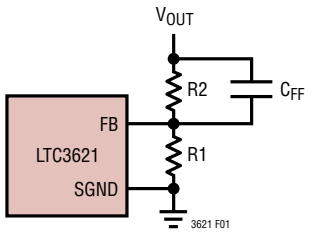


Figure 1. Setting the Output Voltage

Input Capacitor (C_{IN}) Selection

The input capacitance, C_{IN}, is needed to filter the square wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by:

$$I_{RMS} \cong I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where:

$$I_{RMS} \cong \frac{I_{OUT}}{2}$$

This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Output Capacitor (C_{OUT}) Selection

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing

APPLICATIONS INFORMATION

the load transient response. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} < \Delta I_L \left(\frac{1}{8 \bullet f \bullet C_{OUT}} + ESR \right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors are very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics and small footprints.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the V_{IN} input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R and X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. Typically, five cycles are required to respond to a load step, but only in the first cycle does the output voltage drop linearly. The output droop, V_{DROOP}, is usually about three times the linear drop of the first cycle. Thus, a good place to start with the output capacitor value is approximately:

$$C_{OUT} = 3 \frac{\Delta I_{OUT}}{f \bullet V_{DROOP}}$$

More capacitance may be required depending on the duty cycle and load-step requirements. In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low. A 10µF ceramic capacitor is usually enough for these conditions. Place this input capacitor as close to the V_{IN} pin as possible.

Output Power Good

In the MS8E package, when the LTC3621's output voltage is within the ±7.5% window of the regulation point, the output voltage is good and the PGOOD pin is pulled high with an external resistor. Otherwise, an internal open-drain pull-down device (275Ω) will pull the PGOOD pin low. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTC3621's PGOOD falling edge includes a blanking delay of approximately 32 switching cycles.

Frequency Sync Capability

The LTC3621 has the capability to sync to a frequency within a ±40% range of the internal programmed frequency. It takes 2 to 3 cycles of external clock pulses to engage the sync mode. If the external clock signal were to stop switching during operation, it will take roughly 7µs for the part's internal sync signal to go low and respond accordingly. Once engaged in sync, the LTC3621 immediately runs at the external clock frequency in forced continuous mode.

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Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{V_{OUT}}{f \bullet L}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Lower ripple current reduces power losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency and operating frequency.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As the inductance or frequency increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Copper losses also increase as frequency increases.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard”, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don’t radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Coilcraft, Toko, Vishay, NEC/Tokin, TDK and Würth Electronik. Refer to Table 1 for more details.

Checking Transient Response

The regular loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to the $\Delta I_{LOAD} \bullet$ ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. In addition, a feedforward capacitor can be added to improve the high frequency response, as shown in Figure 1. Capacitor C_{FF} provides phase lead by creating a high frequency zero with R2, which improves the phase margin.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. LTpowerCAD™ and LTSpice® can be used to check control loop and transient performance.

In some applications, a more severe transient can be caused by switching in loads with large (>1µF) load capacitors. The discharged load capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap™ controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection and soft-starting.

APPLICATIONS INFORMATION

Table 1. Inductor Selection Table

INDUCTOR	INDUCTANCE (µH)	DCR (mΩ)	MAX CURRENT (A)	DIMENSIONS (mm)	HEIGHT (mm)	MANUFACTURER
IHLP-1616BZ-11 Series	1.0 2.2 4.7	24 61 95	4.5 3.25 1.7	4.3 × 4.7 4.3 × 4.7 4.3 × 4.7	2 2 2	Vishay www.vishay.com
IHLP-2020BZ-01 Series	1 2.2 3.3 4.7 5.6 6.8	18.9 45.6 79.2 108 113 139	7 4.2 3.3 2.8 2.5 2.4	5.4 × 5.7 5.4 × 5.7 5.4 × 5.7 5.4 × 5.7 5.4 × 5.7 5.4 × 5.7	2 2 2 2 2 2	
FDV0620 Series	1 2.2 3.3 4.7	18 37 51 68	5.7 4 3.2 2.8	6.7 × 7.4 6.7 × 7.4 6.7 × 7.4 6.7 × 7.4	2 2 2 2	Toko www.toko.com
MPLC0525L Series	1 1.5 2.2	16 24 40	6.4 5.2 4.1	6.2 × 5.4 6.2 × 5.4 6.2 × 5.4	2.5 2.5 2.5	NEC/Tokin www.nec-tokin.com
XFL4020 Series	1.0 1.5 2.2 3.3 4.7	10.8 14.4 21.3 34.8 52.2	5.1 4.4 3.5 2.5 2.5	4 × 4 4 × 4 4 × 4 4 × 4 4 × 4	2.1 2.1 2.1 2.1 2.1	Coilcraft www.coilcraft.com
RLF7030 Series	1 1.5 2.2 3.3 4.7 6.8	8.8 9.6 12 20 31 45	6.4 6.1 5.4 4.1 3.4 2.8	6.9 × 7.3 6.9 × 7.3 6.9 × 7.3 6.9 × 7.3 6.9 × 7.3 6.9 × 7.3	3.2 3.2 3.2 3.2 3.2 3.2	TDK www.tdk.com
WE-TPC 4828 Series	1.2 1.8 2.2 2.7 3.3 3.9 4.7	17 20 23 27 30 47 52	3.1 2.7 2.5 2.35 2.15 1.72 1.55	4.8 × 4.8 4.8 × 4.8 4.8 × 4.8 4.8 × 4.8 4.8 × 4.8 4.8 × 4.8 4.8 × 4.8	2.8 2.8 2.8 2.8 2.8 2.8 2.8	Würth Elektronik www.we-online.com

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (\text{Loss1} + \text{Loss2} + \ldots)$$

where Loss1, Loss2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LTC3621 circuits: 1) I^2R losses, 2) switching and biasing losses, 3) other losses.

1. I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L but is "chopped" between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus to obtain I^2R losses:

$$I^2R \text{ losses} = I_{OUT}^2(R_{SW} + R_L)$$

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2. The switching current is the sum of the MOSFET driver and control currents. The power MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} that is typically much larger than the DC control bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs and f is the switching frequency. The power loss is thus:

   Switching Loss = $I_{GATECHG} \bullet V_{IN}$

   The gate charge loss is proportional to V_{IN} and f and thus their effects will be more pronounced at higher supply voltages and higher frequencies.

3. Other "hidden" losses such as transition loss and copper trace and internal load resistances can account for additional efficiency degradations in the overall power system. It is very important to include these "system" level losses in the design of a system. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. The LTC3621 internal power devices switch quickly enough that these losses are not significant compared to other sources. These losses plus other losses, including diode conduction losses during dead-time and inductor core losses, generally account for less than 2% total additional loss.

Thermal Conditions

In a majority of applications, the LTC3621 does not dissipate much heat due to its high efficiency and low thermal resistance of its exposed pad package. However, in applications where the LTC3621 is running at high ambient temperature, high V_{IN}, high switching frequency, and maximum output current load, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 160°C, both power switches will be turned off until the temperature drops about 15°C cooler.

To avoid the LTC3621 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

As an example, consider the case when the LTC3621 is used in applications where V_{IN} = 12V, I_{OUT} = 1A, f = 2.25MHz, V_{OUT} = 1.8V. The equivalent power MOSFET resistance R_{SW} is:

$$R_{SW} = R_{DS(ON)TOP} \bullet \frac{V_{OUT}}{V_{IN}} + R_{DS(ON)BOT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$= 370m\Omega \bullet \frac{1.8V}{12V} + 150m\Omega \bullet \left(1 - \frac{1.8V}{12V}\right)$$

$$= 183m\Omega$$

The V_{IN} current during 2.25MHz force continuous operation with no load is about 5mA, which includes switching and internal biasing current loss, transition loss, inductor core loss and other losses in the application. Therefore, the total power dissipated by the part is:

$$P_D = I_{OUT}^2 \bullet R_{SW} + V_{IN} \bullet I_{IN(Q)}$$
$$= 1A^2 \bullet 183m\Omega + 12V \bullet 5mA$$
$$= 243mW$$

The DFN 2mm × 3mm package junction-to-ambient thermal resistance, θ_{JA}, is around 64°C/W. Therefore, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately:

$$T_J = 0.243W \bullet 64°C/W + 25°C = 40.6°C$$

Remembering that the above junction temperature is obtained from an $R_{DS(ON)}$ at 25°C, we might recalculate the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature. Redoing the calculation assuming that R_{SW} increased 5% at 40.6°C yields a new junction temperature of 41.1°C. If the application calls for a higher ambient temperature and/or higher switching frequency, care should be taken to reduce the temperature rise of the part by using a heat sink or forced air flow.

APPLICATIONS INFORMATION

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3621 (refer to Figure 3). Check the following in your layout:

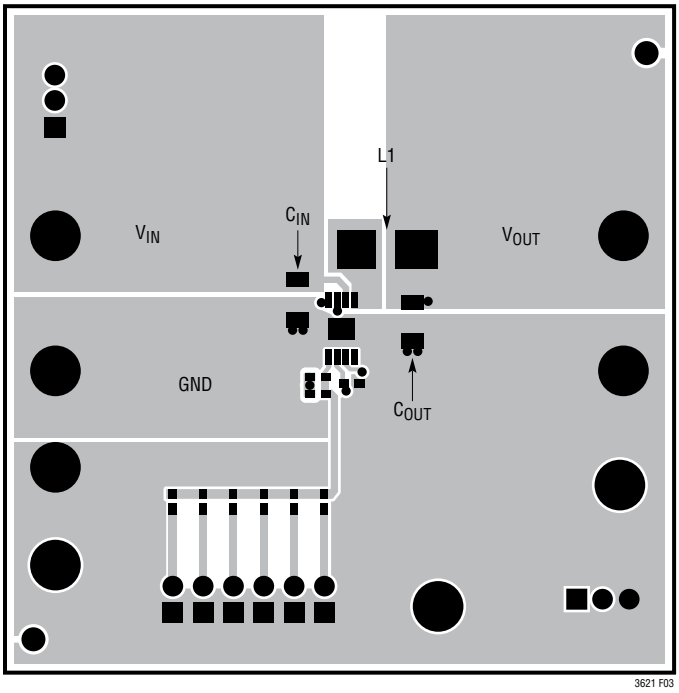


Figure 3. Sample PCB Layout

1. Do the capacitors C_{IN} connect to the V_{IN} pin and GND pin as close as possible? These capacitors provide the AC current to the internal power MOSFETs and their drivers.
2. Are C_{OUT} and L closely connected? The (–) plate of C_{OUT} returns current to GND.
3. The resistive divider, R1 and R2, must be connected between the (+) plate of C_{OUT} and a ground line terminated near GND. The feedback signal V_{FB} should be routed away from noisy components and traces, such as the SW line, and its trace should be minimized. Keep R1 and R2 close to the IC.
4. Solder the exposed pad (Pin 7 for DFN, Pin 9 for MSOP) on the bottom of the package to the GND plane. Connect this GND plane to other layers with thermal vias to help dissipate heat from the LTC3621.
5. Keep sensitive components away from the SW pin. The feedback resistors and $INTV_{CC}$ bypass capacitors should be routed away from the SW trace and the inductor.
6. A ground plane is preferred.
7. Flood all unused areas on all layers with copper, which reduces the temperature rise of power components. These copper areas should be connected to GND.

Design Example

As a design example, consider using the LTC3621 in an application with the following specifications:

V_{IN} = 10.8V to 13.2V

V_{OUT} = 3.3V

$I_{OUT(MAX)}$ = 1A

$I_{OUT(MIN)}$ = 0A

f_{SW} = 2.25MHz

Because efficiency and quiescent current is important at both 500mA and 0A current states, Burst Mode operation will be utilized.

Given the internal oscillator of 2.25MHz, we can calculate the inductor value for about 40% ripple current at maximum V_{IN}:

$$L = \left(\frac{3.3V}{2.25MHz \bullet 0.4A}\right)\left(1-\frac{3.3V}{13.2V}\right) = 2.75\mu H$$

Given this, a 2.7µH or 3.3µH, >1.2A inductor would suffice.

C_{OUT} will be selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. For this design, a 22µF ceramic capacitor will be used.

C_{IN} should be sized for a maximum current rating of:

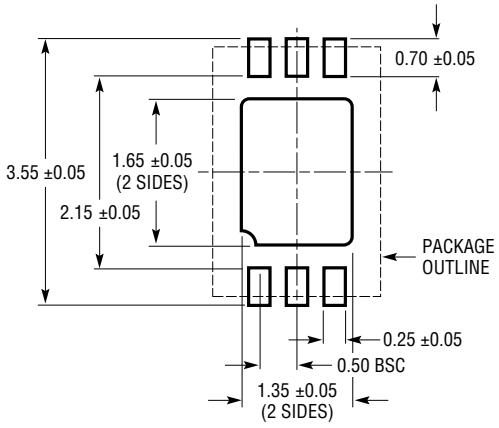
$$I_{RMS} = 1A\left(\frac{3.3V}{13.2V}\right)\left(\frac{13.2V}{3.3V}-1\right)^{1/2} = 0.43A$$

Decoupling the V_{IN} pin with 10µF ceramic capacitors is adequate for most applications.

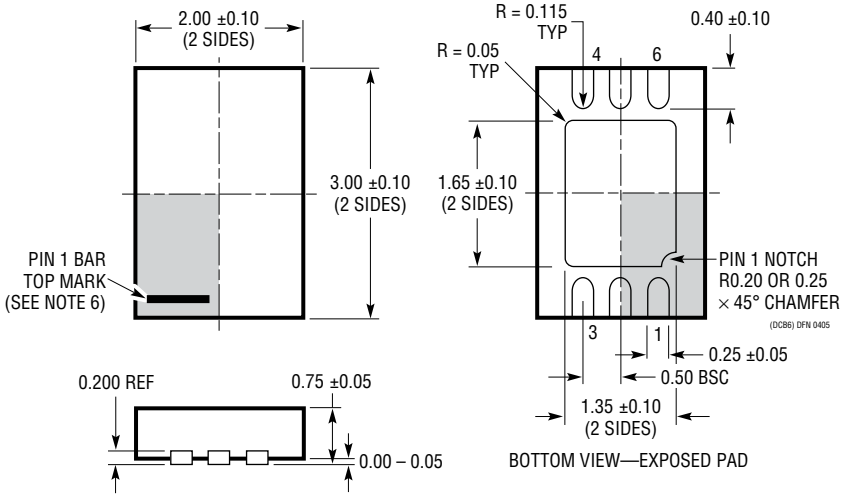
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DCB Package
6-Lead Plastic DFN (2mm × 3mm)
(Reference LTC DWG # 05-08-1715 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



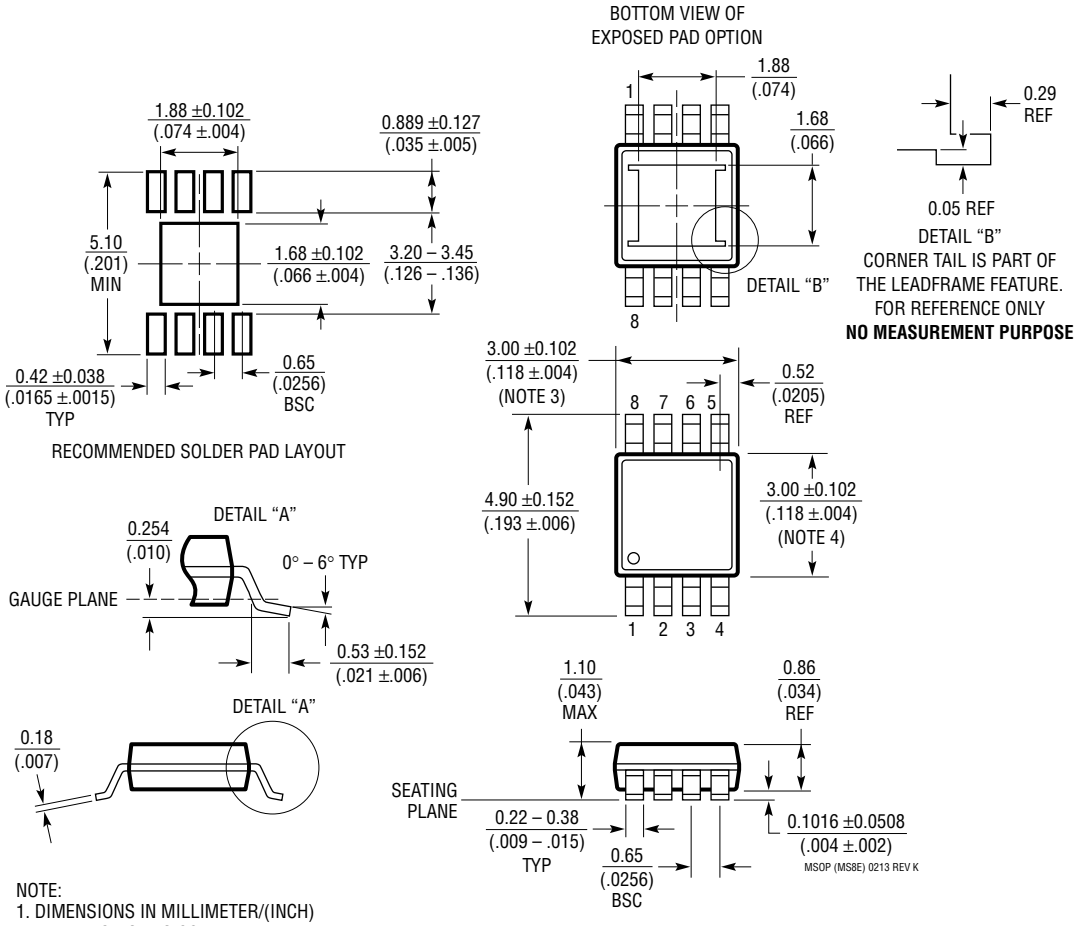
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (TBD)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS8E Package
8-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1662 Rev K)



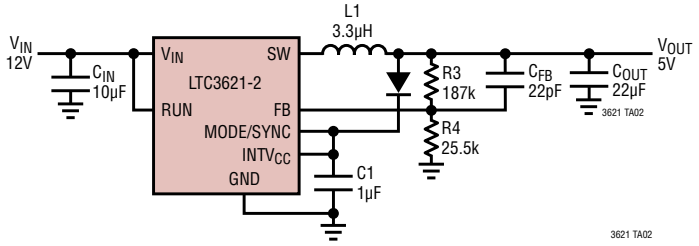
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

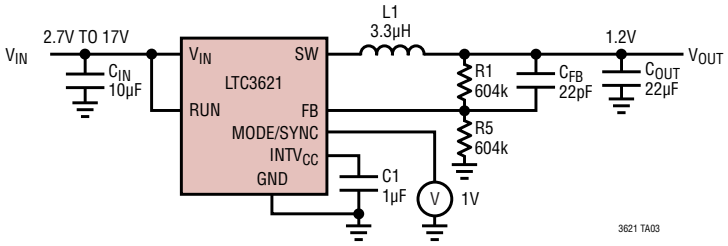
REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/13	Updated Efficiency curve	1
		Input quiescent current limits changed	2
		Oscillator frequency (f_{OSC}) conditions changed	2
B	03/14	Clarified Features and Description	1
		Clarified options	1
		Clarified ordering info and Absolute Maximum Ratings	2
		Added Note 7	2 - 3
		Clarified electrical specifications	3
		Clarified pin descriptions, Block Diagram	6
		Clarified Operation description	7
		Added box to figure	7
		Clarified Applications Information	9 - 13
		Clarified Typical Application	16
		Swapped locations of C_{FB} and R1	18
C	04/15	Added H-Grade Options and Specifications	2, 3
		Added H-Grade Options and Specifications	4
		Clarified Graphs to Accommodate 150°C Performance	5, 6

TYPICAL APPLICATION

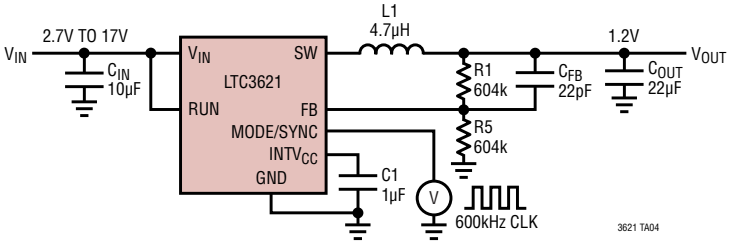
5V$_{OUT}$ with 400mA Burst Mode Operation, 2.25MHz



1.2V$_{OUT}$, Forced Continuous Mode, 1MHz



1.2V$_{OUT}$, Synchronized to 600kHz, Forced Continuous Mode



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3646/ LTC3646-1	40V, 1A (I_{OUT}), 3MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4V to 40V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 140µA, I_{SD} < 8µA, 3mm × 4mm DFN-14, MSOP-16E Packages
LTC3600	1.5A, 15V, 4MHz Synchronous Rail-to-Rail Single Resistor Step-Down Regulator	95% Efficiency, V_{IN}: 4V to 15V, $V_{OUT(MIN)}$ = 0V, I_Q = 700µA, I_{SD} < 1µA, 3mm × 3mm DFN-12, MSOP-12E Packages
LTC3601	15V, 1.5A (I_{OUT}) 4MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} < 1µA, 4mm × 4mm QFN-20, MSOP-16E Packages
LTC3603	15V, 2.5A (I_{OUT}) 3MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 4mm × 4mm QFN-20, MSOP-16E Packages
LTC3633/ LTC3633A	15V/20V, Dual 3A (I_{OUT}) 4MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 3.6V to 15V/20V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 500µA, I_{SD} < 15µA, 4mm × 5mm QFN-28, TSSOP-28E Packages. A Version Up to 20V_{IN}
LTC3605/ LTC3605A	15V/20V, 5A (I_{OUT}) 4MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4V to 15V/20V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 2mA, I_{SD} < 15µA, 4mm × 4mm QFN-24 Package. A Version Up to 20V_{IN}
LTC3604	15V, 2.5A (I_{OUT}) 4MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 3.6V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} < 14µA, 3mm × 3mm QFN-16, MSOP-16E Packages
LTC1877	600mA (I_{OUT}) 550kHz Synchronous Step-Down DC/DC Converter	V_{IN}: 2.7V to 10V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 10µA, I_{SD} < 1µA, MSOP-8 Package
LT8610/LT8611	42V, 2.5A (I_{OUT}) Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN}: 3.4V to 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-16E Package

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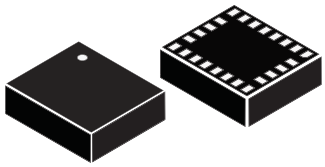
2.2.12. Acelerómetro, Magnetómetro y Giroscopio

LSM9DS1

iNEMO inertial module: 3D accelerometer, 3D gyroscope, 3D magnetometer

Datasheet - production data



LGA-24L (3.5x3x1.0 mm)

Features

- 3 acceleration channels, 3 angular rate channels, 3 magnetic field channels
- ±2/±4/±8/±16 *g* linear acceleration full scale
- ±4/±8/±12/±16 gauss magnetic full scale
- ±245/±500/±2000 dps angular rate full scale
- 16-bit data output
- SPI / I^2C serial interfaces
- Analog supply voltage 1.9 V to 3.6 V
- “Always-on” eco power mode down to 1.9 mA
- Programmable interrupt generators
- Embedded temperature sensor
- Embedded FIFO
- Position and motion detection functions
- Click/double-click recognition
- Intelligent power saving for handheld devices
- ECOPACK®, RoHS and “Green” compliant

Applications

- Indoor navigation
- Smart user interfaces
- Advanced gesture recognition
- Gaming and virtual reality input devices
- Display/map orientation and browsing

Description

The LSM9DS1 is a system-in-package featuring a 3D digital linear acceleration sensor, a 3D digital angular rate sensor, and a 3D digital magnetic sensor.

The LSM9DS1 has a linear acceleration full scale of ±2*g*/±4*g*/±8/±16 *g,* a magnetic field full scale of ±4/±8/±12/±16 gauss and an angular rate of ±245/±500/±2000 dps.

The LSM9DS1 includes an I^2C serial bus interface supporting standard and fast mode (100 kHz and 400 kHz) and an SPI serial standard interface.

Magnetic, accelerometer and gyroscope sensing can be enabled or set in power-down mode separately for smart power management.

The LSM9DS1 is available in a plastic land grid array package (LGA) and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

Part number	Temperature range [°C]	Package	Packing
LSM9DS1	-40 to +85	LGA-24L	Tray
LSM9DS1TR	-40 to +85	LGA-24L	Tape and reel

Contents

List of tables

List of figures

1 Pin description

Figure 1. Pin connections

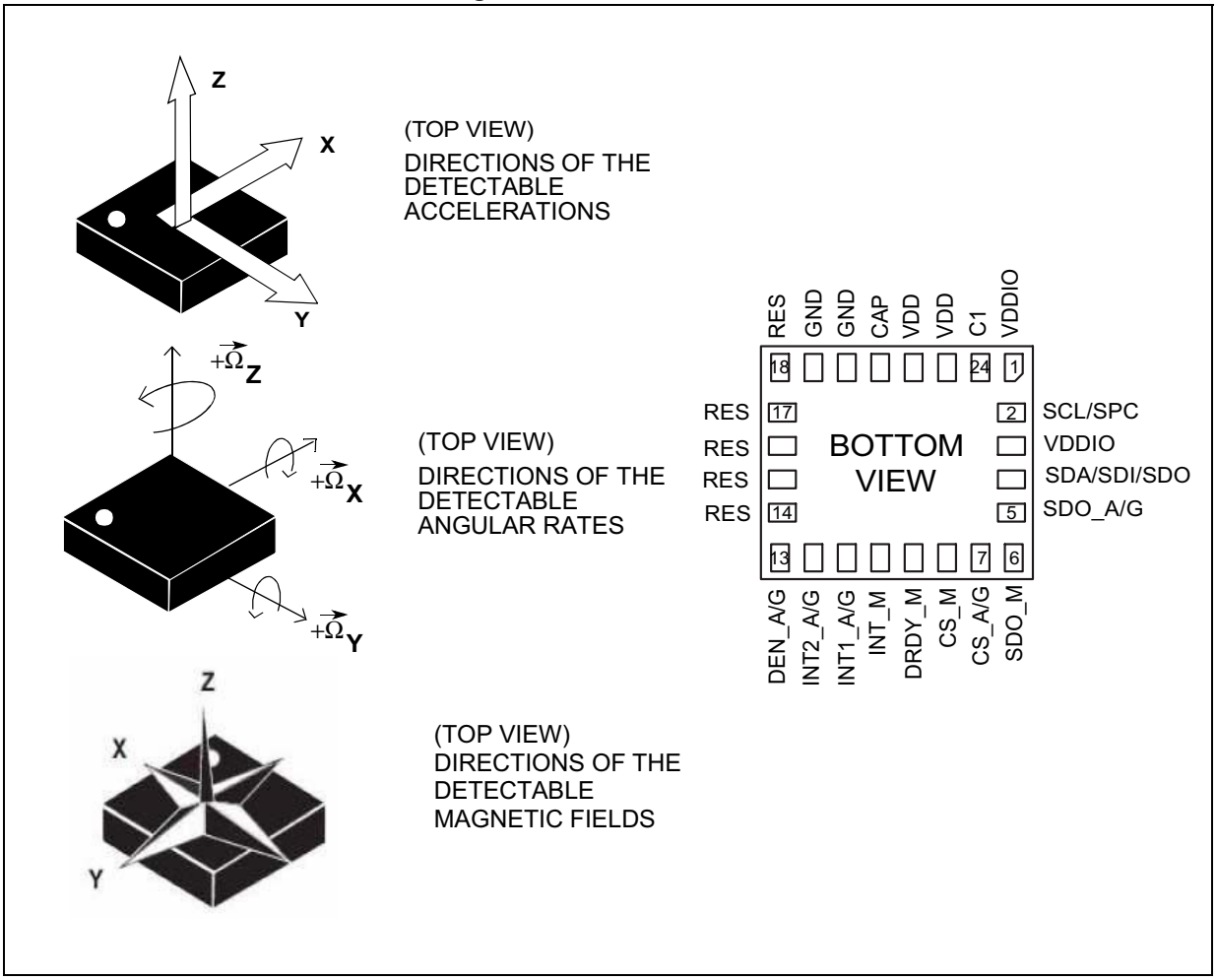


Table 2. Pin description

Pin #	Name	Function
1	VDDIO(1)	Power supply for I/O pins
2	SCL/SPC	I^2C serial clock (SCL) / SPI serial port clock (SPC)
3	VDDIO(2)	Power supply for I/O pins
4	SDA/SDI/SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	SDO_A/G	SPI serial data output (SDO) for the accelerometer and gyroscope I^2C least significant bit of the device address (SA0) for the accelerometer and gyroscope
6	SDO_M	SPI serial data output (SDO) for the magnetometer I^2C least significant bit of the device address (SA0) for the magnetometer
7	CS_A/G	SPI enable I^2C/SPI mode selection for the accelerometer and gyroscope (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
8	CS_M	SPI enable I^2C/SPI mode selection for the magnetometer (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
9	DRDY_M	Magnetic sensor data ready
10	INT_M	Magnetic sensor interrupt
11	INT1_A/G	Accelerometer and gyroscope interrupt 1
12	INT2_A/G	Accelerometer and gyroscope interrupt 2
13	DEN_A/G	Accelerometer and gyroscope data enable
14	RES	Reserved. Connected to GND.
15	RES	Reserved. Connected to GND.
16	RES	Reserved. Connected to GND.
17	RES	Reserved. Connected to GND.
18	RES	Reserved. Connected to GND.
19	GND	0 V supply
20	GND	0 V supply
21	CAP	Connected to GND with ceramic capacitor(3)
22	VDD(4)	Power supply
23	VDD(5)	Power supply
24	C1	Capacitor connection (C1 = 100 nF)

1. Recommended 100 nF filter capacitor.
2. Recommended 100 nF filter capacitor.
3. 10 nF (±10%), 16 V. 1 nF minimum value has to be guaranteed under 11 V bias condition.
4. Recommended 100 nF plus 10 µF capacitors.
5. Recommended 100 nF plus 10 µF capacitors.

2 Module specifications

2.1 Sensor characteristics

@ Vdd = 2.2 V, T = 25 °C unless otherwise noted[a]

Table 3. Sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
LA_FS	Linear acceleration measurement range			±2		*g*
				±4		
				±8		
				±16		
M_FS	Magnetic measurement range			±4		gauss
				±8		
				±12		
				±16		
G_FS	Angular rate measurement range			±245		dps
				±500		
				±2000		
LA_So	Linear acceleration sensitivity	Linear acceleration FS = ±2 *g*		0.061		m*g*/LSB
		Linear acceleration FS = ±4 *g*		0.122		
		Linear acceleration FS = ±8 *g*		0.244		
		Linear acceleration FS = ±16 *g*		0.732		
M_GN	Magnetic sensitivity	Magnetic FS = ±4 gauss		0.14		mgauss/ LSB
		Magnetic FS = ±8 gauss		0.29		
		Magnetic FS = ±12 gauss		0.43		
		Magnetic FS = ±16 gauss		0.58		
G_So	Angular rate sensitivity	Angular rate FS = ±245 dps		8.75		mdps/ LSB
		Angular rate FS = ±500 dps		17.50		
		Angular rate FS = ±2000 dps		70		
LA_TyOff	Linear acceleration typical zero-g level offset accuracy[2]	FS = ±8 *g*		±90		m*g*
M_TyOff	Zero-gauss level [3]	FS = ±4 gauss		±1		gauss
G_TyOff	Angular rate typical zero-rate level [4]	FS = ±2000 dps		±30		dps
M_DF	Magnetic disturbance field	Zero-gauss offset starts to degrade			50	gauss
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed
2. Typical zero-*g* level offset value after soldering
3. Typical zero-gauss level value after test and trimming
4. Typical zero rate level offset value after MSL3 preconditioning

a. The product is factory calibrated at 2.2 V. The operational power supply range is from 1.9 V to 3.6 V.

2.2 Electrical characteristics

@ Vdd = 2.2 V, T = 25 °C unless otherwise noted[b]

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		1.9		3.6	V
Vdd_IO	Module power supply for I/O		1.71		Vdd+0.1	
Idd_XM	Current consumption of the accelerometer and magnetic sensor in normal mode (2)			600		µA
Idd_G	Gyroscope current consumption in normal mode(3)			4.0		mA
Top	Operating temperature range		-40		+85	°C
Trise	Time for power supply rising(4)		0.01		100	ms
Twait	Time delay between Vdd_IO and Vdd(4)		0		10	ms

1. Typical specifications are not guaranteed
2. Magnetic sensor in high-resolution mode (ODR = 20 Hz), accelerometer sensor in normal mode, gyroscope in power-down mode
3. Accelerometer and magnetic sensor in power-down mode
4. Please refer to *Section 2.2.1: Recommended power-up sequence* for more details.

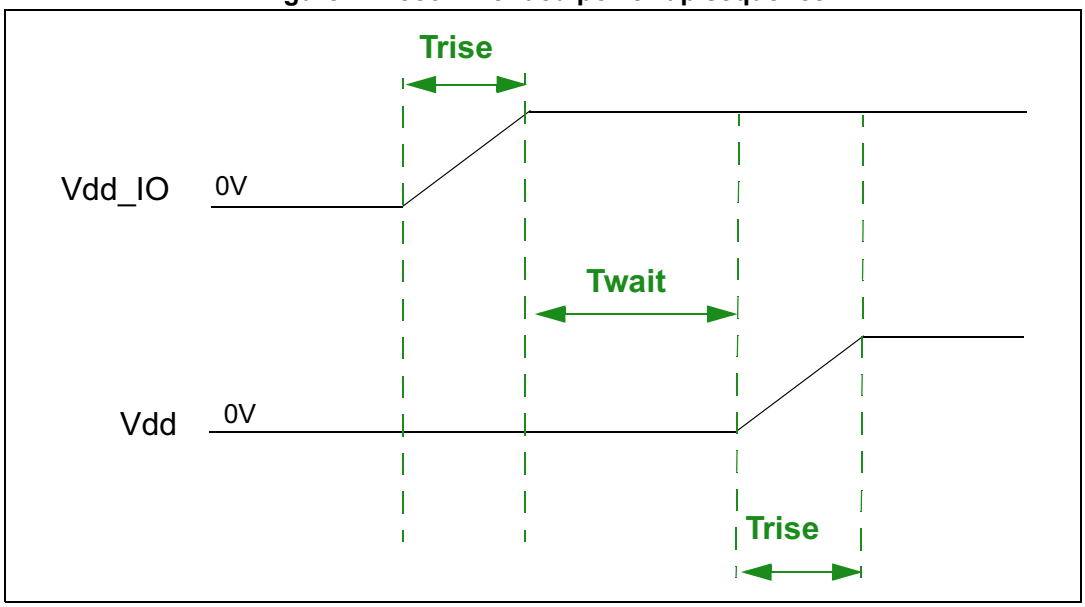
b. LSM9DS1 is factory calibrated at 2.2 V.

2.2.1 Recommended power-up sequence

For the power-up sequence please refer to the following figure, where:

- Trise is the time for the power supply to rise from 10% to 90% of its final value
- Twait is the delay between the end of the Vdd_IO ramp (90% of its final value) and the start of the Vdd ramp

Figure 2. Recommended power-up sequence



2.3 Temperature sensor characteristics

@ Vdd = 2.2 V, T = 25 °C unless otherwise noted [c]

Table 5. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
TODR	Temperature refresh rate	Gyro OFF(2)		50		Hz
		Gyro ON		59.5		
TSen	Temperature sensitivity(3)			16		LSB/°C
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. When the accelerometer ODR is set to 10 Hz and the gyroscope part is turned off, the TODR value is 10 Hz.
3. The output of the temperature sensor is 0 (typ.) at 25 °C

c. The product is factory calibrated at 2.2 V.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

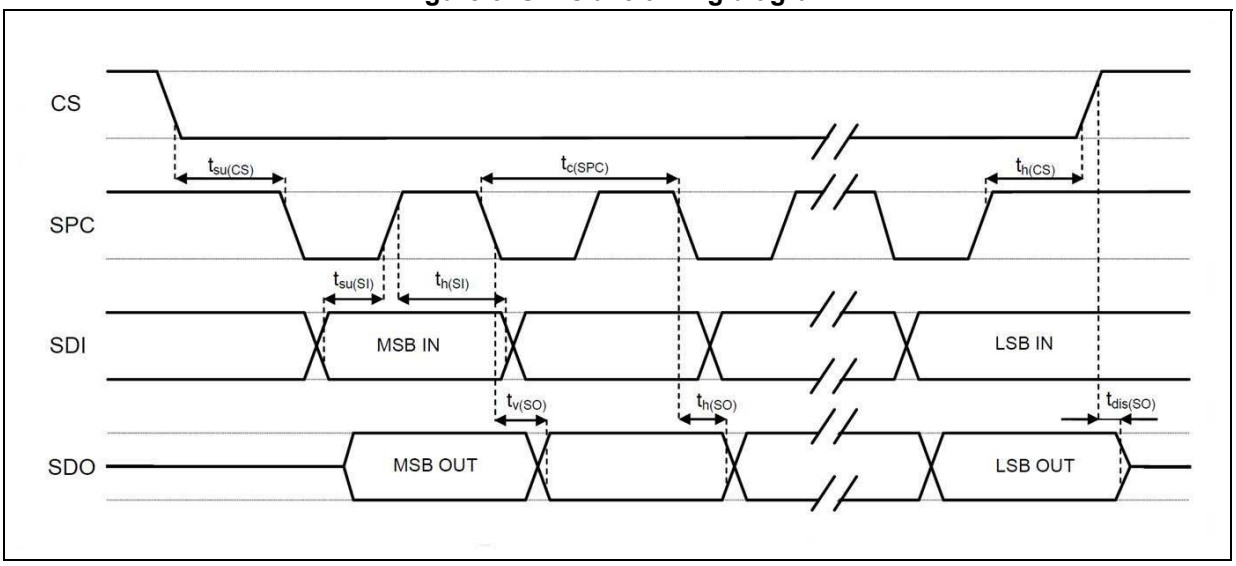
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	5		ns
$t_{h(CS)}$	CS hold time	20		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	5		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production

Figure 3. SPI slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 I²C - inter-IC control interface

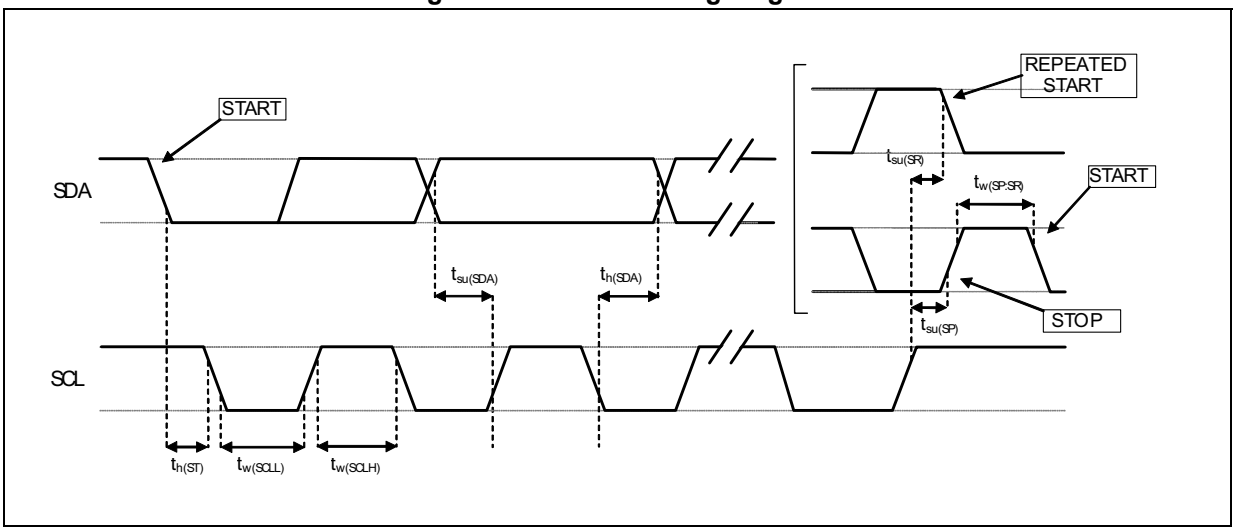
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C Standard mode(1)		I²C Fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports

2.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (including CS_A/G, CS_M, SCL/SPC, SDA/SDI/SDO, SDO_A/G, SDO_M)	0.3 to Vdd_IO +0.3	V
A_{UNP}	Acceleration (any axis)	3,000 for 0.5 ms	g
		10,000 for 0.1 ms	g
M_{EF}	Maximum exposed field	1000	gauss
ESD	Electrostatic discharge protection (HBM)	2	kV
T_{STG}	Storage temperature range	-40 to +125	°C

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

2.6 Terminology

2.6.1 Sensitivity

Linear acceleration sensitivity can be determined, for example, by applying 1 *g* acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors.

An angular rate gyroscope is device that produces a positive-going digital output for counterclockwise rotation around the axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

Magnetic sensor sensitivity describes the gain of the sensor and can be determined, for example, by applying a magnetic field of 1 *gauss* to it.

2.6.2 Zero-*g*, zero-rate and zero-*gauss* level

Linear acceleration zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on both the X-axis and Y-axis, whereas the Z-axis will measure 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-*g* offset.

Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-*g* level change vs. temperature" in *Table 3*. The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a group of sensors.

Zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

Zero-*g*auss level offset (M_TyOff) describes the deviation of an actual output signal from the ideal output if no magnetic field is present.

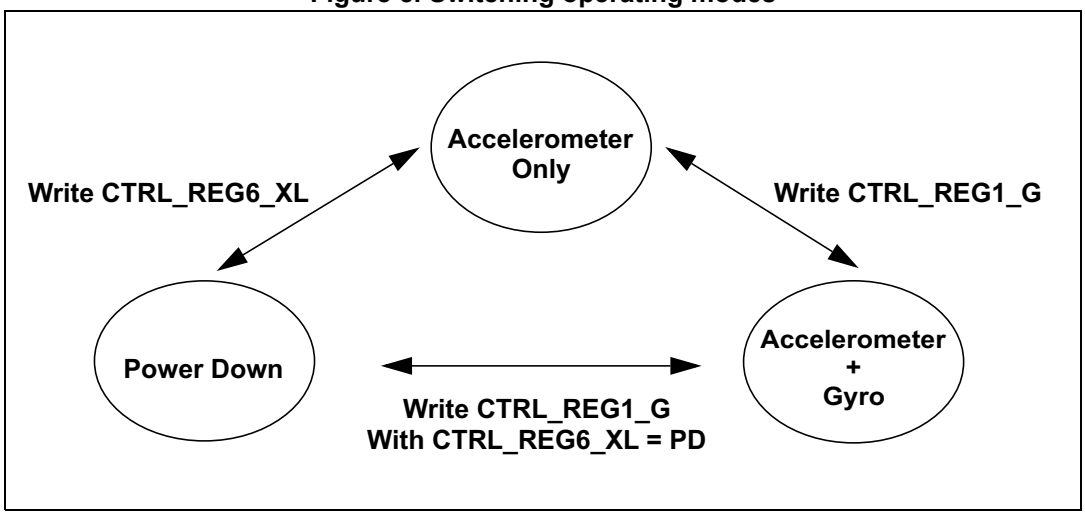
3 LSM9DS1 functionality

3.1 Operating modes

In the LSM9DS1 the accelerometer and gyroscope have two operating modes available: only accelerometer active and gyroscope in power down or both accelerometer and gyroscope sensors active at the same ODR. Switching from one mode to the other requires one write operation: writing to *CTRL_REG6_XL (20h)*, the accelerometer operates in normal mode and the gyroscope is powered down, writing to *CTRL_REG1_G (10h)* both accelerometer and gyroscope are activated at the same ODR.

Figure 5 depicts both modes of operation from power down.

Figure 5. Switching operating modes



The magnetic sensor has three operating modes available: power-down (default), continuous-conversion mode and single-conversion mode. Switching from power-down to the other modes requires one write operation to *CTRL_REG3_M (22h)*, setting values in the MD[1:0] bits. For the output of the magnetic data compensated by temperature, the TEMP_COMP bit in *CTRL_REG1_M (20h)* must be set to '1'.

3.2 Gyroscope power modes

In the LSM9DS1, the gyroscope can be configured in three different operating modes: power-down, low-power and normal mode.

Low-power mode is available for lower ODR (14.9, 59.5, 119 Hz) while for greater ODR (238, 476, 952 Hz) the device is automatically in normal mode. *Table* summarizes the ODR configuration (ODR_G[2:0] bits set in *CTRL_REG1_G (10h)*) and corresponding power modes.

To enable low-power mode, the LP_mode bit in *CTRL_REG3_G (12h)* has to be set to '1'.

Low-power mode allows reaching low power consumption while maintaining the device always on, refer to *Table 10*.

Table 9. Gyroscope operating modes

ODR_G [2:0]	ODR [Hz]	Power mode
000	Power down	Power-down
001	14.9	Low-power/Normal mode
010	59.5	Low-power/Normal mode
011	119	Low-power/Normal mode
100	238	Normal mode
101	476	Normal mode
110	952	Normal mode

Table 10. Operating mode current consumption

ODR [Hz]	Power mode	Current consumption(1) [mA]
14.9	Low-power	1.9
59.5	Low-power	2.4
119	Low-power	3.1
238	Normal mode	4.3
476	Normal mode	4.3
952	Normal mode	4.3

1. Typical values of gyroscope and accelerometer current consumption are based on characterization data.

Table 11. Accelerometer turn-on time

ODR [Hz]	BW = 400 Hz(1)	BW = 200 Hz(1)	BW = 100 Hz(1)	BW = 50 Hz(1)
14.9	0	0	0	0
59.5	0	0	0	0
119	1	1	1	2
238	1	1	2	4
476	1	2	4	7
952	2	4	7	14

1. The table contains the number of samples to be discarded after switching between power-down mode and normal mode.

Table 12. Gyroscope turn-on time

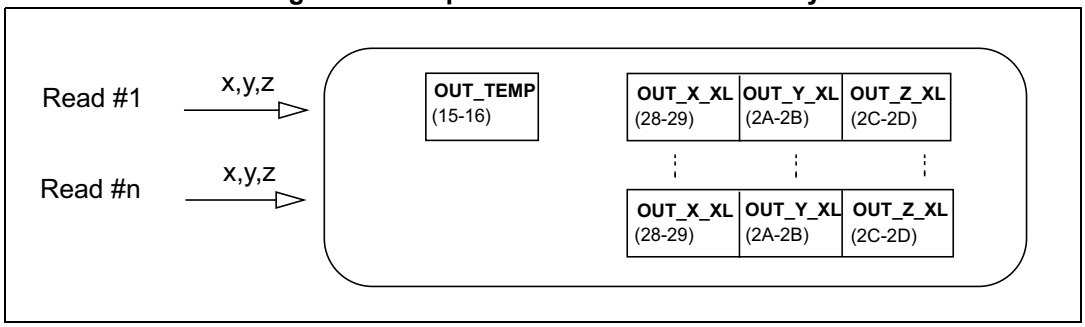
ODR [Hz]	LPF1 only(1)	LPF1 and LPF2(1)
14.9	2	LPF2 not available
59.5 or 119	3	13
238	4	14
476	5	15
952	8	18

1. The table contains the number of samples to be discarded after switching between low-power mode and normal mode.

3.3 Accelerometer and gyroscope multiple reads (burst)

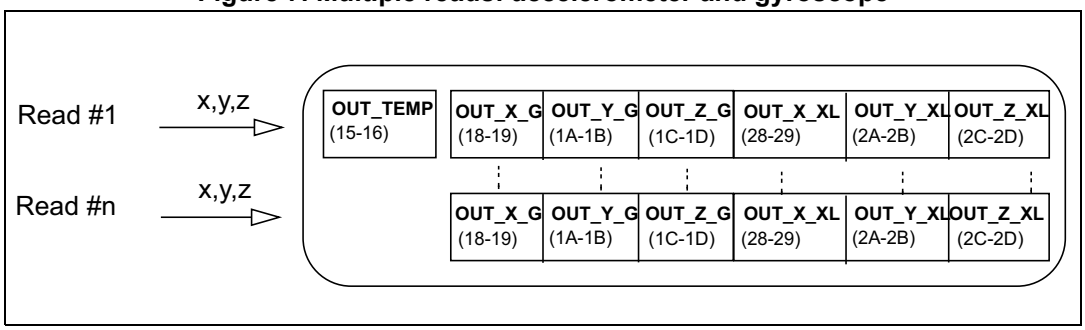
When only accelerometer is activated and the gyroscope is in power down, starting from *OUT_X_XL (28h - 29h)* multiple reads can be performed. Once *OUT_Z_XL (2Ch - 2Dh)* is read, the system automatically restarts from *OUT_X_XL (28h - 29h)* (see *Figure 6*).

Figure 6. Multiple reads: accelerometer only



When both accelerometer and gyroscope sensors are activated at the same ODR, starting from *OUT_X_G (18h - 19h)* multiple reads can be performed. Once *OUT_Z_XL (2Ch - 2Dh)* is read, the system automatically restarts from *OUT_X_G (18h - 19h)* (see *Figure 7*).

Figure 7. Multiple reads: accelerometer and gyroscope



3.4 Block diagram

Figure 8. Accelerometer and gyroscope digital block diagram

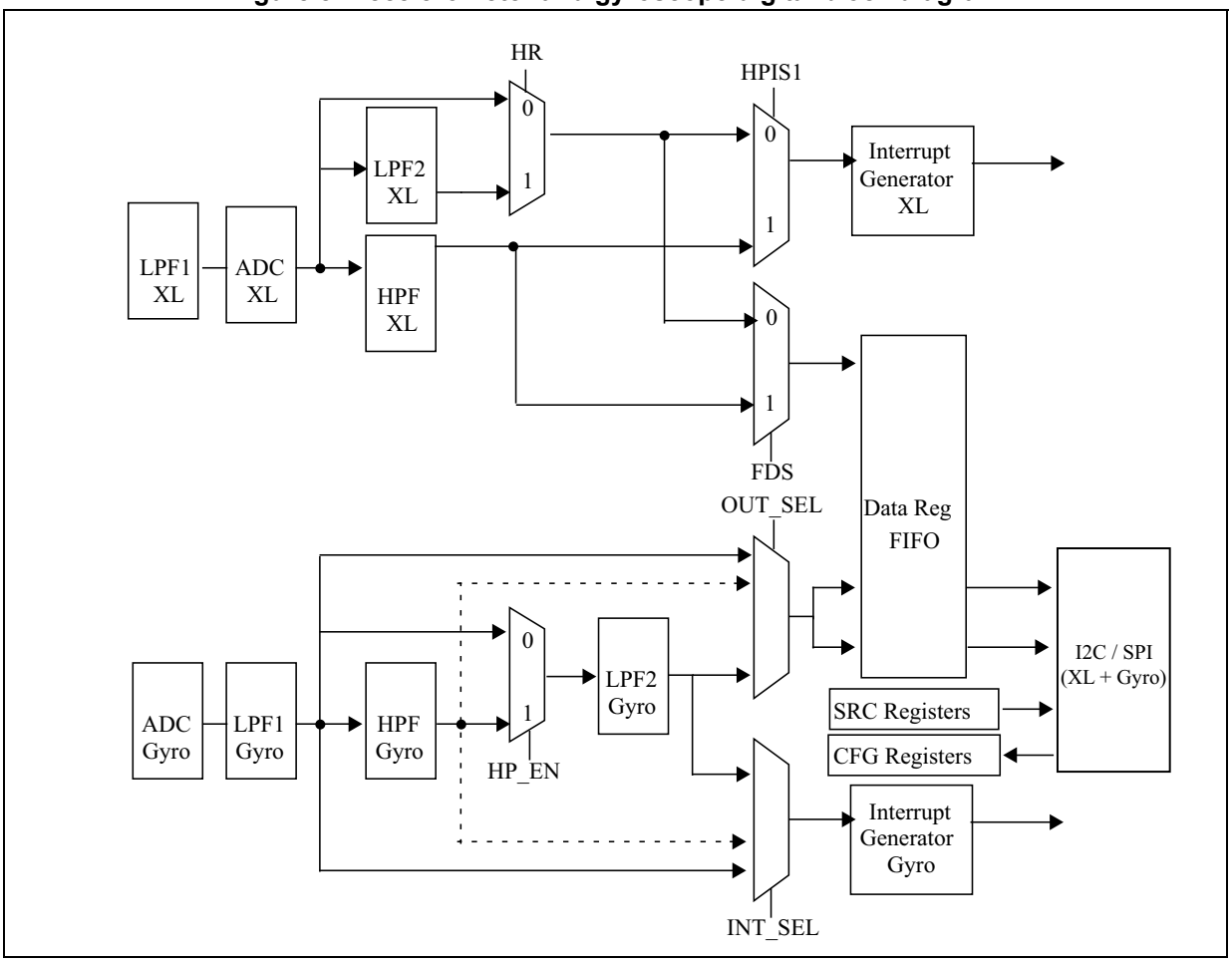
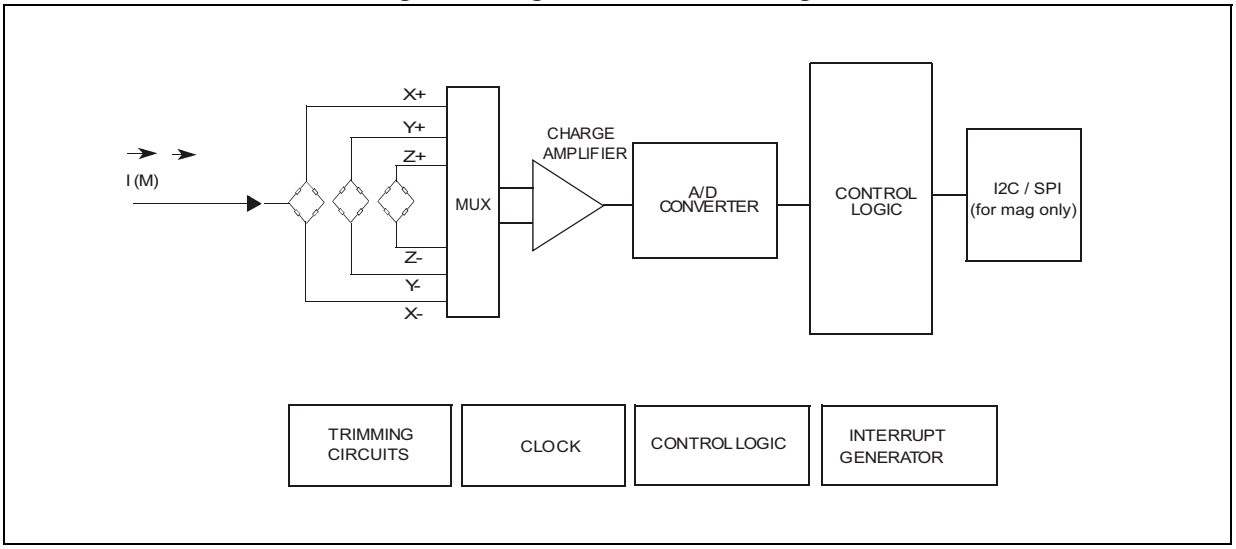


Figure 9. Magnetometer block diagram



3.5 Accelerometer and gyroscope FIFO

The LSM9DS1 embeds 32 slots of 16-bit data FIFO for each of the gyroscope's three output channels, yaw, pitch and roll, and 16-bit data FIFO for each of the accelerometer's three output channels, X, Y and Z. This allows consistent power saving for the system since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work accordingly to five different modes: Bypass mode, FIFO-mode, Continuous mode, Continuous-to-FIFO mode and Bypass-to-Continuous. Each mode is selected by the FMODE [2:0] bits in the *FIFO_CTRL (2Eh)* register. Programmable FIFO threshold status, FIFO overrun events and the number of unread samples stored are available in the *FIFO_SRC (2Fh)* register and can be set to generate dedicated interrupts on the INT1_A/G pin in the *INT1_CTRL (0Ch)* register and on the INT2_A/G pin in the *INT2_CTRL (0Dh)* register.

FIFO_SRC (2Fh)(FTH) goes to '1' when the number of unread samples (*FIFO_SRC (2Fh)* (FSS5:0)) is greater than or equal to FTH [4:0] in *FIFO_CTRL (2Eh)*. If *FIFO_CTRL (2Eh)* (FTH[4:0]) is equal to 0, *FIFO_SRC (2Fh)*(FTH) goes to '0'.

FIFO_SRC (2Fh)(OVRN) is equal to '1' if a FIFO slot is overwritten.

FIFO_SRC (2Fh)(FSS [5:0]) contains stored data levels of unread samples. When FSS [5:0] is equal to '000000' FIFO is empty, when FSS [5:0] is equal to '100000' FIFO is full and the unread samples are 32.

The FIFO feature is enabled by writing '1' in *CTRL_REG9 (23h)* (FIFO_EN).

To guarantee the correct acquisition of data during the switching into and out of FIFO mode, the first sample acquired must be discarded.

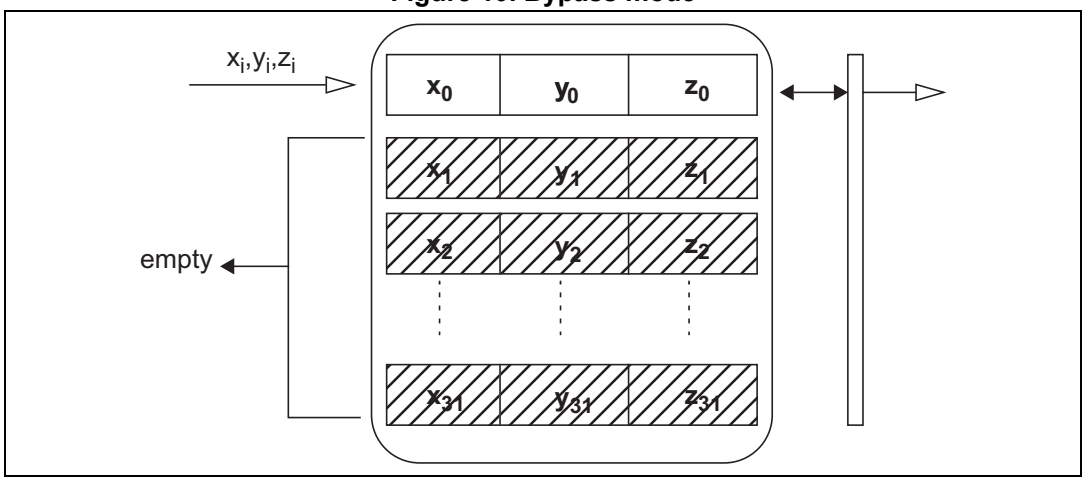
3.5.1 Bypass mode

In Bypass mode (*FIFO_CTRL (2Eh)*(FMODE [2:0]= 000), the FIFO is not operational and it remains empty.

Bypass mode is also used to reset the FIFO when in FIFO mode.

As described in *Figure 10*, for each channel only the first address is used. When new data is available the old data is overwritten.

Figure 10. Bypass mode



3.5.2 FIFO mode

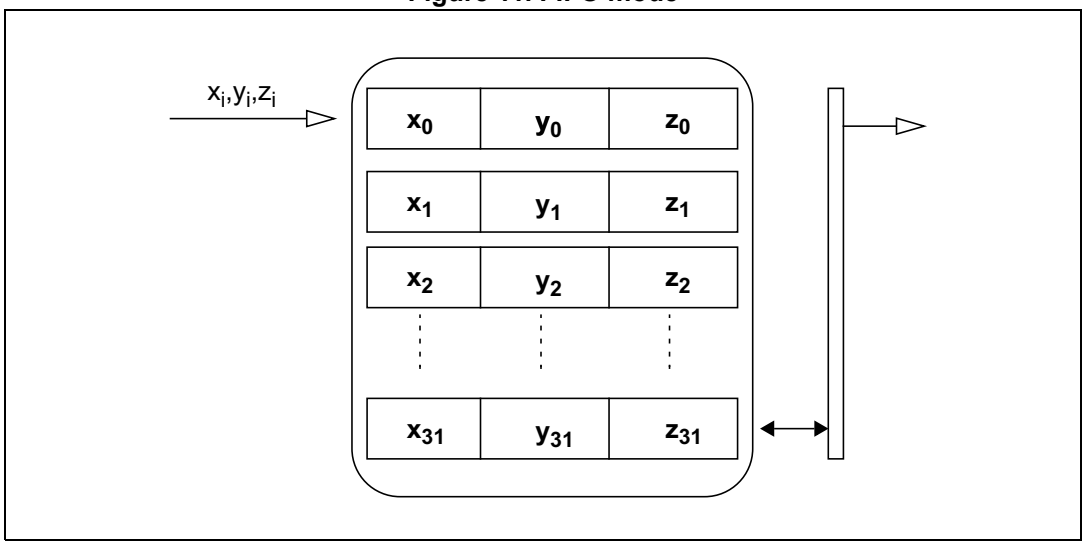
In FIFO mode (*FIFO_CTRL (2Eh)* (FMODE [2:0] = 001) data from the output channels are stored in the FIFO until it is overwritten.

To reset FIFO content, Bypass mode should be selected by writing *FIFO_CTRL (2Eh)* (FMODE [2:0]) to '000'. After this reset command, it is possible to restart FIFO mode by writing *FIFO_CTRL (2Eh)* (FMODE [2:0]) to '001'.

The FIFO buffer memorizes 32 levels of data but the depth of the FIFO can be resized by setting the STOP_ON_FTH bit in *CTRL_REG9 (23h)*. If the STOP_ON_FTH bit is set to '1', FIFO depth is limited to *FIFO_CTRL (2Eh)*(FTH [4:0]) + 1 data.

A FIFO threshold interrupt can be enabled (INT_OVR bit in *INT1_CTRL (0Ch)*) in order to be raised when the FIFO is filled to the level specified by the FTH[4:0] bits of *FIFO_CTRL (2Eh)*. When a FIFO threshold interrupt occurs, the first data has been overwritten and the FIFO stops collecting data from the input channels.

Figure 11. FIFO mode



3.5.3 Continuous mode

Continuous mode (*FIFO_CTRL (2Eh)*(FMODE[2:0] = 110) provides continuous FIFO update: as new data arrives the older is discarded.

A FIFO threshold flag *FIFO_SRC (2Fh)*(FTH) is asserted when the number of unread samples in FIFO is greater than or equal to *FIFO_CTRL (2Eh)*(FTH4:0).

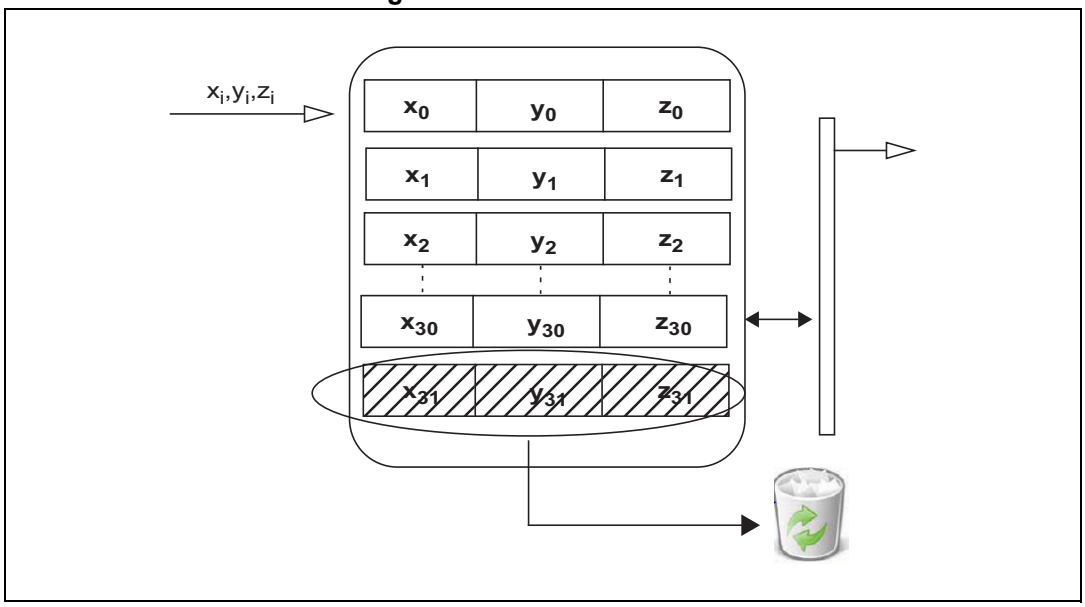
It is possible to route *FIFO_SRC (2Fh)*(FTH) to the INT1_A/G pin by writing in register *INT1_CTRL (0Ch)* (INT1_FTH) = '1', or to the INT2_A/G pin by writing in register *INT2_CTRL (0Dh)* (INT2_FTH) = '1'.

A full-flag interrupt can be enabled, (*INT1_CTRL (0Ch)* (INT_ FSS5)= '1') when the FIFO becomes saturated and in order to read the contents all at once.

If an overrun occurs, the oldest sample in FIFO is overwritten and the OVRN flag in *FIFO_SRC (2Fh)* is asserted.

In order to empty the FIFO before it is full it is also possible to pull from FIFO the number of unread samples available in *FIFO_SRC (2Fh)* (FSS[5:0]).

Figure 12. Continuous mode



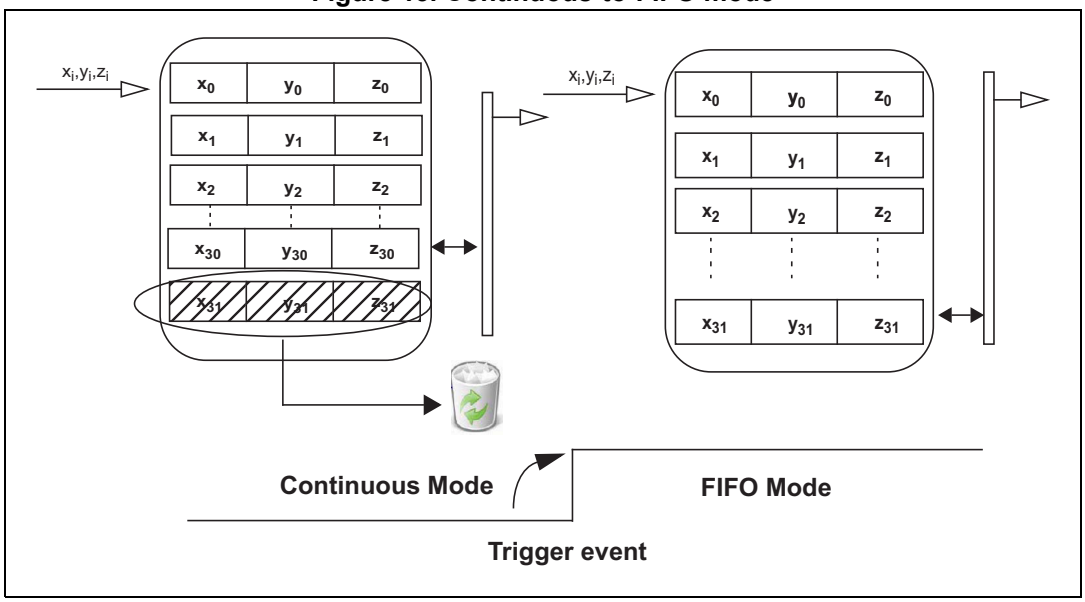
3.5.4 Continuous-to-FIFO mode

In Continuous-to-FIFO mode (*FIFO_CTRL (2Eh)*(FMODE [2:0] = 011), FIFO behavior changes according to the *INT_GEN_SRC_XL (26h)*(IA_XL) bit. When the *INT_GEN_SRC_XL (26h)*(IA_XL) bit is equal to '1', FIFO operates in FIFO-mode, when the *INT_GEN_SRC_XL (26h)*(IA_XL) bit is equal to '0', FIFO operates in Continuous mode.

The interrupt generator should be set to the desired configuration by means of *INT_GEN_CFG_XL (06h)*, *INT_GEN_THS_X_XL (07h)*, *INT_GEN_THS_Y_XL (08h)* and *INT_GEN_THS_Z_XL (09h)*.

The *CTRL_REG4 (1Eh)*(LIR_XL) bit should be set to '1' in order to have latched interrupt.

Figure 13. Continuous-to-FIFO mode



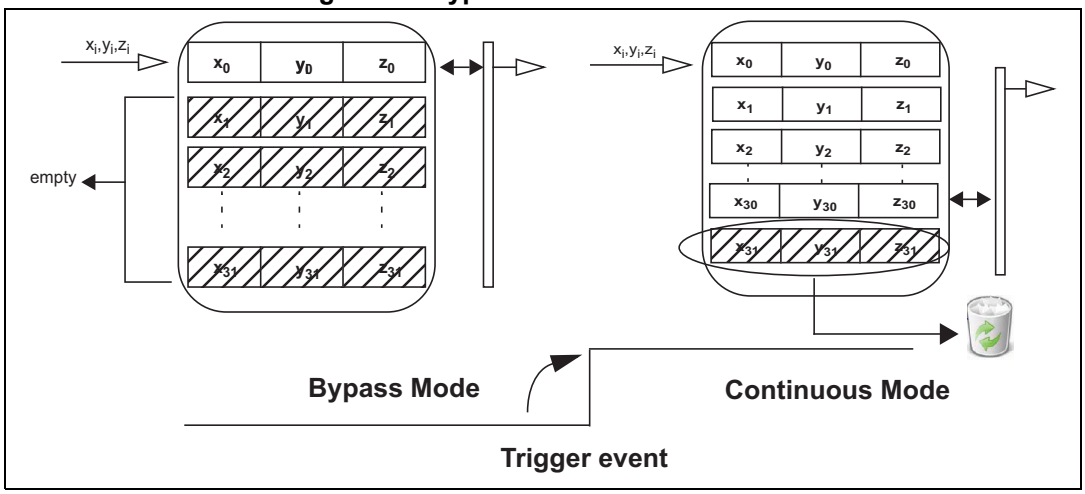
3.5.5 Bypass-to-Continuous mode

In Bypass-to-Continuous mode (*FIFO_CTRL (2Eh)*(FMODE[2:0] = '100'), data measurement storage inside FIFO operates in Continuous mode when *INT_GEN_SRC_XL (26h)*(IA_XL) is equal to '1', otherwise FIFO content is reset (Bypass mode).

The interrupt generator should be set to the desired configuration by means of *INT_GEN_CFG_XL (06h)*, *INT_GEN_THS_X_XL (07h)*, *INT_GEN_THS_Y_XL (08h)* and *INT_GEN_THS_Z_XL (09h)*.

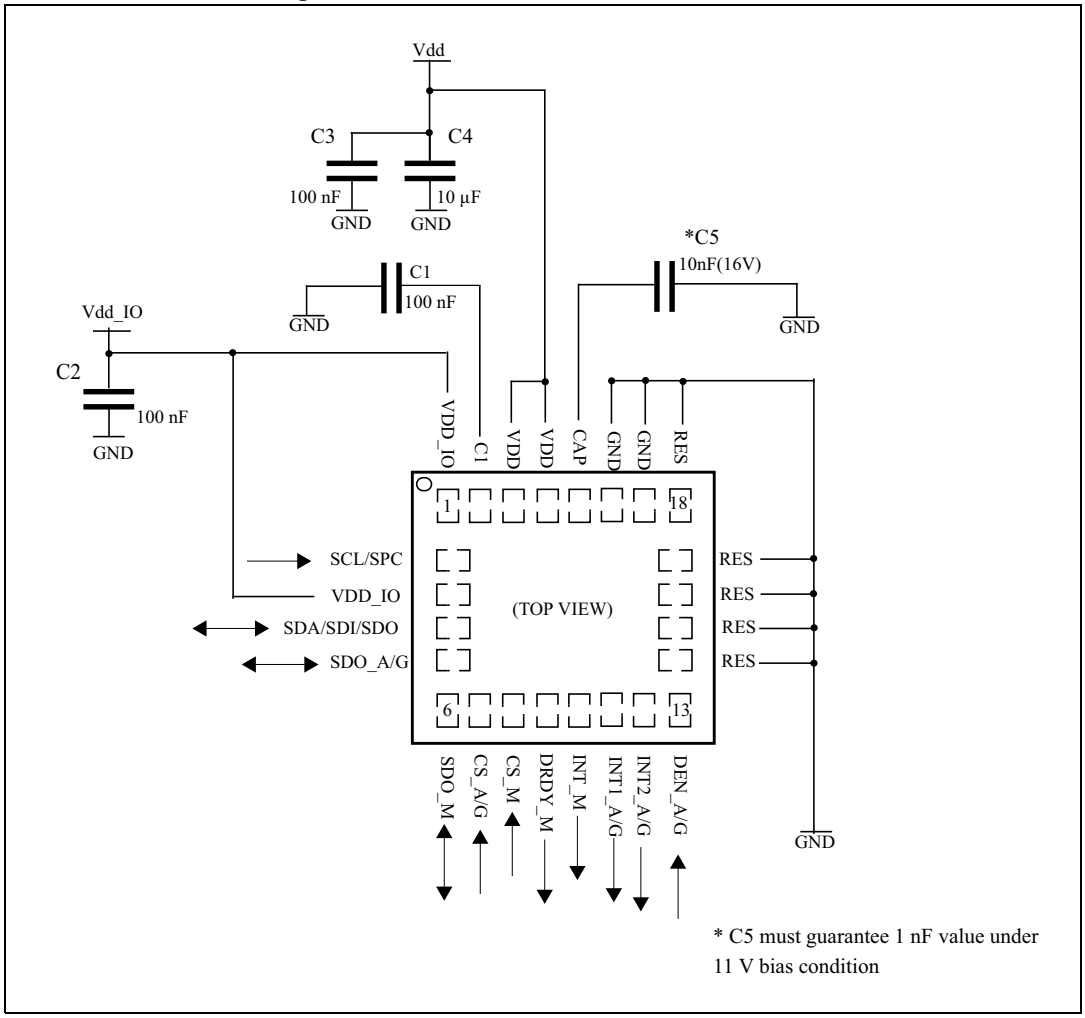
The *CTRL_REG4 (1Eh)*(LIR_XL) bit should be set to '1' in order to have latched interrupt.

Figure 14. Bypass-to-Continuous mode



4 Application hints

Figure 15. LSM9DS1 electrical connections



4.1 External capacitors

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C2, C3 = 100 *nF* ceramic, C4 = 10 *µF* Al) should be placed as near as possible to the supply pin of the device (common design practice). Capacitor C1 (100 nF) should be a capacitor with low ESR value and should be placed as near as possible to the C1 pin.

All voltage and ground supplies must be present at the same time to achieve proper behavior of the IC (refer to *Figure 15*).

5 Digital interfaces

The registers embedded inside the LSM9DS1 may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pins. To select/exploit the I^2C interface, the CS line must be tied high (i.e connected to Vdd_IO).

Table 13. Serial interface pin description

Pin name	Pin description
CS_A/G, CS_M	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
SCL/SPC	I^2C Serial Clock (SCL) SPI Serial Port Clock (SPC)
SDA/SDI/SDO	I^2C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO)
SDO_A/G, SDO_M	SPI Serial Data Output (SDO) I^2C less significant bit of the device address

5.1 I^2C serial interface

The LSM9DS1 I^2C is a bus slave. The I^2C is employed to write the data to the registers, whose content can also be read back.

The relevant I^2C terminology is provided in the table below.

Table 14. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the Serial DAta line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through an external pull-up resistor. When the bus is free, both the lines are high.

The I^2C interface is implemented with fast mode (400 kHz) I^2C standards as well as with the standard mode.

In order to disable the I^2C block for accelerometer and gyroscope the I2C_DISABLE bit must be written to ‘1’ in *CTRL_REG9 (23h)*, while for magnetometer the I2C_DISABLE bit must be written to ‘1’ in *CTRL_REG3_M (22h)*.

5.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a high-to-low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LSM9DS1 behaves like a slave device and the following protocol must be adhered to. In the I²C of the accelerometer and gyroscope sensor, after the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted. The 7 LSb represent the actual register address while the *CTRL_REG8 (22h)* (IF_ADD_INC) bit defines the address increment. In the I²C of the magnetometer sensor, after the START condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted. The 7 LSb represent the actual register address while the MSB enables the address auto increment. The SUB (register address) is automatically increased to allow multiple data read/write.

Table 15. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 16. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 17. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 18. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed

some other function, it can hold the clock line, SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low-to-high transition on the SDA line while the SCL line is high is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In the presented communication format MAK is Master acknowledge and NMAK is No Master Acknowledge.

Default address:

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes. If the bit is '0' (Write) the master will transmit to the slave with direction unchanged. *Table 19* and *Table 20* explain how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 19. Accelerometer and gyroscope SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

Table 20. Magnetic sensor SAD+Read/Write patterns

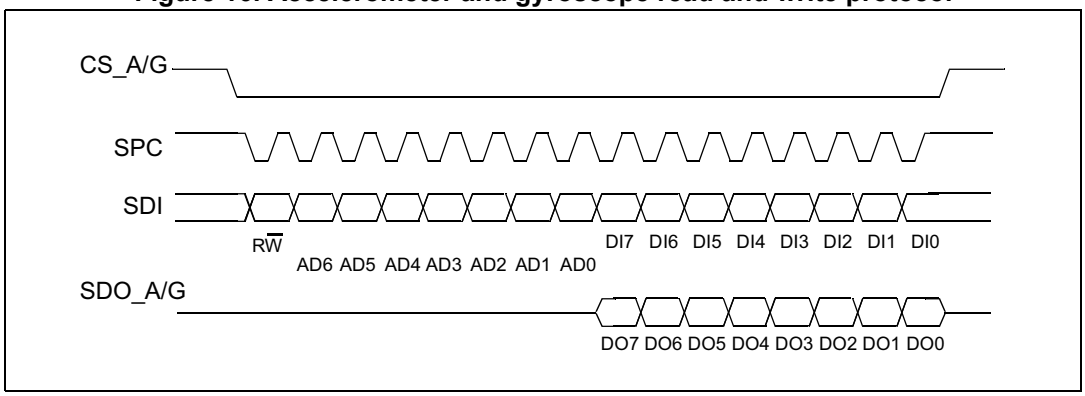
Command	SAD[6:2]	SAD[1] = SDO/SA1	SAD[0]	R/W	SAD+R/W
Read	00111	0	0	1	00111001 (39h)
Write	00111	0	0	0	00111000 (38h)
Read	00111	1	0	1	00111101 (3Dh)
Write	00111	1	0	0	00111100 (3Ch)

5.2 Accelerometer and gyroscope SPI bus interface

The LSM9DS1 accelerometer and gyroscope SPI is a bus slave. The SPI allows to write and read the registers of the device.

The Serial Interface connects to applications using 4 wires: **CS_A/G**, **SPC**, **SDI** and **SDO_A/G**.

Figure 16. Accelerometer and gyroscope read and write protocol



CS_A/G is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS_A/G** is high (no transmission). **SDI** and **SDO_A/G** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS_A/G** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS_A/G**.

bit 0: $\overline{RW}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO_A/G** at the start of bit 8.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

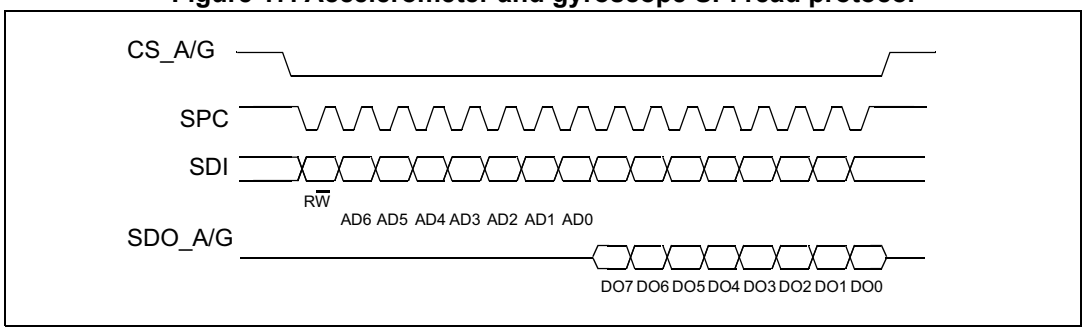
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When the *CTRL_REG8 (22h)* (IF_ADD_INC) bit is '0' the address used to read/write data remains the same for every block. When the *CTRL_REG8 (22h)*(IF_ADD_INC) bit is '1', the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO_A/G** remain unchanged.

5.2.1 SPI read

Figure 17. Accelerometer and gyroscope SPI read protocol



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

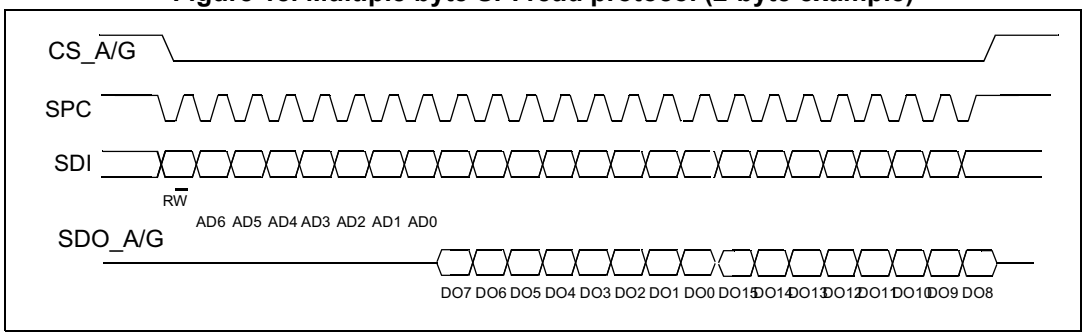
bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

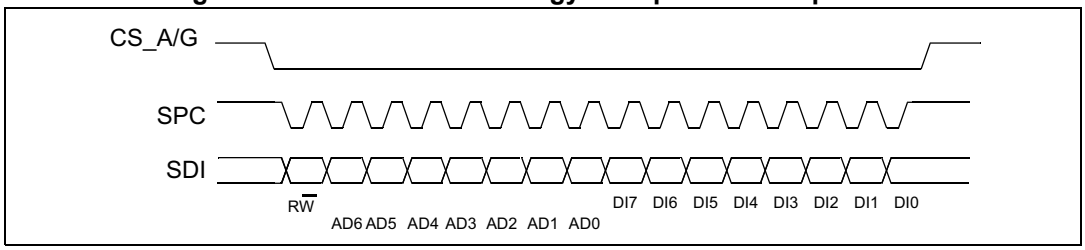
bit 16-... : data DO(...-8). Further data in multiple byte reads.

Figure 18. Multiple byte SPI read protocol (2-byte example)



5.2.2 SPI write

Figure 19. Accelerometer and gyroscope SPI write protocol



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

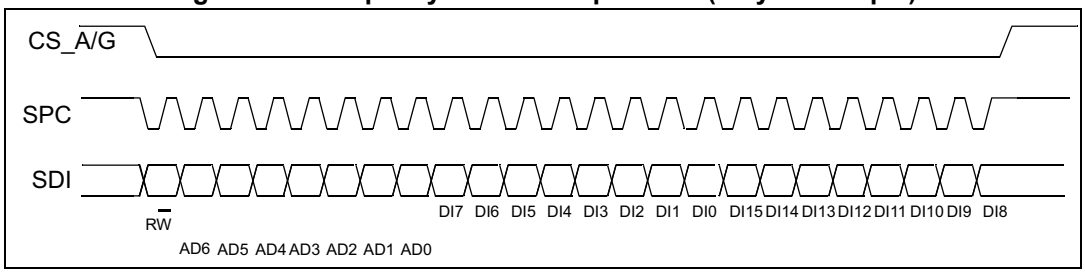
bit 0: WRITE bit. The value is 0.

bit 1 -7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

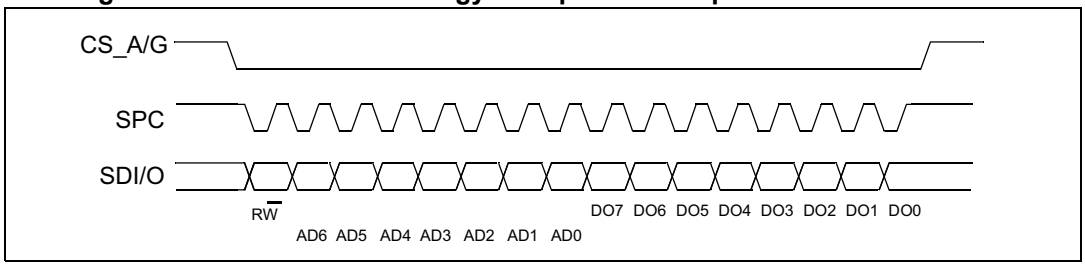
Figure 20. Multiple byte SPI write protocol (2-byte example)



5.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the *CTRL_REG8 (22h)*(SIM) bit equal to ‘1’ (SPI serial interface mode selection).

Figure 21. Accelerometer and gyroscope SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

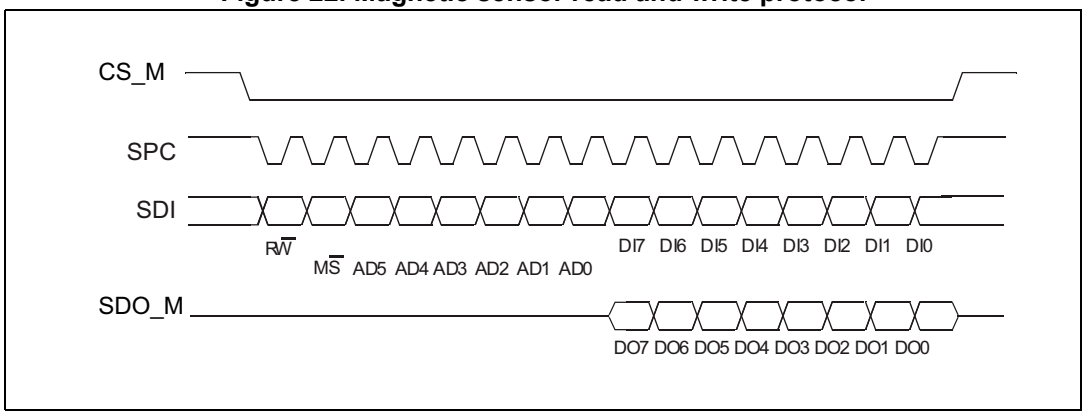
A multiple read command is also available in 3-wire mode.

5.3 Magnetic sensor SPI bus interface

The LSM9DS1 magnetic sensor SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface connects to applications using 4 wires: **CS_M**, **SPC**, **SDI** and **SDO_M**.

Figure 22. Magnetic sensor read and write protocol



CS_M is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS_M** is high (no transmission). **SDI** and **SDO_M** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS_M** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS_M**.

bit 0: $\overline{RW}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO_M** at the start of bit 8.

bit 1: $\overline{MS}$ bit. When 0, the address will remain unchanged in multiple read/write commands. When 1, the address is auto-incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

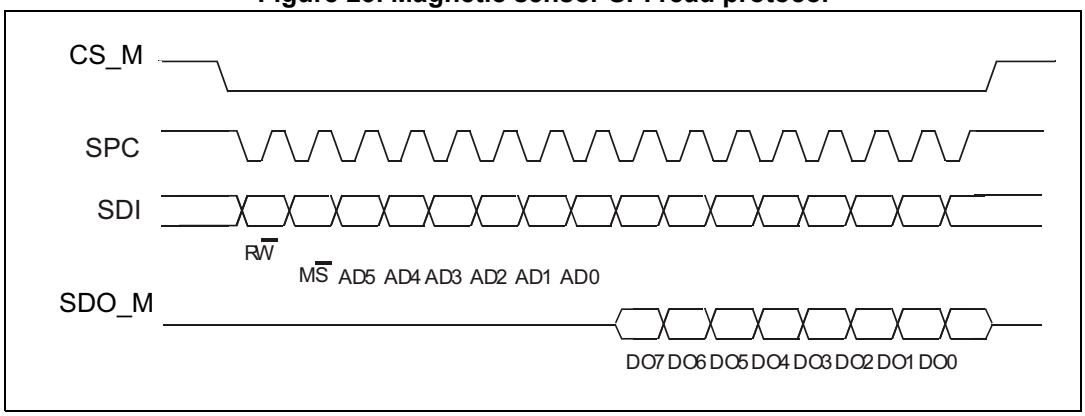
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When the $\overline{MS}$ bit is '0', the address used to read/write data remains the same for every block. When the $\overline{MS}$ bit is '1', the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO_M** remain unchanged.

5.3.1 SPI read

Figure 23. Magnetic sensor SPI read protocol



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: READ bit. The value is 1.

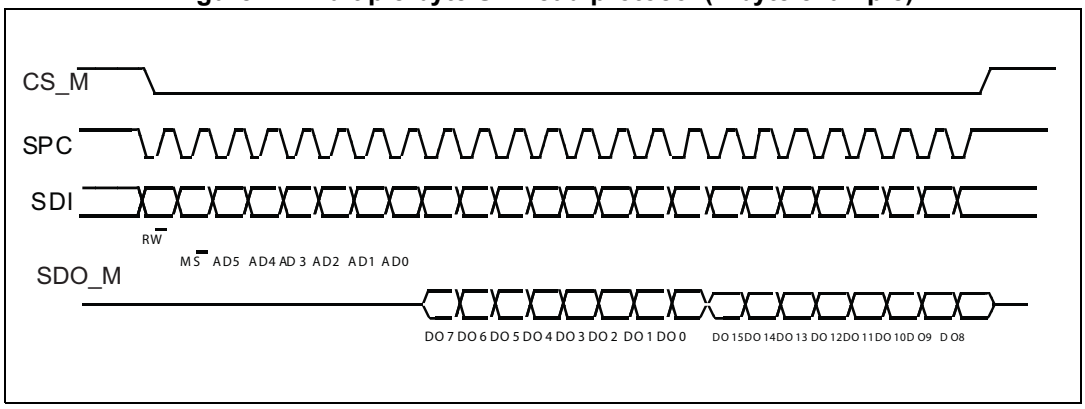
bit 1: MS bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

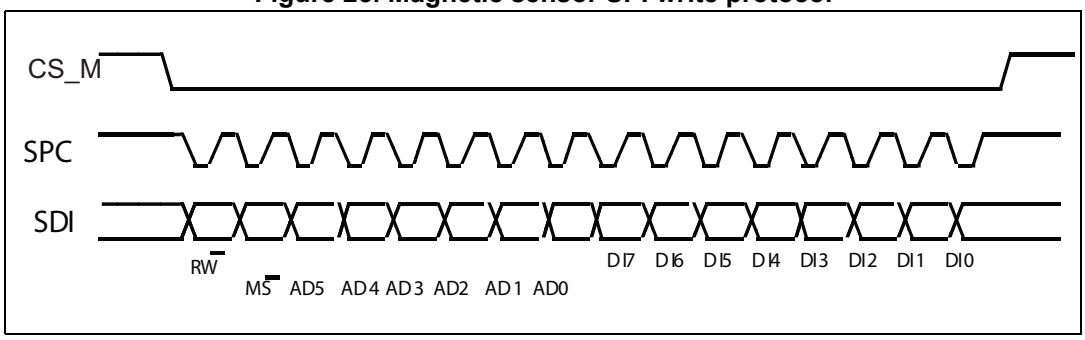
bit 16-... : data DO(...-8). Further data in multiple byte reads.

Figure 24. Multiple byte SPI read protocol (2-byte example)



5.3.2 SPI write

Figure 25. Magnetic sensor SPI write protocol



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

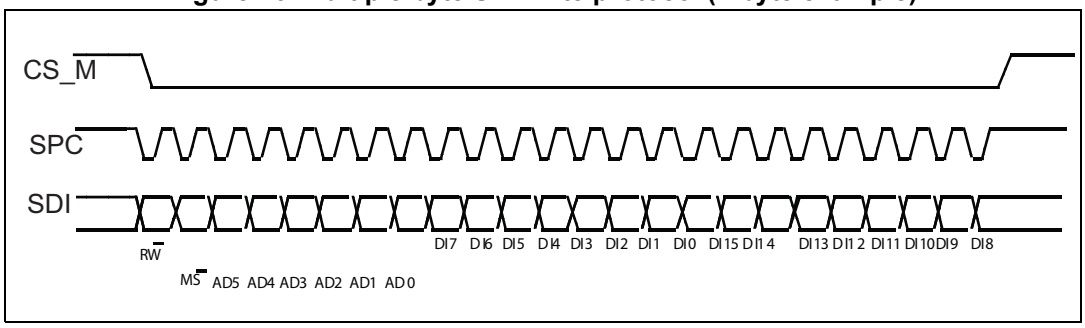
bit 1: $\overline{MS}$ bit. When 0, does not increment the address; when 1, increments the address in multiple writes.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

Figure 26. Multiple byte SPI write protocol (2-byte example)

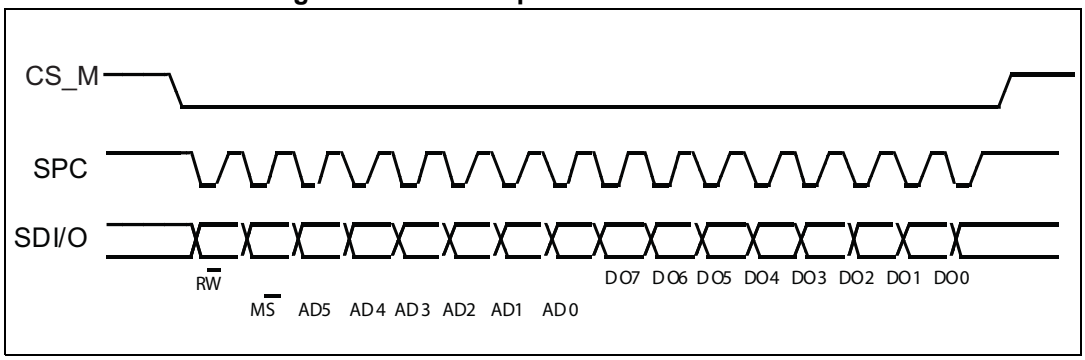


5.3.3 SPI read in 3-wire mode

3-wire mode is entered by setting the SIM bit to '1' (SPI serial interface mode selection) in *CTRL_REG3_M (22h)*.

When 3-wire mode is used, the SDO_M pin has to be connected to GND or Vdd_IO.

Figure 27. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: $\overline{MS}$ bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

6 Register mapping

The table given below provides a list of the 8/16-bit registers embedded in the device and the corresponding addresses.

Table 21. Accelerometer and gyroscope register address map

Name	Type	Register address		Default	Note
		Hex	Binary		
Reserved	--	00-03	--	--	Reserved
ACT_THS	r/w	04	00000100	00000000	
ACT_DUR	r/w	05	00000101	00000000	
INT_GEN_CFG_XL	r/w	06	00000110	00000000	
INT_GEN_THS_X_XL	r/w	07	00000111	00000000	
INT_GEN_THS_Y_XL	r/w	08	00001000	00000000	
INT_GEN_THS_Z_XL	r/w	09	00001001	00000000	
INT_GEN_DUR_XL	r/w	0A	00001010	00000000	
REFERENCE_G	r/w	0B	00001011	00000000	
INT1_CTRL	r/w	0C	00001100	00000000	
INT2_CTRL	r/w	0D	00001101	00000000	
Reserved	--	0E	--	--	Reserved
WHO_AM_I	r	0F	00001111	01101000	
CTRL_REG1_G	r/w	10	00010000	00000000	
CTRL_REG2_G	r/w	11	00010001	00000000	
CTRL_REG3_G	r/w	12	00010010	00000000	
ORIENT_CFG_G	r/w	13	00010011	00000000	
INT_GEN_SRC_G	r	14	00010100	output	
OUT_TEMP_L	r	15	00010101	output	
OUT_TEMP_H	r	16	00010110	output	
STATUS_REG	r	17	00010111	output	
OUT_X_L_G	r	18	00011000	output	
OUT_X_H_G	r	19	00011001	output	
OUT_Y_L_G	r	1A	00011010	output	
OUT_Y_H_G	r	1B	00011011	output	
OUT_Z_L_G	r	1C	00011100	output	
OUT_Z_H_G	r	1D	00011101	output	
CTRL_REG4	r/w	1E	00011110	00111000	
CTRL_REG5_XL	r/w	1F	00011111	00111000	

Table 21. Accelerometer and gyroscope register address map (continued)

Name	Type	Register address		Default	Note
		Hex	Binary		
CTRL_REG6_XL	r/w	20	00100000	00000000	
CTRL_REG7_XL	r/w	21	00100001	00000000	
CTRL_REG8	r/w	22	00100010	00000100	
CTRL_REG9	r/w	23	00100011	00000000	
CTRL_REG10	r/w	24	00100100	00000000	
Reserved	--	25	--	--	Reserved
INT_GEN_SRC_XL	r	26	00100110	output	
STATUS_REG	r	27	00100111	output	
OUT_X_L_XL	r	28	00101000	output	
OUT_X_H_XL	r	29	00101001	output	
OUT_Y_L_XL	r	2A	00101010	output	
OUT_Y_H_XL	r	2B	00101011	output	
OUT_Z_L_XL	r	2C	00101100	output	
OUT_Z_H_XL	r	2D	00101101	output	
FIFO_CTRL	r/w	2E	00101110	00000000	
FIFO_SRC	r	2F	00101111	output	
INT_GEN_CFG_G	r/w	30	00110000	00000000	
INT_GEN_THS_XH_G	r/w	31	00110001	00000000	
INT_GEN_THS_XL_G	r/w	32	00110010	00000000	
INT_GEN_THS_YH_G	r/w	33	00110011	00000000	
INT_GEN_THS_YL_G	r/w	34	00110100	00000000	
INT_GEN_THS_ZH_G	r/w	35	00110101	00000000	
INT_GEN_THS_ZL_G	r/w	36	00110110	00000000	
INT_GEN_DUR_G	r/w	37	00110111	00000000	
Reserved	r	38-7F	--	--	Reserved

Table 22. Magnetic sensor register address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
Reserved		00 - 04	--	--	Reserved
OFFSET_X_REG_L_M	r/w	05		00000000	Offset in order to compensate environmental effects
OFFSET_X_REG_H_M	r/w	06		00000000	
OFFSET_Y_REG_L_M	r/w	07		00000000	
OFFSET_Y_REG_H_M	r/w	08		00000000	
OFFSET_Z_REG_L_M	r/w	09		00000000	
OFFSET_Z_REG_H_M	r/w	0A		00000000	
Reserved		0B - 0E	--	--	Reserved
WHO_AM_I_M	r	0F	0000 1111	00111101	Magnetic Who I am ID
Reserved		10 - 1F	--	--	Reserved
CTRL_REG1_M	r/w	20	0010 0000	00010000	Magnetic control registers
CTRL_REG2_M	r/w	21	0010 0001	00000000	
CTRL_REG3_M	r/w	22	0010 0010	00000011	
CTRL_REG4_M	r/w	23	0010 0011	00000000	
CTRL_REG5_M	r/w	24	0010 0100	00000000	
Reserved		25 - 26	--	--	Reserved
STATUS_REG_M	r	27	0010 0111	Output	
OUT_X_L_M	r	28	0010 1000	Output	Magnetic output registers
OUT_X_H_M	r	29	0010 1001	Output	
OUT_Y_L_M	r	2A	0010 1010	Output	
OUT_Y_H_M	r	2B	0010 1011	Output	
OUT_Z_L_M	r	2C	0010 1100	Output	
OUT_Z_H_M	r	2D	0010 1101	Output	
Reserved	r	2E-2F	--	--	Reserved
INT_CFG_M	rw	30	00110000	00001000	Magnetic interrupt configuration register
INT_SRC_M	r	31	00110001	00000000	Magnetic interrupt generator status register
INT_THS_L_M	r	32	00110010	00000000	Magnetic interrupt generator threshold
INT_THS_H_M	r	33	00110011	00000000	

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

To guarantee proper behavior of the device, all registers addresses not listed in the above table must not be accessed and the content stored on those registers must not be changed.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

7 Accelerometer and gyroscope register description

The device contains a set of registers which are used to control its behavior and to retrieve linear acceleration, angular rate and temperature data. The register addresses, made up of 7 bits, are used to identify them and to write the data through the serial interface.

7.1 ACT_THS (04h)

Activity threshold register.

Table 23. ACT_THS register

SLEEP_ON _INACT_EN	ACT_THS 6	ACT_THS 5	ACT_THS 4	ACT_THS 3	ACT_THS 2	ACT_TH S1	ACT_THS 0

Table 24. ACT_THS register description

SLEEP_ON_ INACT_EN	Gyroscope operating mode during inactivity. Default value: 0 (0: gyroscope in power-down; 1: gyroscope in sleep mode)
ACT_THS [6:0]	Inactivity threshold. Default value: 000 0000

7.2 ACT_DUR (05h)

Inactivity duration register.

Table 25. ACT_DUR register

ACT_DUR 7	ACT_DUR 6	ACT_DUR 5	ACT_DUR 4	ACT_DUR 3	ACT_DUR 2	ACT_DUR 1	ACT_DUR 0

Table 26. ACT_DUR register description

ACT_DUR [7:0]	Inactivity duration. Default value: 0000 0000

7.3 INT_GEN_CFG_XL (06h)

Linear acceleration sensor interrupt generator configuration register.

Table 27. INT_GEN_CFG_XL register

AOI_XL	6D	ZHIE_XL	ZLIE_XL	YHIE_XL	YLIE_XL	XHIE_XL	XLIE_XL

Table 28. INT_GEN_CFG_XL register description

AOI_XL	AND/OR combination of accelerometer's interrupt events. Default value: 0 (0: OR combination; 1: AND combination)
6D	6-direction detection function for interrupt. Default value: 0 (0: disabled; 1: enabled)
ZHIE_XL	Enable interrupt generation on accelerometer's Z-axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value higher than preset threshold)
ZLIE_XL	Enable interrupt generation on accelerometer's Z-axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value lower than preset threshold)
YHIE_XL	Enable interrupt generation on accelerometer's Y-axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value higher than preset threshold)
YLIE_XL	Enable interrupt generation on accelerometer's Y-axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value lower than preset threshold)
XHIE_XL	Enable interrupt generation on accelerometer's X-axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value higher than preset threshold)
XLIE_XL	Enable interrupt generation on accelerometer's X-axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value lower than preset threshold)

7.4 INT_GEN_THS_X_XL (07h)

Linear acceleration sensor interrupt threshold register.

Table 29. INT_GEN_THS_X_XL register

THS_XL_X7	THS_XL_X6	THS_XL_X5	THS_XL_X4	THS_XL_X3	THS_XL_X2	THS_XL_X1	THS_XL_X0

Table 30. INT_GEN_THS_X_XL register description

THS_XL_X [7:0]	X-axis interrupt threshold. Default value: 0000 0000

7.5 INT_GEN_THS_Y_XL (08h)

Linear acceleration sensor interrupt threshold register.

Table 31. INT_GEN_THS_Y_XL register

THS_XL_Y7	THS_XL_Y6	THS_XL_Y5	THS_XL_Y4	THS_XL_Y3	THS_XL_Y2	THS_XL_Y1	THS_XL_Y0

Table 32. INT_GEN_THS_Y_XL register description

THS_XL_Y [7:0]	Y-axis interrupt threshold. Default value: 0000 0000

7.6 INT_GEN_THS_Z_XL (09h)

Linear acceleration sensor interrupt threshold register.

Table 33. INT_GEN_THS_Z_XL register

THS_XL_Z 7	THS_XL_Z 6	THS_XL_Z 5	THS_XL_Z 4	THS_XL_Z 3	THS_XL_Z 2	THS_XL_Z 1	THS_XL_Z 0

Table 34. INT_GEN_THS_Z_XL register description

THS_XL_Z [7:0]	Z-axis interrupt threshold. Default value: 0000 0000

7.7 INT_GEN_DUR_XL (0Ah)

Linear acceleration sensor interrupt duration register.

Table 35. INT_GEN_DUR_XL register

WAIT_XL	DUR_XL6	DUR_XL5	DUR_XL4	DUR_XL3	DUR_XL2	DUR_XL1	DUR_XL0

Table 36. INT_GEN_DUR_XL register description

WAIT_XL	Wait function enabled on duration counter. Default value: 0 (0: wait function off; 1: wait for DUR_XL [6:0] samples before exiting interrupt)
DUR_XL [6:0]	Enter/exit interrupt duration value. Default value: 000 0000

7.8 REFERENCE_G (0Bh)

Angular rate sensor reference value register for digital high-pass filter (r/w).

Table 37. REFERENCE_G register

REF7_G	REF6_G	REF5_G	REF4_G	REF3_G	REF2_G	REF1_G	REF0_G

Table 38. REFERENCE_G register description

REF_G [7:0]	Reference value for gyroscope's digital high-pass filter (r/w). Default value: 0000 0000

7.9 INT1_CTRL (0Ch)

INT1_A/G pin control register.

Table 39. INT1_CTRL register

INT1_IG _G	INT1_IG_ XL	INT1_ FSS5	INT1_OVR	INT1_FTH	INT1_ Boot	INT1_ DRDY_G	INT1_ DRDY_XL

Table 40. INT1_CTRL register description

INT1_IG_G	Gyroscope interrupt enable on INT 1_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT_ IG_XL	Accelerometer interrupt generator on INT 1_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT_ FSS5	FSS5 interrupt enable on INT 1_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT_OVR	Overrun interrupt on INT 1_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT_FTH	FIFO threshold interrupt on INT 1_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT_ Boot	Boot status available on INT 1_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT_DRDY_G	Gyroscope data ready on INT 1_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT_DRDY_XL	Accelerometer data ready on INT 1_A/G pin. Default value: 0 (0: disabled; 1: enabled)

7.10 INT2_CTRL (0Dh)

INT2_A/G pin control register.

Table 41. INT2_CTRL register

INT2_IN ACT	0	INT2_ FSS5	INT2_OVR	INT2_FTH	INT2_ DRDY_ TEMP	INT2_ DRDY_G	INT2_ DRDY_XL

Table 42. INT2_CTRL register description

INT2_INACT	Inactivity interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
INT2_ FSS5	FSS5 interrupt enable on INT2_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT2_OVR	Overrun interrupt on INT2_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT2_FTH	FIFO threshold interrupt on INT2_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT2_ DRDY_TEMP	Temperature data ready on INT2_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT2_DRDY_G	Gyroscope data ready on INT2_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT2_DRDY_XL	Accelerometer data ready on INT2_A/G pin. Default value: 0 (0: disabled; 1: enabled)

7.11 WHO_AM_I (0Fh)

Who_AM_I register.

Table 43. WHO_AM_I register

0	1	1	0	1	0	0	0

7.12 CTRL_REG1_G (10h)

Angular rate sensor Control Register 1.

Table 44. CTRL_REG1_G register

ODR_G2	ODR_G1	ODR_G0	FS_G1	FS_G0	0(1)	BW_G1	BW_G0

1. This bit must be set to '0' for the correct operation of the device.

Table 45. CTRL_REG1_G register description

ODR_G [2:0]	Gyroscope output data rate selection. Default value: 000 (Refer to *Table 46* and *Table 47*)
FS_G [1:0]	Gyroscope full-scale selection. Default value: 00 (00: 245 dps; 01: 500 dps; 10: Not Available; 11: 2000 dps)
BW_G [1:0]	Gyroscope bandwidth selection. Default value: 00

ODR_G [2:0] are used to set ODR selection when both the accelerometer and gyroscope are activated. BW_G [1:0] are used to set gyroscope bandwidth selection.

The following table summarizes all frequencies available for each combination of the ODR_G / BW_G bits after LPF1 (see *Table 46*) and LPF2 (see *Table 47*) when both the accelerometer and gyroscope are activated. For more details regarding signal processing please refer to *Figure 28*.

Table 46. ODR and BW configuration setting (after LPF1)

ODR_G2	ODR_G1	ODR_G0	ODR [Hz]	Cutoff [Hz](1)
0	0	0	Power-down	n.a.
0	0	1	14.9	5
0	1	0	59.5	19
0	1	1	119	38
1	0	0	238	76
1	0	1	476	100
1	1	0	952	100
1	1	1	n.a.	n.a.

1. Values in the table are indicative and can vary proportionally with the specific ODR value.

Table 47. ODR and BW configuration setting (after LPF2)

ODR_G [2:0]	BW_G [1:0]	ODR [Hz]	Cutoff [Hz](1)
000	00	Power-down	n.a.
000	01	Power-down	n.a.
000	10	Power-down	n.a.
000	11	Power-down	n.a.
001	00	14.9	n.a.
001	01	14.9	n.a.
001	10	14.9	n.a.
001	11	14.9	n.a.
010	00	59.5	16
010	01	59.5	16
010	10	59.5	16
010	11	59.5	16
011	00	119	14
011	01	119	31
011	10	119	31
011	11	119	31
100	00	238	14
100	01	238	29
100	10	238	63
100	11	238	78
101	00	476	21
101	01	476	28
101	10	476	57
101	11	476	100
110	00	952	33
110	01	952	40
110	10	952	58
110	11	952	100
111	00	n.a.	n.a.
111	01	n.a.	n.a.
111	10	n.a.	n.a.
111	11	n.a.	n.a.

1. Values in the table are indicative and can vary proportionally with the specific ODR value.

7.13 CTRL_REG2_G (11h)

Angular rate sensor Control Register 2.

Table 48. CTRL_REG2_G register

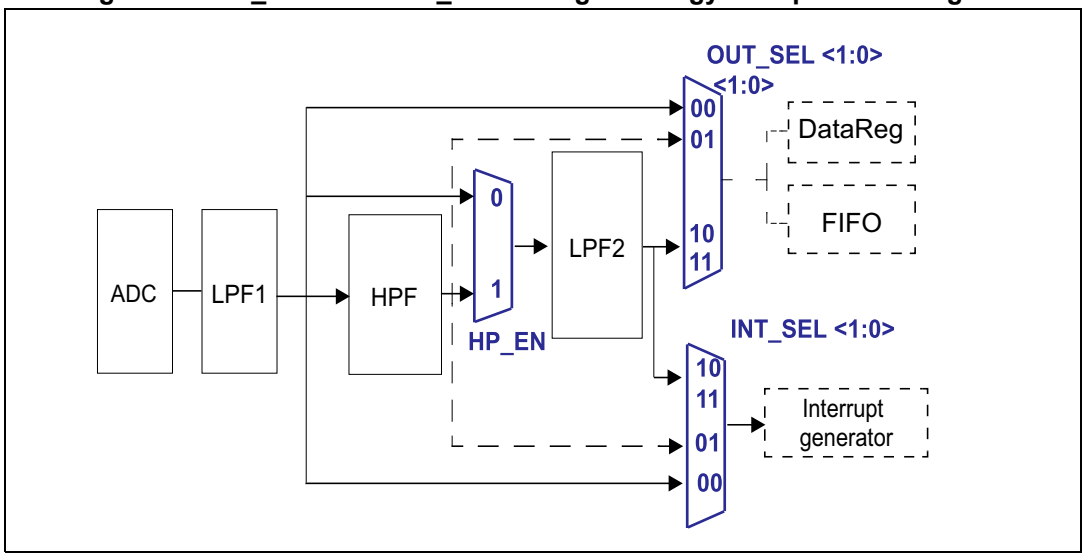
0(1)	0(1)	0(1)	0(1)	INT_SEL1	INT_SEL0	OUT_SEL1	OUT_SEL0

1. These bits must be set to '0' for the correct operation of the device

Table 49. CTRL_REG2_G register description

INT_SEL [1:0]	INT selection configuration. Default value: 00 (Refer to *Figure 28*)
OUT_SEL [1:0]	Out selection configuration. Default value: 00 (Refer to *Figure 28*)

Figure 28. INT_SEL and OUT_SEL configuration gyroscope block diagram



7.14 CTRL_REG3_G (12h)

Angular rate sensor Control Register 3.

Table 50. CTRL_REG3_G register

LP_mode	HP_EN	0(1)	0(1)	HPCF3_G	HPCF2_G	HPCF1_G	HPCF0_G

1. These bits must be set to '0' for the correct operation of the device

Table 51. CTRL_REG3_G register description

LP_mode	Low-power mode enable. Default value: 0 (0: Low-power disabled; 1: Low-power enabled)
HP_EN	High-pass filter enable. Default value: 0 (0: HPF disabled; 1: HPF enabled, refer to *Figure 28*)
HPCF_G [3:0]	Gyroscope high-pass filter cutoff frequency selection. Default value: 0000 Refer to *Table 52*.

Table 52. Gyroscope high-pass filter cutoff frequency configuration [Hz](1)

HPCF_G [3:0]	ODR= 14.9 Hz	ODR= 59.5 Hz	ODR= 119 Hz	ODR= 238 Hz	ODR= 476 Hz	ODR= 952 Hz
0000	1	4	8	15	30	57
0001	0.5	2	4	8	15	30
0010	0.2	1	2	4	8	15
0011	0.1	0.5	1	2	4	8
0100	0.05	0.2	0.5	1	2	4
0101	0.02	0.1	0.2	0.5	1	2
0110	0.01	0.05	0.1	0.2	0.5	1
0111	0.005	0.02	0.05	0.1	0.2	0.5
1000	0.002	0.01	0.02	0.05	0.1	0.2
1001	0.001	0.005	0.01	0.02	0.05	0.1

1. Values in the table are indicative and can vary proportionally with the specific ODR value.

7.15 ORIENT_CFG_G (13h)

Angular rate sensor sign and orientation register.

Table 53. ORIENT_CFG_G register

0(1)	0(1)	SignX_G	SignY_G	SignZ_G	Orient_2	Orient_1	Orient_0

1. These bits must be set to ‘0’ for the correct operation of the device.

Table 54. ORIENT_CFG_G register description

SignX_G	Pitch axis (X) angular rate sign. Default value: 0 (0: positive sign; 1: negative sign)
SignY_G	Roll axis (Y) angular rate sign. Default value: 0 (0: positive sign; 1: negative sign)
SignZ_G	Yaw axis (Z) angular rate sign. Default value: 0 (0: positive sign; 1: negative sign)
Orient [2:0]	Directional user orientation selection. Default value: 000

7.16 INT_GEN_SRC_G (14h)

Angular rate sensor interrupt source register.

Table 55. INT_GEN_SRC_G register

0	IA_G	ZH_G	ZL_G	YH_G	YL_G	XH_G	XL_G

Table 56. INT_GEN_SRC_G register description

IA_G	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH_G	Yaw (Z) high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL_G	Yaw (Z) low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH_G	Roll (Y) high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL_G	Roll (Y) low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH_G	Pitch (X) high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL_G	Pitch (X) low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

7.17 OUT_TEMP_L (15h), OUT_TEMP_H (16h)

Temperature data output register. L and H registers together express a 16-bit word in two's complement right-justified.

Table 57. OUT_TEMP_L register

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

Table 58. OUT_TEMP_H register

Temp11	Temp11	Temp11	Temp11	Temp11	Temp10	Temp9	Temp8

Table 59. OUT_TEMP register description

Temp [11:0]	Temperature sensor output data. The value is expressed as two's complement sign extended on the MSB.

7.18 STATUS_REG (17h)

Status register.

Table 60. STATUS_REG register

0	IG_XL	IG_G	INACT	BOOT_ STATUS	TDA	GDA	XLDA

Table 61. STATUS_REG register description

IG_XL	Accelerometer interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
IG_G	Gyroscope interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
INACT	Inactivity interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
BOOT_ STATUS	Boot running flag signal. Default value: 0 (0: no boot running; 1: boot running)
TDA	Temperature sensor new data available. Default value: 0 (0: new data is not yet available; 1: new data is available)
GDA	Gyroscope new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
XLDA	Accelerometer new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)

7.19 OUT_X_G (18h - 19h)

Angular rate sensor pitch axis (X) angular rate output register. The value is expressed as a 16-bit word in two's complement.

7.20 OUT_Y_G (1Ah - 1Bh)

Angular rate sensor roll axis (Y) angular rate output register. The value is expressed as a 16-bit word in two's complement.

7.21 OUT_Z_G (1Ch - 1Dh)

Angular rate sensor Yaw axis (Z) angular rate output register. The value is expressed as a 16-bit word in two's complement.

7.22 CTRL_REG4 (1Eh)

Control register 4.

Table 62. CTRL_REG4 register

0(1)	0(1)	Zen_G	Yen_G	Xen_G	0(1)	LIR_XL1	4D_XL1

1. These bits must be set to '0' for the correct operation of the device.

Table 63. CTRL_REG4 register description

Zen_G	Gyroscope's Yaw axis (Z) output enable. Default value: 1 (0: Z-axis output disabled; 1: Z-axis output enabled)
Yen_G	Gyroscope's roll axis (Y) output enable. Default value: 1 (0: Y-axis output disabled; 1: Y-axis output enabled)
Xen_G	Gyroscope's pitch axis (X) output enable. Default value: 1 (0: X -xis output disabled; 1: X-axis output enabled)
LIR_XL1	Latched Interrupt. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)
4D_XL1	4D option enabled on Interrupt. Default value: 0 (0: interrupt generator uses 6D for position recognition; 1: interrupt generator uses 4D for position recognition)

7.23 CTRL_REG5_XL (1Fh)

Linear acceleration sensor Control Register 5.

Table 64. CTRL_REG5_XL register

DEC_1	DEC_0	Zen_XL	Yen_XL	Xen_XL	0(1)	0(1)	0(1)

1. These bits must be set to '0' for the correct operation of the device.

Table 65. CTRL_REG5_XL register description

DEC_ [0:1]	Decimation of acceleration data on OUT REG and FIFO. Default value: 00 (00: no decimation; 01: update every 2 samples; 10: update every 4 samples; 11: update every 8 samples)
Zen_XL	Accelerometer's Z-axis output enable. Default value: 1 (0: Z-axis output disabled; 1: Z-axis output enabled)
Yen_XL	Accelerometer's Y-axis output enable. Default value: 1 (0: Y-axis output disabled; 1: Y-axis output enabled)
Xen_XL	Accelerometer's X-axis output enable. Default value: 1 (0: X-axis output disabled; 1: X-axis output enabled)

7.24 CTRL_REG6_XL (20h)

Linear acceleration sensor Control Register 6.

Table 66. CTRL_REG6_XL register

ODR_XL2	ODR_XL1	ODR_XL0	FS1_XL	FS0_XL	BW_SCAL_ODR	BW_XL1	BW_XL0

Table 67. CTRL_REG6_XL register description

ODR_XL [2:0]	Output data rate and power mode selection. default value: 000 (see *Table 68*)
FS_XL [1:0]	Accelerometer full-scale selection. Default value: 00 (00: ±2*g*; 01: ±16 *g;* 10: ±4 *g*; 11: ±8 *g*)
BW_SCAL_ ODR	Bandwidth selection. Default value: 0 (0: bandwidth determined by ODR selection: - BW = 408 Hz when ODR = 952 Hz, 50 Hz, 10 Hz; - BW = 211 Hz when ODR = 476 Hz; - BW = 105 Hz when ODR = 238 Hz; - BW = 50 Hz when ODR = 119 Hz; 1: bandwidth selected according to BW_XL [2:1] selection)
BW_XL [1:0]	Anti-aliasing filter bandwidth selection. Default value: 00 (00: 408 Hz; 01: 211 Hz; 10: 105 Hz; 11: 50 Hz)

ODR_XL [2:0] is used to set power mode and ODR selection. *Table 68* indicates all the frequencies available when only the accelerometer is activated.

Table 68. ODR register setting (accelerometer only mode)

ODR_XL2	ODR_XL1	ODR_XL0	ODR selection [Hz]
0	0	0	Power-down
0	0	1	10 Hz
0	1	0	50 Hz
0	1	1	119 Hz
1	0	0	238 Hz
1	0	1	476 Hz
1	1	0	952 Hz
1	1	1	n.a.

7.25 CTRL_REG7_XL (21h)

Linear acceleration sensor Control Register 7.

Table 69. CTRL_REG7_XL register

HR	DCF1	DCF0	0(1)	0(1)	FDS	0(1)	HPIS1

1. These bits must be set to ‘0’ for the correct operation of the device

Table 70. CTRL_REG7_XL register description

HR	High resolution mode for accelerometer enable. Default value: 0 (0: disabled; 1: enabled). Refer to *Table 71*
DCF[1:0]	Accelerometer digital filter (high pass and low pass) cutoff frequency selection: the band-width of the high-pass filter depends on the selected ODR. Refer to *Table 71*
FDS	Filtered data selection. Default value: 0 (0: internal filter bypassed; 1: data from internal filter sent to output register and FIFO)
HPIS1	High-pass filter enabled for acceleration sensor interrupt function on Interrupt. Default value: 0 (0: filter bypassed; 1: filter enabled)

Table 71. Low pass cutoff frequency in high resolution mode (HR = 1)

HR	CTRL_REG7 (DCF [1:0])	LP cutoff freq. [Hz]
1	00	ODR/50
1	01	ODR/100
1	10	ODR/9
1	11	ODR/400

7.26 CTRL_REG8 (22h)

Control register 8.

Table 72. CTRL_REG8 register

BOOT	BDU	H_LACTIVE	PP_OD	SIM	IF_ADD_INC	BLE	SW_RESET

Table 73. CTRL_REG8 register description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content(1))
BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB read)
H_LACTIVE	Interrupt activation level. Default value: 0 (0: interrupt output pins active high; 1: interrupt output pins active low)
PP_OD	Push-pull/open-drain selection on the INT1_A/G pin and INT2_A/G pin. Default value: 0 (0: push-pull mode; 1: open-drain mode)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface).
IF_ADD_INC	Register address automatically incremented during a multiple byte access with a serial interface (I^2C or SPI). Default value: 1 (0: disabled; 1: enabled)
BLE	Big/Little Endian data selection. Default value 0 (0: data LSB @ lower address; 1: data MSB @ lower address)
SW_RESET	Software reset. Default value: 0 (0: normal mode; 1: reset device) This bit is cleared by hardware after next flash boot.

1. Boot request is executed as soon as internal oscillator is turned-on. It is possible to set bit while in power-down mode, in this case it will be served at the next normal mode or sleep mode.

7.27 CTRL_REG9 (23h)

Control register 9.

Table 74. CTRL_REG9 register

0(1)	SLEEP_G	0(1)	FIFO_ TEMP_EN	DRDY_ mask_bit	I2C_DISAB LE	FIFO_EN	STOP_ON _FTH

1. These bits must be set to '0' for the correct operation of the device

Table 75. CTRL_REG9 register description

SLEEP_G	Gyroscope sleep mode enable. Default value: 0 (0: disabled; 1: enabled)
FIFO_TEMP_EN	Temperature data storage in FIFO enable. Default value: 0 (0: temperature data not stored in FIFO; 1: temperature data stored in FIFO)
DRDY_mask_bit	Data available enable bit. Default value: 0 (0: DA timer disabled; 1: DA timer enabled)
I2C_DISABLE	Disable I^2C interface. Default value: 0 (0: both I^2C and SPI enabled; 1: I^2C disabled, SPI only)
FIFO_EN	FIFO memory enable. Default value: 0 (0: disabled; 1: enabled)
STOP_ON_FTH	Enable FIFO threshold level use. Default value: 0 (0: FIFO depth is not limited; 1: FIFO depth is limited to threshold level)

7.28 CTRL_REG10 (24h)

Control register 10.

Table 76. CTRL_REG10 register

0(1)	0(1)	0(1)	0(1)	0(1)	ST_G	0(1)	ST_XL

1. These bits must be set to '0' for the correct operation of the device

Table 77. CTRL_REG10 register description

ST_G	Angular rate sensor self-test enable. Default value: 0 (0: Self-test disabled; 1: Self-test enabled)
ST_XL	Linear acceleration sensor self-test enable. Default value: 0 (0: Self-test disabled; 1: Self-test enabled)

7.29 INT_GEN_SRC_XL (26h)

Linear acceleration sensor interrupt source register.

Table 78. INT_GEN_SRC_XL register

0	IA_XL	ZH_XL	ZL_XL	YH_XL	YL_XL	XH_XL	XL_XL

Table 79. INT_GEN_SRC_XL register description

IA_XL	Interrupt active. Default value: 0. (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH_XL	Accelerometer's Z high event. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL_XL	Accelerometer's Z low event. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH_XL	Accelerometer's Y high event. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL_XL	Accelerometer's Y low event. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH_XL	Accelerometer's X high event. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL_XL	Accelerometer's X low. event. Default value: 0 (0: no interrupt, 1: X low event has occurred)

7.30 STATUS_REG (27h)

Status register.

Table 80. STATUS_REG register

0	IG_XL	IG_G	INACT	BOOT_ STATUS	TDA	GDA	XLDA

Table 81. STATUS_REG register description

IG_XL	Accelerometer interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
IG_G	Gyroscope interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
INACT	Inactivity interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
BOOT_ STATUS	Boot running flag signal. Default value: 0 (0: no boot running; 1: boot running)
TDA	Temperature sensor new data available. Default value: 0 (0: a new data is not yet available; 1: a new data is available)
GDA	Gyroscope new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
XLDA	Accelerometer new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)

7.31 OUT_X_XL (28h - 29h)

Linear acceleration sensor X-axis output register. The value is expressed as a 16-bit word in two's complement.

7.32 OUT_Y_XL (2Ah - 2Bh)

Linear acceleration sensor Y-axis output register. The value is expressed as a 16-bit word in two's complement.

7.33 OUT_Z_XL (2Ch - 2Dh)

Linear acceleration sensor Z-axis output register. The value is expressed as a 16-bit word in two's complement.

7.34 FIFO_CTRL (2Eh)

FIFO control register.

Table 82. FIFO_CTRL register

FMODE2	FMODE1	FMODE0	FTH4	FTH3	FTH2	FTH1	FTH0

Table 83. FIFO_CTRL register description

FMODE [2:0]	FIFO mode selection bits. Default value: 000 For further details refer to *Table 84*.
FTH [4:0]	FIFO threshold level setting. Default value: 0 0000

Table 84. FIFO mode selection

FMODE2	FMODE1	FMODE0	Mode
0	0	0	Bypass mode. FIFO turned off
0	0	1	FIFO mode. Stops collecting data when FIFO is full.
0	1	0	Reserved
0	1	1	Continuous mode until trigger is deasserted, then FIFO mode.
1	0	0	Bypass mode until trigger is deasserted, then Continuous mode.
1	1	0	Continuous mode. If the FIFO is full, the new sample over-writes the older sample.

7.35 FIFO_SRC (2Fh)

FIFO status control register.

Table 85. FIFO_SRC register

FTH	OVRN	FSS5	FSS4	FSS3	FSS2	FSS1	FSS0

Table 86. FIFO_SRC register description

FTH	FIFO threshold status. (0: FIFO filling is lower than threshold level; 1: FIFO filling is equal or higher than threshold level
OVRN	FIFO overrun status. (0: FIFO is not completely filled; 1: FIFO is completely filled and at least one samples has been overwritten) For further details refer to *Table 87*.
FSS [5:0]	Number of unread samples stored into FIFO. (000000: FIFO empty; 100000: FIFO full, 32 unread samples) For further details refer to *Table 87*.

Table 87. FIFO_SRC example: OVR/FSS details

FTH	OVRN	FSS5	FSS4	FSS3	FSS2	FSS1	FSS0	Description
0	0	0	0	0	0	0	0	FIFO empty
--(1)	0	0	0	0	0	0	1	1 unread sample
...								
--(1)	0	1	0	0	0	0	0	32 unread samples
1	1	1	0	0	0	0	0	At least one sample has been overwritten

1. When the number of unread samples in FIFO is greater than the threshold level set in register *FIFO_CTRL (2Eh)*, FTH value is '1'.

7.36 INT_GEN_CFG_G (30h)

Angular rate sensor interrupt generator configuration register.

Table 88. INT_GEN_CFG_G register

AOI_G	LIR_G	ZHIE_G	ZLIE_G	YHIE_G	YLIE_G	XHIE_G	XLIE_G

Table 89. INT_GEN_CFG_G register description

AOI_G	AND/OR combination of gyroscope's interrupt events. Default value: 0 (0: OR combination; 1: AND combination)
LIR_G	Latch Gyroscope interrupt request. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)
ZHIE_G	Enable interrupt generation on gyroscope's yaw (Z) axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value higher than preset threshold)
ZLIE_G	Enable interrupt generation on gyroscope's yaw (Z) axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value lowerthan preset threshold)
YHIE_G	Enable interrupt generation on gyroscope's roll (Y) axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value higher than preset threshold)
YLIE_G	Enable interrupt generation on gyroscope's roll (Y) axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value lower than preset threshold)
XHIE_G	Enable interrupt generation on gyroscope's pitch (X) axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value higher than preset threshold)
XLIE_G	Enable interrupt generation on gyroscope's pitch (X) axis low event. Default value: 0. (0: disable interrupt request; 1: interrupt request on measured angular rate value lower than preset threshold)

7.37 INT_GEN_THS_X_G (31h - 32h)

Angular rate sensor interrupt generator threshold registers. The value is expressed as a 15-bit word in two's complement.

Table 90. INT_GEN_THS_XH_G register

DCRM_G	THS_G_X14	THS_G_X13	THS_G_X12	THS_G_X11	THS_G_X10	THS_G_X9	THS_G_X8

Table 91. INT_GEN_THS_XL_G register

THS_G_X7	THS_G_X6	THS_G_X5	THS_G_X4	THS_G_X3	THS_G_X2	THS_G_X1	THS_G_X0

Table 92. INT_GEN_THS_X_G register description

DCRM_G	Decrement or reset counter mode selection. Default value: 0 (0: Reset; 1: Decrement, as per counter behavior in *Figure 29* and *Figure 30*)
THS_G_X [14:0]	Angular rate sensor interrupt threshold on pitch (X) axis. Default value: 0000000 00000000

7.38 INT_GEN_THS_Y_G (33h - 34h)

Angular rate sensor interrupt generator threshold registers. The value is expressed as a 15-bit word in two's complement.

Table 93. INT_GEN_THS_YH_G register

0(1)	THS_G_Y14	THS_G_Y13	THS_G_Y12	THS_G_Y11	THS_G_Y10	THS_G_Y9	THS_G_Y8

1. This bit must be set to '0' for the correct operation of the device.

Table 94. INT_GEN_THS_YL_G register

THS_G_Y7	THS_G_Y6	THS_G_Y5	THS_G_Y4	THS_G_Y3	THS_G_Y2	THS_G_Y1	THS_G_Y0

Table 95. INT_GEN_THS_Y_G register description

THS_G_Y [14:0]	Angular rate sensor interrupt threshold on roll (Y) axis. Default value: 0000000 00000000.

7.39 INT_GEN_THS_Z_G (35h - 36h)

Angular rate sensor interrupt generator threshold registers. The value is expressed as a 15-bit word in two's complement.

Table 96. INT_GEN_THS_ZH_G register

0(1)	THS_G_Z14	THS_G_Z13	THS_G_Z12	THS_G_Z11	THS_G_Z10	THS_G_Z9	THS_G_Z8

1. This bit must be set to '0' for the correct operation of the device.

Table 97. INT_GEN_THS_ZL_G register

THS_G_Z7	THS_G_Z6	THS_G_Z5	THS_G_Z4	THS_G_Z3	THS_G_Z2	THS_G_Z1	THS_G_Z0

Table 98. INT_GEN_THS_Z_G register description

THS_G_Z [14:0]	Angular rate sensor interrupt thresholds on yaw (Z) axis. Default value: 0000000 00000000.

7.40 INT_GEN_DUR_G (37h)

Angular rate sensor interrupt generator duration register.

Table 99. INT_GEN_DUR_G register

WAIT_G	DUR_G6	DUR_G5	DUR_G4	DUR_G3	DUR_G2	DUR_G1	DUR_G0

Table 100. INT_GEN_DUR_G register description

WAIT_G	Exit from interrupt wait function enable. Default value: 0 (0: wait function off; 1: wait for DUR_G [6:0] samples before exiting interrupt)
DUR_G [6:0]	Enter/exit interrupt duration value. Default Value: 000 0000

The **DUR_G [6:0]** bits set the minimum duration of the interrupt event to be recognized. Duration steps and maximum values depend on the ODR chosen.

The **WAIT_G** bit has the following meaning:

'0': the interrupt falls immediately if the signal crosses the selected threshold

'1': if the signal crosses the selected threshold, the interrupt falls after a number of samples equal to the value of the duration counter register.

For further details refer to *Figure 29* and *Figure 30*.

Figure 29. Wait bit disabled

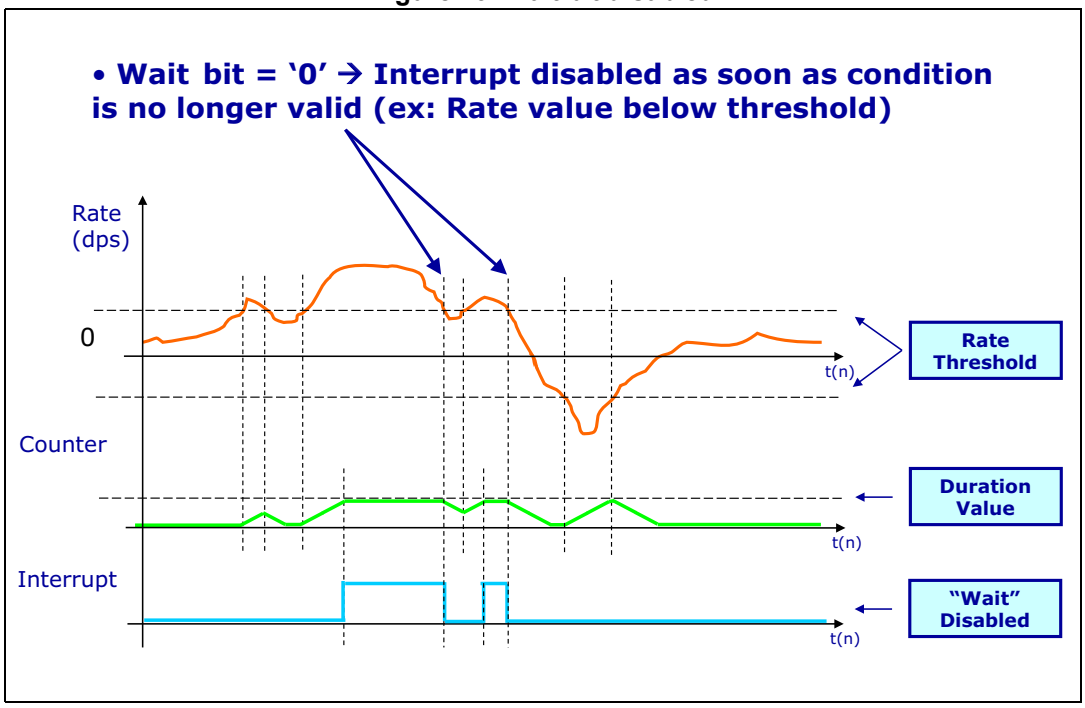
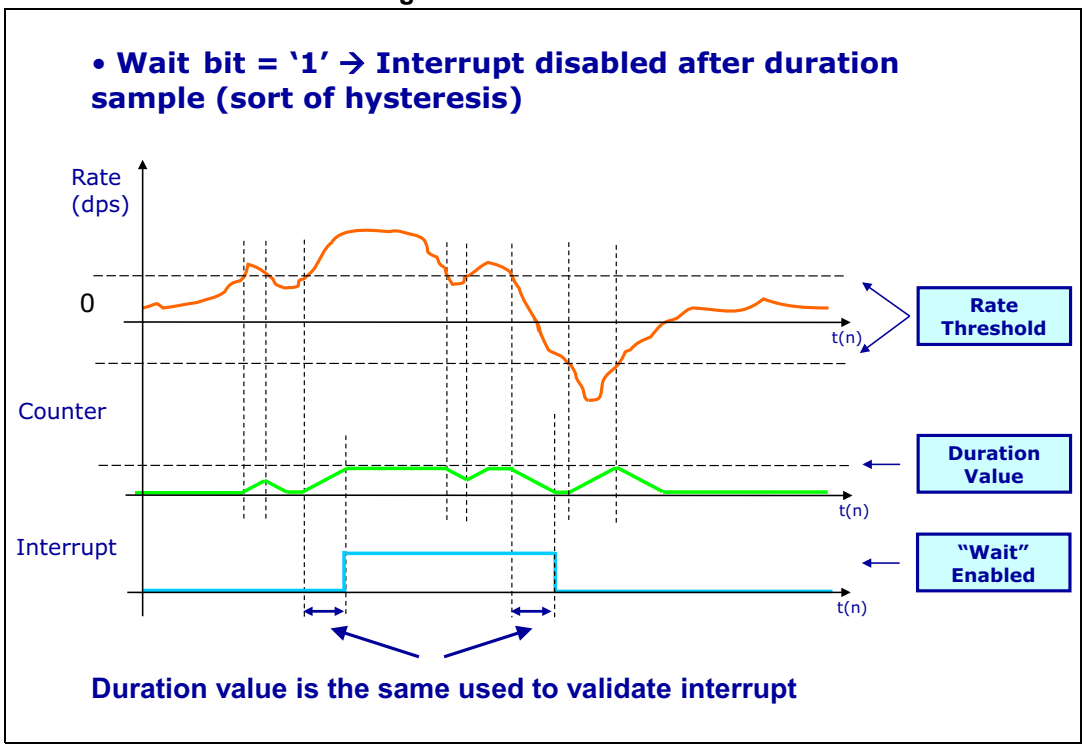


Figure 30. Wait bit enabled



8 Magnetometer register description

8.1 OFFSET_X_REG_L_M (05h), OFFSET_X_REG_H_M (06h)

This register is a 16-bit register and represents the X offset used to compensate environmental effects (data is expressed as two's complement). This value acts on the magnetic output data value in order to subtract the environmental offset.

Default value: 0

Table 101. OFFSET_X_REG_L_M register

OFXM7	OFXM6	OFXM5	OFXM4	OFXM3	OFXM2	OFXM1	OFXM0

Table 102. OFFSET_X_REG_H_M register

OFXM15	OFXM14	OFXM13	OFXM12	OFXM11	OFXM10	OFXM9	OFXM8

8.2 OFFSET_Y_REG_L_M (07h), OFFSET_Y_REG_H_M (08h)

This register is a 16-bit register and represents the Y offset used to compensate environmental effects (data is expressed as two's complement). This value acts on the magnetic output data value in order to subtract the environmental offset.

Default value: 0

Table 103. OFFSET_Y_REG_L_M register

OFYM7	OFYM6	OFYM5	OFYM4	OFYM3	OFYM2	OFYM1	OFYM0

Table 104. OFFSET_Y_REG_H_M register

OFYM15	OFYM14	OFYM13	OFYM12	OFYM11	OFYM10	OFYM9	OFYM8

8.3 OFFSET_Z_REG_L_M (09h), OFFSET_Z_REG_H_M (0Ah)

This register is a 16-bit register and represents the Z offset used to compensate environmental effects (data is expressed as two's complement). This value acts on the magnetic output data value in order to subtract the environmental offset.

Default value: 0.

Table 105. OFFSET_Z_REG_L_M register

OFZM7	OFZM6	OFZM5	OFZM4	OFZM3	OFZM2	OFZM1	OFZM0

Table 106. OFFSET_Z_REG_H_M register

OFZM15	OFZM14	OFZM13	OFZM12	OFZM11	OFZM10	OFZM9	OFZM8

8.4 WHO_AM_I_M (0Fh)

Device identification register.

Table 107. WHO_AM_I_M register

0	0	1	1	1	1	0	1

8.5 CTRL_REG1_M (20h)

Table 108. CTRL_REG1_M register

TEMP_ COMP	OM1	OM0	DO2	DO1	DO0	FAST_ODR	ST

Table 109. CTRL_REG1_M register description

TEMP_COMP	Temperature compensation enable. Default value: 0 (0: temperature compensation disabled; 1: temperature compensation enabled)
OM[1:0]	X and Y axes operative mode selection. Default value: 00 (Refer to *Table 110*)
DO[2:0]	Output data rate selection. Default value: 100 (Refer to *Table 111*)
FAST_ODR	FAST_ODR enables data rates higher than 80 Hz. Default value: 0 (0: Fast_ODR disabled; 1: FAST_ODR enabled)
ST	Self-test enable. Default value: 0 (0: self-test disabled; 1: self-test enabled)

Table 110. X and Y axes operative mode selection

OM1	OM0	Operative mode for X and Y axes
0	0	Low-power mode
0	1	Medium-performance mode
1	0	High-performance mode
1	1	Ultra-high performance mode

Table 111. Output data rate configuration

DO2	DO1	DO0	ODR [Hz]
0	0	0	0.625
0	0	1	1.25
0	1	0	2.5
0	1	1	5
1	0	0	10
1	0	1	20
1	1	0	40
1	1	1	80

8.6 CTRL_REG2_M (21h)

Table 112. CTRL_REG2_M register

0(1)	FS1	FS0	0(1)	REBOOT	SOFT_RST	0(1)	0(1)

1. These bits must be set to '0' for the correct operation of the device.

Table 113. CTRL_REG2_M register description

FS[1:0]	Full-scale configuration. Default value: 00 Refer to *Table 114*
REBOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
SOFT_RST	Configuration registers and user register reset function. (0: default value; 1: reset operation)

Table 114. Full-scale selection

FS1	FS0	Full scale
0	0	± 4 gauss
0	1	± 8 gauss
1	0	± 12 gauss
1	1	± 16 gauss

8.7 CTRL_REG3_M (22h)

Table 115. CTRL_REG3_M register

I2C_ DISABLE	0(1)	LP	0(1)	0(1)	SIM	MD1	MD0

1. These bits must be set to '0' for the correct operation of the device.

Table 116. CTRL_REG3_M register description

I2C_DISABLE	Disable I^2C interface. Default value 0. (0: I^2C enable; 1: I^2C disable)
LP	Low-power mode configuration. Default value: 0 If this bit is '1', the DO[2:0] is set to 0.625 Hz and the system performs, for each channel, the minimum number of averages. Once the bit is set to '0', the magnetic data rate is configured by the DO bits in the *CTRL_REG1_M (20h)* register.
SIM	SPI Serial Interface mode selection. Default value: 0 (0: SPI only write operations enabled; 1: SPI read and write operations enable).
MD[1:0]	Operating mode selection. Default value: 11 Refer to *Table 117.*

Table 117. System operating mode selection

MD1	MD0	Mode
0	0	Continuous-conversion mode
0	1	Single-conversion mode
1	0	Power-down mode
1	1	Power-down mode

8.8 CTRL_REG4_M (23h)

Table 118. CTRL_REG4_M register

0(1)	0(1)	0(1)	0(1)	OMZ1	OMZ0	BLE	0(1)

1. These bits must be set to '0' for the correct operation of the device

Table 119. CTRL_REG4_M register description

OMZ[1:0]	Z-axis operative mode selection. Default value: 00. Refer to *Table 120.*
BLE	Big/Little Endian data selection. Default value: 0 (0: data LSb at lower address; 1: data MSb at lower address)

Table 120. Z-axis operative mode selection

OMZ1	OMZ0	Operative mode for Z-axis
0	0	Low-power mode
0	1	Medium-performance mode
1	0	High-performance mode
1	1	Ultra-high performance mode

8.9 CTRL_REG5_M (24h)

Table 121. CTRL_REG5_M register

FAST_READ	BDU	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)

1. These bits must be set to '0' for the correct operation of the device.

Table 122. CTRL_REG5_M register description

FAST_READ	FAST_READ allows reading the high part of DATA OUT only in order to increase reading efficiency. Default value: 0 (0: FAST_READ disabled; 1: FAST_READ enabled)
BDU	Block data update for magnetic data. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB have been read)

8.10 STATUS_REG_M (27h)

Table 123. STATUS_REG_M register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 124. STATUS_REG_M register description

ZYXOR	X, Y and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous set)
ZOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YOR	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXDA	X, Y and Z-axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z-axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y-axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)
XDA	X-axis new data available. Default value: 0 (0: a new data for the X-axis is not yet available; 1: a new data for the X-axis is available)

8.11 OUT_X_L_M (28h), OUT_X_H_M(29h)

Magnetometer X-axis data output. The value of the magnetic field is expressed as two’s complement.

8.12 OUT_Y_L_M (2Ah), OUT_Y_H_M (2Bh)

Magnetometer Y-axis data output. The value of the magnetic field is expressed as two’s complement.

8.13 OUT_Z_L_M (2Ch), OUT_Z_H_M (2Dh)

Magnetometer Z-axis data output. The value of the magnetic field is expressed as two’s complement.

8.14 INT_CFG_M (30h)

Table 125. INT_CFG_M register

XIEN	YIEN	ZIEN	0(1)	0(1)	IEA	IEL	IEN

1. This bit must be set to '0' for the correct operation of the device.

Table 126. INT_CFG_M register description

XIEN	Enable interrupt generation on X-axis. Default value: 0 0: disable interrupt request; 1: enable interrupt request
YIEN	Enable interrupt generation on Y-axis. Default value: 0 0: disable interrupt request; 1: enable interrupt request
ZIEN	Enable interrupt generation on Z-axis. Default value: 0 0: disable interrupt request; 1: enable interrupt request
IEA	Interrupt active configuration on INT_MAG. Default value: 0 0: low; 1: high
IEL	Latch interrupt request. Default value: 0 0: interrupt request latched; 1: interrupt request not latched) Once latched, the INT_M pin remains in the same state until *INT_SRC_M (31h)*) is read.
IEN	Interrupt enable on the INT_M pin. Default value: 0 0: disable; 1: enable

8.15 INT_SRC_M (31h)

Table 127. INT_SRC_M register

PTH_X	PTH_Y	PTH_Z	NTH_X	NTH_Y	NTH_Z	MROI(1)	INT

1. This functionality can be enabled only if the IEN bit in *INT_CFG_M (30h)* is enabled.

Table 128. INT_SRC_M register description

PTH_X	Value on X-axis exceeds the threshold on the positive side. Default value: 0
PTH_Y	Value on Y-axis exceeds the threshold on the positive side. Default value: 0
PTH_Z	Value on Z-axis exceeds the threshold on the positive side. Default value: 0
NTH_X	Value on X-axis exceeds the threshold on the negative side. Default value: 0
NTH_Y	Value on Y-axis exceeds the threshold on the negative side. Default value: 0
NTH_Z	Value on Z-axis exceeds the threshold on the negative side. Default value: 0
MROI	Internal measurement range overflow on magnetic value. Default value: 0
INT	This bit signals when the interrupt event occurs.

8.16 INT_THS_L(32h), INT_THS_H(33h)

Interrupt threshold. Default value: 0.

The value is expressed in 15-bit unsigned.

Even if the threshold is expressed in absolute value, the device detects both positive and negative thresholds.

Table 129. INT_THS_L_M register

THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 130. INT_THS_H_M register

0(1)	THS14	THS13	THS12	THS11	THS10	THS9	THS8

1. This bit must be set to ‘0’ for the correct operation of the device.

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

9.1 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard. It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

9.2 LGA package information

Figure 31. LGA (3.5x3x1 mm) 24-lead package outline

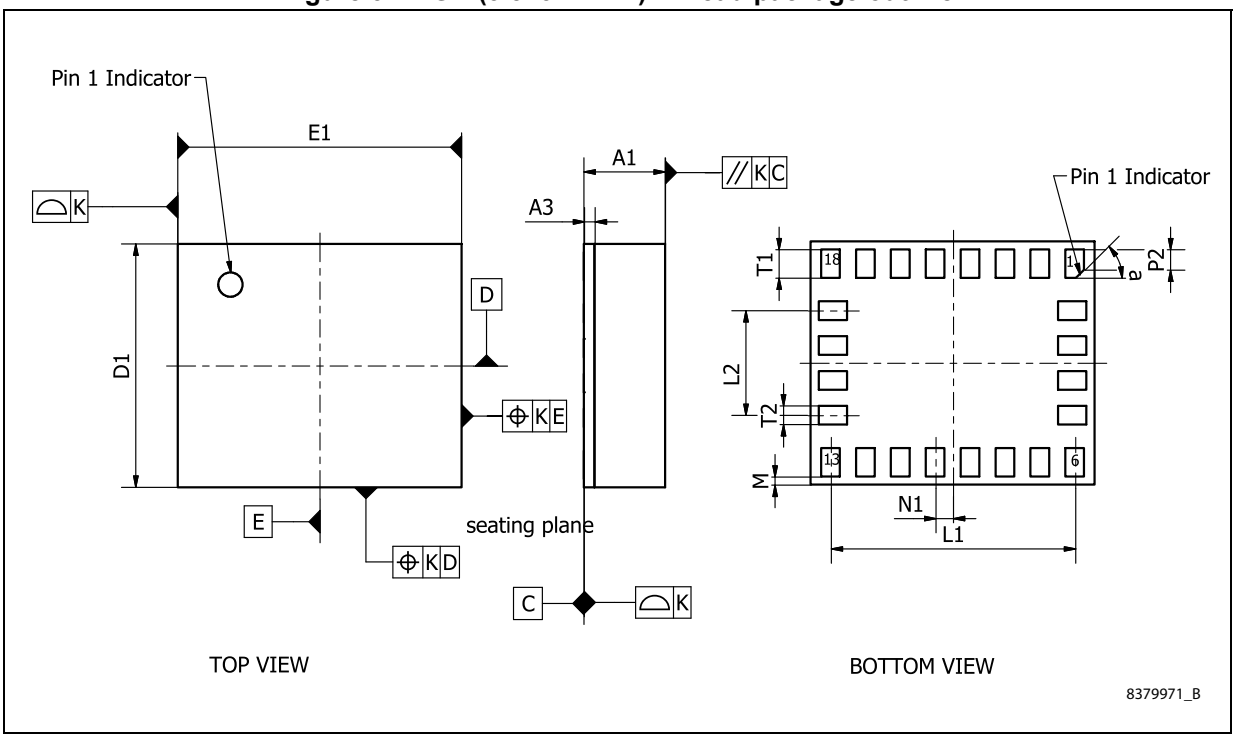


Table 131. LGA (3.5x3x1 mm) 24-lead package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A1		1.000	1.027
A3		0.130	
D1	2.850	3.000	3.150
E1	3.350	3.500	3.650
L1	2.960	3.010	3.060
L2	1.240	1.290	1.340
N1	0.165	0.215	0.265
P2	0.200	0.250	0.300
a		45°	
T1	0.300	0.350	0.400
T2	0.180	0.230	0.280
K		0.050	
M		0.100	

10 Revision history

Table 132. Document revision history

Date	Revision	Changes
18-Dec-2013	1	Initial release
05-Nov-2014	2	Datasheet status promoted from preliminary to production data Added ±16 *g* linear acceleration full scale throughout datasheet Corrected typo in footnote *3*, *4* and *5* of *Table 2: Pin description* Updated *Figure 15: LSM9DS1 electrical connections* and *Section 4.1: External capacitors* Updated *Table 117: System operating mode selection*
12-Mar-2015	3	Added FAST_ODR bit to *CTRL_REG1_M (20h)* Added FAST_READ bit to *CTRL_REG5_M (24h)*

2.2.13. Diodo Schotky

SS3 Series
Controlled Avalanche Power Diodes

RoHS Compliant

Features:

- For surface mounted application.
- Metal to silicon rectifier, majority carrier conduction.
- Low forward voltage drop.
- Easy pick and place.
- High surge current capability.
- Epitaxial construction
- High temperature soldering : 260°C/10 seconds at terminals.

Mechanical Data:

Case : Moulded plastic.
Terminals : Solder plated.
Polarity : Indicated by cathode band.

Max. Ratings and Electrical Characteristics

Rating at 25°C ambient temperature unless otherwise specified.
Single phase, half wave, 60Hz, resistive or inductive load. For capacitive load, derate current by 20%.

Characteristics	Symbol	SS34	SS36	Unit
Max. Recurrent Peak Reverse Voltage	V_{RRM}	40	60	V
Max. RMS Voltage	V_{RMS}	28	42	
Max. DC Blocking Voltage	V DC	40	60	
Max. Average Forward Rectified Current at T_L	$I_{(AV)}$	3.0		A
Peak forward surge current, 8.3ms single half sine-wave superimposed A on rated load (JEDEC method)	I_{FSM}	100		
Max. Instantaneous Forward Voltage at 3.0A (Note 1)	V_F	0.5	0.75	V
Max. DC Reverse Current at T_A = 25°C at rated DC blocking voltage at T_A = 100°C	I_R	0.5 20	10.0	mA
Typical Thermal Resistance (Note 2)	$R_{\theta JL}$ $R_{\theta JA}$	17 55		°C/W
Operating Temperature Range	T_J	-55 to +125	-55 to +150	°C
Storage Temperature Range	T_{STG}	-55 to +150		

Notes:
1. Pulse test with PW = 300µsec, 1% duty cycle.
2. Measured on PC Board with 0.6 x 0.6” (16mm × 16mm) copper pad areas.

Ratings and Characteristic Curves:

Figure 1 Maximum Forward Current Derating Curve

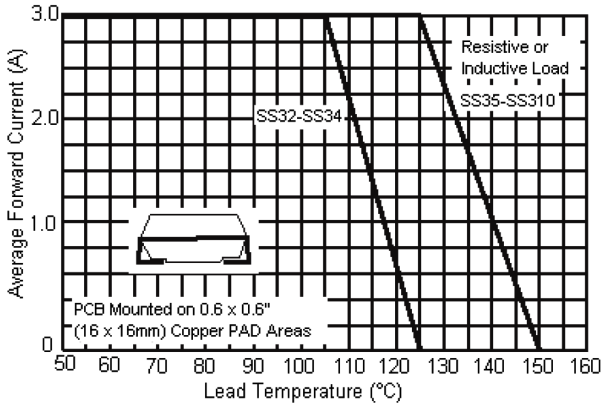


Figure 2 Maximum Non-Repetitive Forward Surge Current

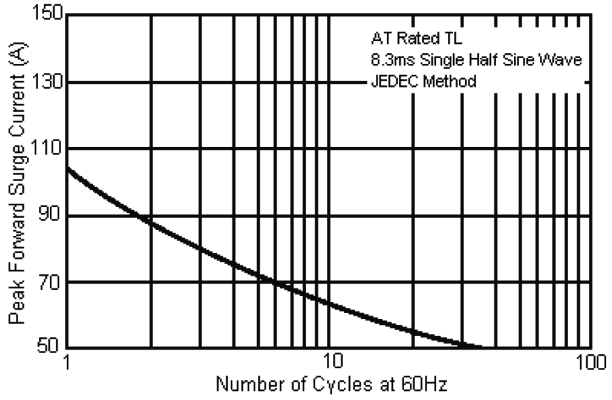


Figure 3 Typical Forward Characteristics

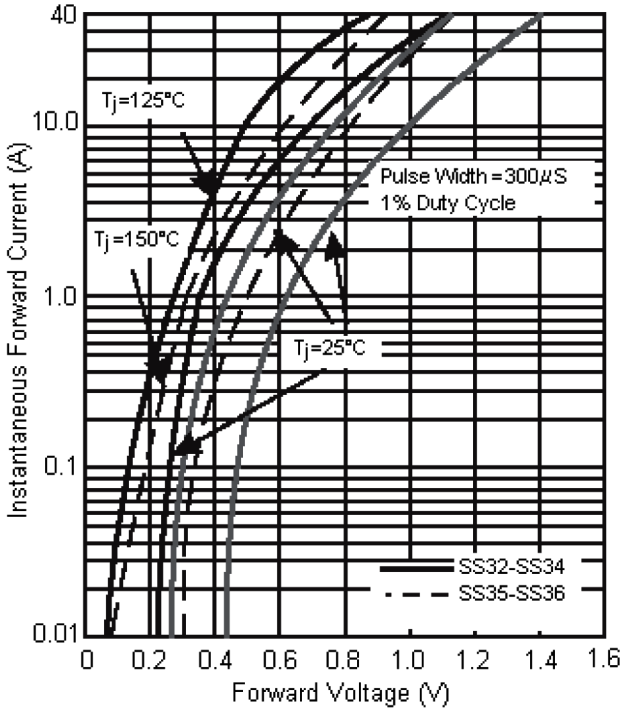


Figure 4 Typical Reverse Characteristics

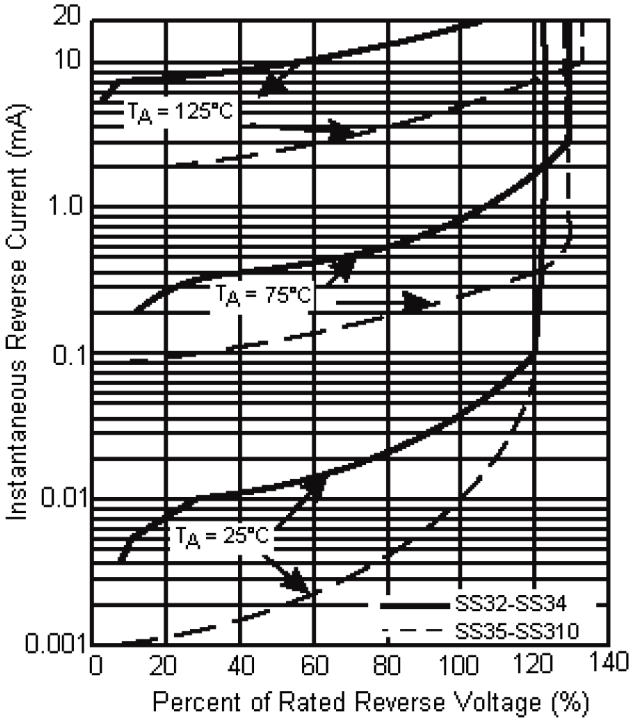


Figure 5 Typical Junction Capacitance

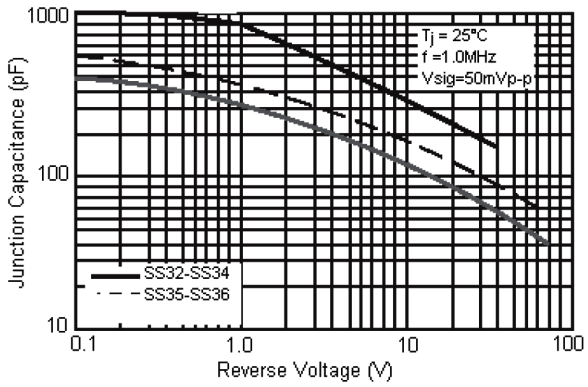
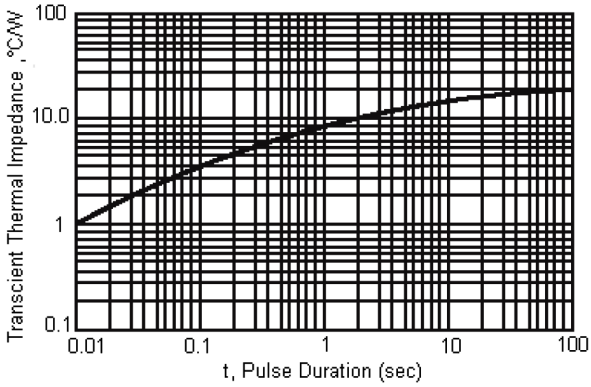
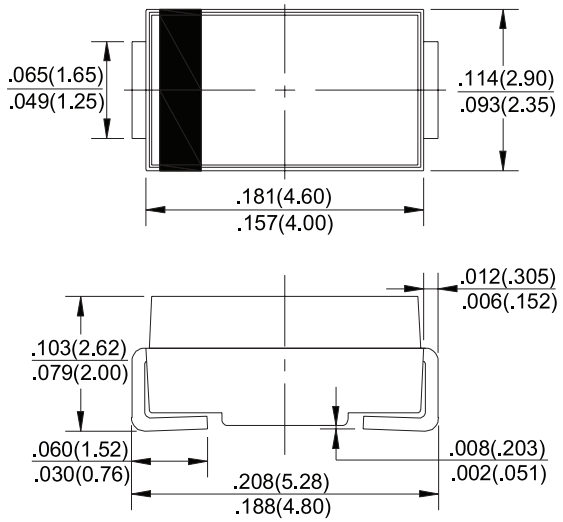


Figure 6 Typical Transient Thermal Impedance



Package Dimensions:

SMA



Dimensions : Inches (Millimetres)

Part Number Table

$I_{F(AV)}$ (A)	T_C (°C)	V_{RRM} (V)	V_{FM} maximum (V)	I_{RM} maximum (mA)	Package	Part Number
3	105	40	0.5	0.5	SMA	SS34
		60	0.75			SS36

2.2.14. Amplificador Lineal

2.2.15. Inductor

TDK

SMD Inductors(Coils)
For Power Line(Wound, Magnetic Shielded)

Conformity to RoHS Directive

GLFR Series GLFR1608

FEATURES

- It delivers low Rdc with high Idc.
- It is lead-free compatible.
  The product contains no lead whatsoever.
  It is able to withstand high temperature reflows (260°C during the peak) used in lead-free soldering.
- It is a product conforming to RoHS directive.
- It's construction supports bulk mounting.

APPLICATIONS

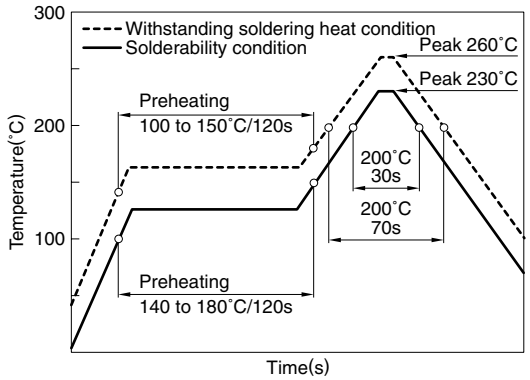
Portable audio visual devices (DSCs, DVCs, etc.)
Mobile communication devices (cellular phones, etc.)
Information devices (PCs, etc.)

SPECIFICATIONS

Operating temperature range	–40 to +105°C [Including self-temperature rise]
Storage temperature range	–40 to +105°C

RECOMMENDED SOLDERING CONDITIONS

REFLOW SOLDERING



PRODUCT IDENTIFICATION

GLFR	1608	T	100	M	-	LR
(1)	(2)	(3)	(4)	(5)		(6)

(1) Series name

(2) Dimensions

1608	1.6×0.8mm

(3) Packaging style

T	Taping

(4) Inductance

1R0	1µH
100	10µH
101	100µH

(5) Inductance tolerance

M	±20%

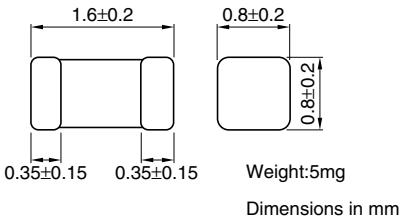
(6) TDK internal code

PACKAGING STYLE AND QUANTITIES

Packaging style	Quantity
Taping	4000 pieces/reel

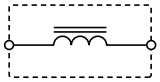
- Conformity to RoHS Directive: This means that, in conformity with EU Directive 2002/95/EC, lead, cadmium, mercury, hexavalent chromium, and specific bromine-based flame retardants, PBB and PBDE, have not been used, except for exempted applications.
- Please contact our Sales office when your application are considered the following:
  The device's failure or malfunction may directly endanger human life (e.g. application for automobile/aircraft/medical/nuclear power devices, etc.)

SHAPES AND DIMENSIONS/CIRCUIT DIAGRAM/RECOMMENDED PC BOARD PATTERN

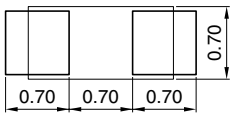


Weight:5mg

Dimensions in mm



• No polarity



Dimensions in mm

ELECTRICAL CHARACTERISTICS

Inductance (μH)	Inductance tolerance (%)	DC resistance (Ω)±30%	Rated current*1 (mA)max.	Rated current*2 (mA)max.	Rated current*3 (mA)max.	Part No.
0.35	±20	0.04	330	500	1200	GLFR1608TR35M-LR
0.47	±20	0.05	300	475	1100	GLFR1608TR47M-LR
0.55	±20	0.05	250	400	1100	GLFR1608TR55M-LR
1	±20	0.08	230	360	900	GLFR1608T1R0M-LR
1.5	±20	0.15	170	260	625	GLFR1608T1R5M-LR
2.2	±20	0.17	160	240	600	GLFR1608T2R2M-LR
3.3	±20	0.23	120	190	525	GLFR1608T3R3M-LR
4.7	±20	0.24	110	170	500	GLFR1608T4R7M-LR
6.8	±20	0.35	90	135	400	GLFR1608T6R8M-LR
10	±20	0.36	80	120	400	GLFR1608T100M-LR
15	±20	0.9	55	75	220	GLFR1608T150M-LR
22	±20	1	50	70	200	GLFR1608T220M-LR
33	±20	2.2	40	60	120	GLFR1608T330M-LR
47	±20	2.3	35	50	100	GLFR1608T470M-LR
68	±20	4	20	35	90	GLFR1608T680M-LR
100	±20	5.5	15	25	80	GLFR1608T101M-LR

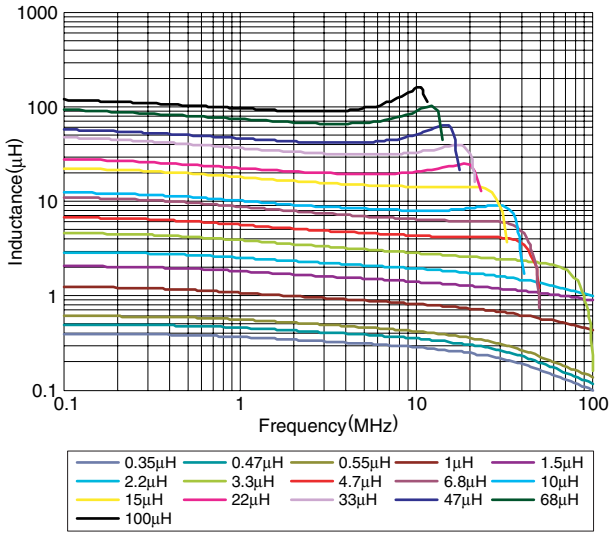
*1 Rated current based on inductance variation: Current when inductance decreases by 10% of the initial value due to direct current superimposed characteristics

*2 Rated current based on inductance variation: Current when inductance decreases by 30% of the initial value due to direct current superimposed characteristics

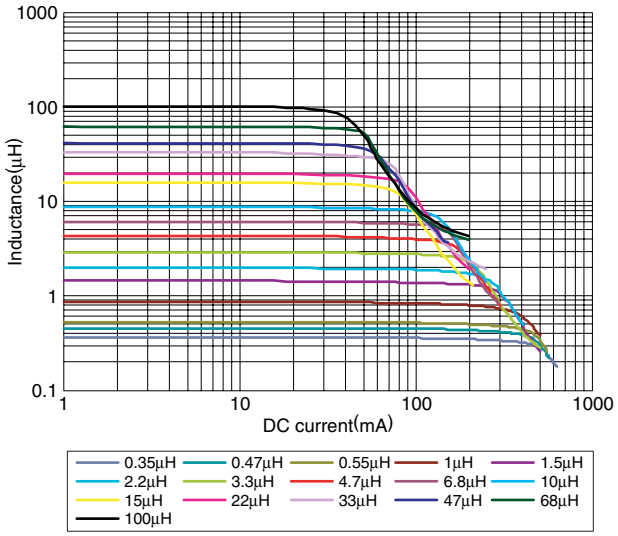
*3 Rated current based on increasing product temperature: Current when temperature of the product reaches +20°C

TYPICAL ELECTRICAL CHARACTERISTICS

INDUCTANCE vs. FREQUENCY CHARACTERISTICS

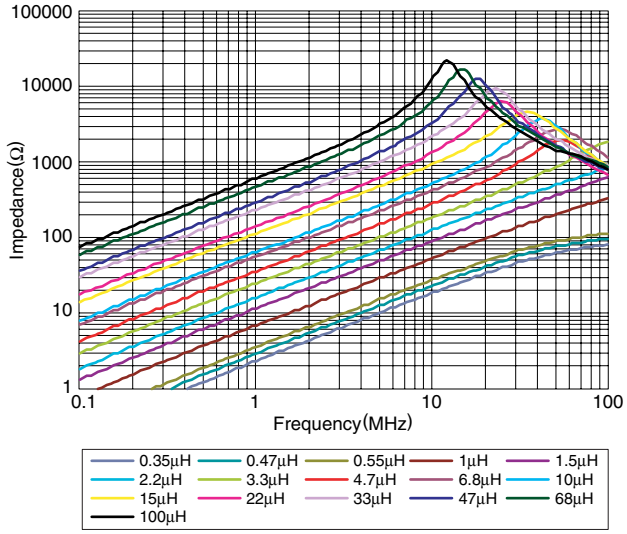


INDUCTANCE vs. DC SUPERPOSITION CHARACTERISTICS

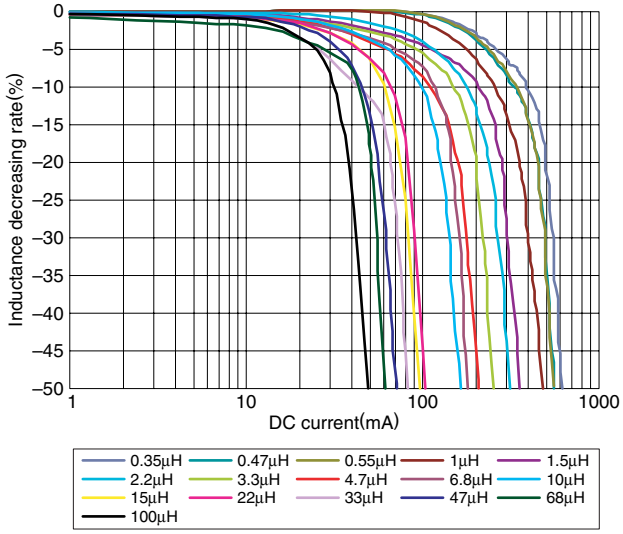


TYPICAL ELECTRICAL CHARACTERISTICS

IMPEDANCE vs. FREQUENCY CHARACTERISTICS



DC SUPERPOSITION vs. INDUCTANCE DECREASING RATE



2.3. PROGRAMA

2.3.1. Programa Coche:

```
#include <dummy.h> //libreria general esp32
#include <WiFi.h> //libreria servidor wifi esp32
#include <SPI.h> //libreria SPI

const char   *ssid      = "Copidron";
const char   *pass      = "1234Copidron";
const int    RESET      = 6;
const int    CS2        = 7;
const int    MOSI_pin   = 9;
const int    MISO_pin   = 8;
const int    CLK        = 10;
const int    CS1        = 11;
const int    GPS_ON     = 30;
struct spi_bus_config_t {
  int mosi_io_num     = MOSI_pin;
  int miso_io_num     = MISO_pin;
  int sclk_io_num     = CLK;
  int quadwp_io_num   = -1;
  int quadhd_io_num   = -1;
  int max_transfer_sz = 0;
};


void setup()
{
 //Configuramos los pines del gps y de la pantalla
 pinMode (CS1, OUTPUT);
 pinMode (CS2, OUTPUT);
 pinMode (GPS_ON, OUTPUT);
 digitalWrite(GPS_ON, HIGH);

 //Configuramos el Access Point WiFi.
 WiFi.mode(WIFI_AP);
 WiFi.softAP(ssid, pass);


}

void loop()
{


}
```

2.3.2. Programa Dron

```
#include <dummy.h>
#include <WiFi.h>
#include <SPI.h>
#include <SPIFFS.h>

const int GPS_ON     = 6;
const int CS4        = 7;
const int MOSI_pin   = 8;
const int MISO_pin   = 9;
const int CS1        = 11;
const int CS2        = 12;
const int CS3        = 13;
const int TRIG       = 14;
const int U3         = 26;
const int ML1        = 27;
const int MD2        = 30;
const int MD1        = 31;
const int ML2        = 33;
const int RXD        = 34;
const int TXD        = 35;
const int U2         = 36;
const int U1         = 37;
const float alturaref = 3;
long alturat;
long obstaculo1;
long obstaculo2;
static float altura;
static bool parar;
static bool bajar;
static float loncoche;
static float latcoche;
static float londron;
static float latdron;
float dlon;
float dlat;
float dlonkm;
float dlatkm;
float distcochedron;
const float distcochedronref = 50;

void setup() {
  pinMode (GPS_ON, OUTPUT);
  pinMode (CS1, OUTPUT);
  pinMode (CS2, OUTPUT);
  pinMode (CS3, OUTPUT);
  pinMode (CS4, OUTPUT);
  pinMode (TRIG, OUTPUT);
  pinMode (U1, INPUT);
  pinMode (U2, INPUT);
  pinMode (U3, INPUT);
  pinMode (ML1, OUTPUT);
  pinMode (ML2, OUTPUT);
  pinMode (MD1, OUTPUT);
  pinMode (MD2, OUTPUT);
```

```
  //inicializar camara
  //conectar a wifi
}

void comprobarUS () {
  //Mandamos el pulso por los 3 ultrasonidos
  digitalWrite(TRIG, LOW);
  delayMicroseconds (2);
  digitalWrite(TRIG, HIGH);
  delayMicroseconds(10);
  digitalWrite(TRIG, LOW);
  //Registramos los ecos
  alturat = (pulseIn(U1, HIGH) / 2);
  obstaculo1 = (pulseIn(U2, HIGH) / 2);
  obstaculo2 = (pulseIn(U3, HIGH) / 2);
  //Hacemos el calculo de la altura a la que estamos
  altura = float(alturat * 1 / 1000000 * 343);
  if (altura = alturaref) {//Si la altura es la de referencia
    if (obstaculo1 > 14578) {//Si no hay obstáculo
      parar = false;
      bajar = false;
      //seguir volando
    }
    if (obstaculo1 < 14578) {//Si sí que hay obstáculo
      //Parar
      parar = true;
      //Bajar 0.5m altura
      bajar = true;
      //Volvemos a comprobar si hay obstáculo
      //Mandamos el pulso
      digitalWrite(TRIG, LOW);
      delayMicroseconds(2);
      digitalWrite(TRIG, HIGH);
      delayMicroseconds(10);
      digitalWrite(TRIG, LOW);
      //Registramos altura y presencia de obstáculo
      alturat = (pulseIn(U1, HIGH) / 2);
      obstaculo1 = (pulseIn(U2, HIGH) / 2);
      //Calculamos altura
      altura = float(alturat * 1 / 1000000 * 343);
      if (obstaculo1 > 14578) {//Si ya no hay obstáculo
        parar = false;
        bajar = false;
        //seguir volando
      }
      if (obstaculo1 < 14578) {//Si sigue habiendo obstáculo
        //Bajar 0.5m altura
        bajar = true;
        //Volvemos a comprobar si hay obstáculo
        //Mandamos el pulso
        digitalWrite(TRIG, LOW);
        delayMicroseconds(2);
        digitalWrite(TRIG, HIGH);
        delayMicroseconds(10);
        digitalWrite(TRIG, LOW);
        //Comprobamos la presencia de obstáculo
        obstaculo1 = (pulseIn(U2, HIGH) / 2);
```

```
      if (obstaculo1 > 14578) { //Si ya no hay obstáculo
        parar = false;
        bajar = false;
        //seguir volando
      }
      if (obstaculo1 < 14578) { //Si sigue habiendo obstáculo
        //Error
        bajar = false;
        parar = true;
      }
    }
  }
 }

 if (altura != alturaref) {//Si la altura es distinta a la de referencia
  if (obstaculo2 < 1458) {//Si tenemos obstáculo por arriba a menos de 0,5m
   //mantener altura
  }
  if (obstaculo2 > 1458) {
   if (obstaculo2 > 2916) {
    //subir 1m
   }
   if (obstaculo2 < 2916) {
    //subir 0,5m
   }
  }
 }
}

void distanciacochedron() {
 //calculamos la diferencia en latitud y longitud entre dron y coche
 dlon = float(loncoche - londron);
 dlat = float(latcoche - latdron);
 //Transformamos la diferencia a Km
 dlatkm = float(39941.580 / 360 * dlat);
 dlonkm = float(cos(londron) * 6367.6 / 360 * dlon);
 //Calculamos la distancia del coche al dron en m.
 distcochedron = float(dlat*1000 + dlon*1000);
 distcochedron = float(distcochedron*distcochedron);
 distcochedron = float( sqrt(distcochedron));
 if (distcochedron > distcochedronref) {
  parar = true;
 }
 if (distcochedron < distcochedronref) {
  parar = false;
 }
}

void loop() {
 //Obtener datos SPI
 obtenerdatos();
 //asignamos latitudes del dron y del coche a las variables
 distanciacochedron();
 if (parar = true){
  //paramos el dron
 }
 if (parar = false){
```

```
    comprobarUS();
  }

}
```

Relación de documentos

(_) Memoria ..... 62 páginas

(X) Anexos .....288 páginas

La Almunia, a 08 de 11 de 2017

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