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Trabajo Fin de Grado

Diseño de un dron de vigilancia controlado de forma remota por teléfono móvil

Design of a surveillance drone remotely controlled by smartphone

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ESCUELA UNIVERSITARIA POLITÉCNICA
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MEMORIA

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INDICE DE CONTENIDO

INDICE DE ILUSTRACIONES

INDICE DE TABLAS

1. RESUMEN

El uso de drones es uno de los campos que mayor evolución está teniendo dentro del campo de la robótica aérea. Este sector abarca infinidad de posibilidades y se puede utilizar en múltiples tareas. Esta es la razón por la que su interés, tanto a nivel usuario como a nivel empresarial, haya experimentado un elevado crecimiento y el futuro de estas tecnologías se presente lleno de posibilidades. El objetivo de este Trabajo Fin de Grado es el diseño de un cuadricóptero que permita vigilar una determinada instalación de forma remota.

Para alcanzar este objetivo se han seguido una serie de pasos. En primer lugar, se ha establecido el empuje necesario para este tipo de drones (3 Kg) así como la relación empuje/peso para el tipo de vuelo a realizar. A continuación, se ha calculado la relación potencia/empuje parametrizando la velocidad máxima estimada (60 Km/h). Con los resultados obtenidos se halla la potencia, se escoge un paso (3) y se fija la tensión de alimentación de los motores (12 V). Una vez realizado este proceso se han elegido los modelos comerciales de los motores y las hélices que se van a montar en el cuadricóptero.

Posteriormente se ha realizado el diseño en 3D del dron tomando como referencia varios modelos de cuadricópteros existentes en el mercado. Para ello se ha utilizado el software Autodesk Inventor.

El siguiente proceso ha sido el diseño electrónico para el cuál se han analizado diversos tipos de componentes comerciales para escoger los que más se ajustan a las necesidades establecidas. Se ha realizado el diseño del circuito por medio del programa KiCAD para, por medio del mismo, crear la PCB (Placa de Circuito Impreso).

Por último, se ha realizado el diseño del algoritmo de control que permita al dron, por medio de los componentes electrónicos establecidos previamente, realizar correctamente las funciones propuestas.

2. ABSTRACT

The use of drones is one of the fields which more evolution is experiencing in the aerial robotics area. This sector encompasses a huge number of possibilities and can be used in multiple tasks. This is the reason why its interest, at user and managerial level, has experienced a high growth and the future of these technologies is full of possibilities. The objective of this Final Project is the design of a quadcopter that monitors a particular installation remotely.

To achieve this, it has been followed a series of steps. Firstly, it has been established the necessary thrust for this type of drone (3 Kg) and the thrust/weight relation for the type of flight to be performed. Then, it has been calculated the power/thrust relation setting the estimated top speed (60km/h). With the results, the power is found and the supply voltage of the motors (12 V) is fixed. Once this process has been finished, the commercial models of engines and propellers are chosen to be mounted on the quadcopter.

Subsequently, it has been made the 3D drone design with reference to several quadcopter models on the market. With this aim, the Autodesk Inventor software was used. The following process has been the electronic design for which it has been analyzed various types of commercial components in order to choose the best options for the identified needs. The circuit has been designed through the program KiCAD to, by the same, create the PCB (Printed Circuit Board).

Finally, it has been designed the control algorithm that allows the drone, through the electronic components previously established, to perform successfully the proposed functions.

3. INTRODUCCIÓN

3.1. OBJETIVO

El *objetivo* de este proyecto es **diseñar un dron cuadricóptero** con cámara de vigilancia para captar imágenes que permitan supervisar de forma remota alguna instalación. Para ello se van a plantear una serie de *objetivos secundarios*:

- Diseñar la parte mecánica que contenga en su interior todos los elementos, tanto electrónicos como mecánicos, intentando ajustar las dimensiones y el peso a las necesidades de un óptimo funcionamiento.
- Diseñar la parte electrónica de forma que el sistema realice correctamente las funciones de locomoción, visión artificial y detección.
- Diseñar la parte de control que permita la monitorización por software de forma remota mediante una interfaz externa a través de un teléfono móvil.

3.2. METODOLOGÍA

El proyecto consiste en **diseñar un dron que permita el manejo a distancia por medio de un teléfono móvil**, de manera que podemos visualizar las imágenes recibidas por la videocámara que contiene y, en caso de observar situaciones anómalas, detectadas por una cámara infrarroja, realizar automáticamente una captura fotográfica y mandar un mensaje de alerta al usuario.

Estudio: Tarea dedicada a buscar información y entender las diferentes tecnologías, fundamentos y teorías necesarias para el dron.

Desarrollo: Diseño e implementación del proyecto en sus distintas partes acordes al estudio realizado previamente.

Seguimiento: Parte destinada a revisar el desarrollo del trabajo realizando los ajustes necesarios para su correcto funcionamiento.

Verificación: Comprobación de la fiabilidad del dron, así como de cada una de sus partes.

3.3. ANTECEDENTES

En el ámbito comercial existen varios modelos de cuadricópteros disponibles en el mercado, tales como el AR.Drone. Este dron utiliza señal Wifi para comunicarse a una plataforma móvil. El aparato puede retransmitir imágenes de alta calidad en tiempo real, además de ofrecer información de vuelo. El modelo ofrece algunas configuraciones adicionales, tales como intercambiar el tipo de batería por alguno de mayor capacidad, personalizar la estructura del chasis y diferentes funcionalidades digitales como programar el plan de vuelo o compartir información entre usuarios.

Ilustración 1:AR Drone

Existe otro modelo en el mercado, el Phantom. Éste ofrece comunicación por radiocontrol a través de un mando, lo cual obliga al usuario a estar situado en una zona física para poder emplear la aeronave. A cambio, este producto ofrece funcionalidades de gran interés como las que tiene el AR.Drone, programar el plan de vuelo, que por la tecnología RC se puede hacer a una distancia mayor que la de AR.Drone. Tiene una funcionalidad adicional que es auto detectar si se ha salido del perímetro de cobertura máxima y si es así, el cuadricóptero regresa automáticamente hasta el punto de inicio.(GenLei, 2014)

Ilustración 2: DJI Phantom

4. MARCO TEÓRICO

La robótica aérea permite el desarrollo de diversas tareas que cubren diferentes funciones en múltiples sectores como la investigación, la seguridad, la agricultura y el medio ambiente entre otras. El interés de estas tecnologías, tanto por parte de empresas como de los usuarios, ha aumentado potencialmente durante los últimos años. Uno de los campos donde tiene más posibilidades de aplicación es el de la videovigilancia. En el mismo se abarcan diferentes disciplinas como la robótica, electrónica, mecánica e informática cuyo fin es obtener datos de localización, imágenes e información útil de forma que pueda actuar y resolver de una manera más rápida y eficaz las situaciones específicas para las que está diseñado.(Silva Bohórquez, Mendoza, & Peña Cortés, 2013)

4.1. PROBLEMA DE SEGURIDAD Y APLICACIONES DE VIGILANCIA

Existen multitud de métodos para mantener una determinada infraestructura vigilada de intrusos o situaciones anómalas que pueden causar desperfectos en la misma. Uno de los más utilizados es la vigilancia de esa zona de forma remota a distancia, para ello se suelen disponer diversas cámaras fijas distribuidas en el interior del recinto siendo programada su grabación de forma externa.

Actualmente, se dispone de drones que realizan este mismo proceso, pero de una forma más cómoda y eficaz para el usuario, ya que, al no ser elementos fijos, abarcan mayor ángulo de visión que las cámaras fijas, pueden variar su posición según las exigencias de la situación y pueden ser controlados a distancia amoldándose de mejor forma a las circunstancias y exigencias del usuario en un determinado momento, por ello, en este proyecto se va a diseñar un sistema de vigilancia de estas características.

4.2. JUSTIFICACIÓN DEL MODELO CUADRICÓPTERO

Cada tipo de dron varía en diversas características, como es el coste, consumo eléctrico o estabilidad durante el vuelo.

Como regla sencilla, a mayor cantidad de motores, el dron tiene mayor estabilidad, pero a su vez más peso, lentitud y consumo de energía.

De este modo, el tricóptero tiene tres brazos y tres motores, simplificando así la ecuación eléctrica en consumo, cables y partes. Como resultado también se simplifica su armado, a la vez que su coste de reparación ante eventuales accidentes. Por el contrario, este tipo de configuración es más inestable porque únicamente tiene tres puntos de sustentación, menor capacidad de carga debido a que sólo cuenta con tres motores para generar fuerza de empuje.

Por otro lado, el cuadricóptero, al contar con cuatro brazos y un motor en cada punta de los mismos, cuenta con mayor estabilidad y capacidad de carga. En caso de filmación y fotografía, se gana mayor estabilidad al utilizar un cuerpo de cuadricóptero, comenzando los brazos para cada motor en cada vértice del rectángulo, ya que así se gana mayor superficie para la electrónica y un poco más de superficie para cada motor, aportando un extra de estabilidad.

De esta forma, en este proyecto se va a utilizar un cuadricóptero ya que es más estable, dispone de mayor capacidad de carga que los tricópteros y además la cámara dispone de un campo de visión superior que en configuraciones con mayor número de motores.

4.3. DRON CUADRICÓPTERO

Un cuadricóptero es una aeronave de ala giratoria, propulsada por cuatro rotores. Al ser un tipo de helicóptero, tanto la sustentación como la propulsión se basan en el aire impulsado por las hélices de sus rotores. En cambio, a diferencia de los helicópteros, que varían el ángulo de inclinación de las palas de las hélices para maniobrar, los cuadricópteros basan sus maniobras en el cambio de revoluciones de sus distintos motores. De esta forma usan hélices con palas de paso fijo que simplifican en gran medida la mecánica de este tipo de aeronaves. (Omar Luque Rodríguez, 2014)

4.4. CONFIGURACIONES DE CUADRICÓPTERO

Existen dos tipos de configuraciones de cuadricópteros, los de tipo en aspa y los de tipo en cruz. Estas denominaciones se deben a lo que es considerado como la parte delantera de la aeronave.

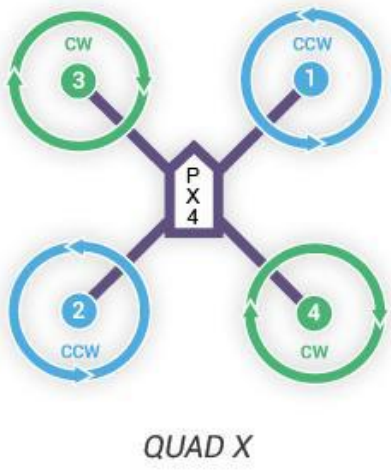

Ilustración 3: Configuración en aspa

En un cuadricóptero configurado en aspa, se tienen dos rotores delanteros y dos rotores traseros. Este tipo de montaje es más popular para llevar cámaras frontales en ellos, pues la cámara no tiene ningún brazo en su campo de visión.

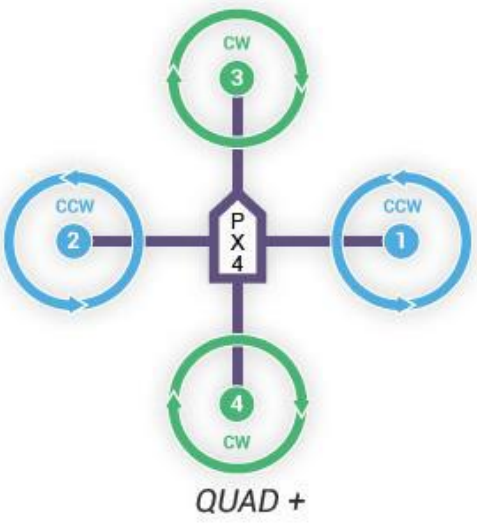

Ilustración 4: Configuración en cruz

De otro modo, la configuración en cruz conlleva tener un rotor delantero, uno trasero, uno izquierdo y uno derecho. Esta configuración suele ser más sencilla de

programar y entender, pero no está pensada para incluir cámaras frontales debido a que el campo de visión se vería interrumpido por las hélices.

Últimamente, han aparecido otros dos tipos de cuadricópteros, cuyos rotores no están colocados formando un cuadrado, los del tipo Y4 y los VTail. Por definición son cuadricópteros, pero su comportamiento y forma es similar al de los tricópteros, aunque aumentan la estabilidad de estos últimos gracias a tener un número par de rotores.

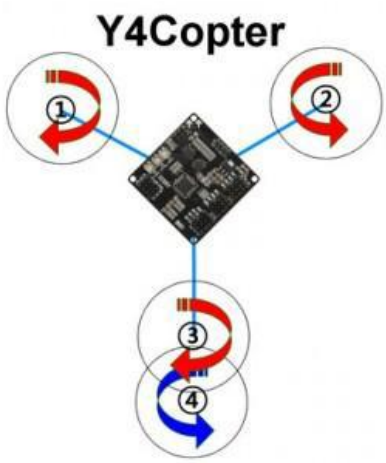

Ilustración 5: Configuración Y4

La configuración Y4 consiste en una estructura en forma de Y, teniendo en su parte delantera dos rotores y otros dos rotores coaxiales en la cola. Esta forma es una evolución de los tricópteros convencionales, pero evitando el servo necesario para el giro sobre el eje vertical usando los dos rotores coaxiales, girando en dirección contraria el uno del otro. Con esto se logra alrededor de 1/3 más de fuerza de sustentación y una mayor estabilidad y fiabilidad, pues no se depende de ningún servo.

Ilustración 6: Configuración VTail

La configuración VTail corresponde a una mezcla entre los cuadricópteros en x y los tricópteros. Como los cuadricópteros, tiene dos rotores delanteros y dos traseros, pero estando los delanteros colocados cada uno sobre un brazo los traseros se encuentran sobre un único brazo trasero colocado uno a cada lado de su extremo, he

inclinados alrededor de él en un ángulo determinado. Esta configuración no es muy popular, debido a que es menos eficiente que la Y4 y a que su control de motores es algo más complicado. Pero, por otra parte, es una configuración más estable, y su orientación es más reconocible a distancia gracias a su clara distinción entre cabeza y cola.(Omar Luque Rodríguez, 2014)

4.5. CÁMARA DE VISIÓN ARTIFICIAL

La visión artificial es una herramienta para establecer la relación entre el espacio real y sus vistas bidimensionales. Una cámara de visión artificial permite hacer una reconstrucción del espacio tridimensional a partir de sus vistas y también llevar a cabo una simulación de una escena tridimensional en la posición deseada a un plano bidimensional.(Mery, 2004)

4.6. RIESGOS

Estos aparatos, al ser controlados remotamente y enviar datos, pueden conllevar una serie de riesgos como son los posibles accidentes causados por la pérdida de control de los mismos, así como infringir la protección de datos personales. Con objeto de intentar minimizar estos riesgos de la mejor forma posible, el pilotaje y características del sistema deberán ajustarse al Real Decreto Ley 18/2014, que regula el horario, tiempo y características de cada vuelo, además de ser necesario un permiso especial para pilotar drones dependiendo del tamaño y potencia de los mismos.(Hogan Lovells, 2014).

4.7. SENSORES

4.7.1. Acelerómetro

Los acelerómetros son sistemas que miden el efecto de la fuerza de gravedad sobre ellos mismos, al disponer de 3 acelerómetros formando 3 ejes ortogonales, el aumento de percepción de gravedad en uno de los ejes indica que este se está poniendo en vertical, incidiendo toda la fuerza de gravedad sobre él.

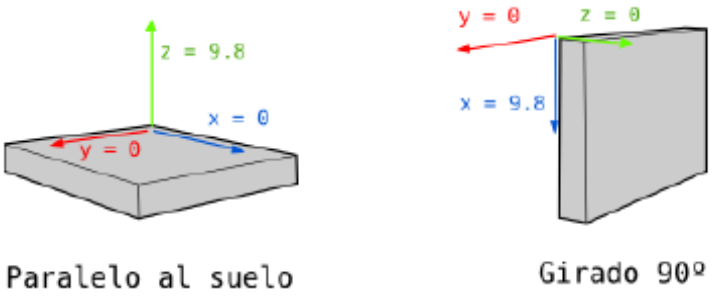

Ilustración 7: Percepción del acelerómetro en función de su posición respecto al campo gravitatorio

Estos dispositivos utilizan la tecnología MEMS.

La tecnología MEMS (Micro Electro Mecanical Systems) ha logrado reducir a tamaños muy pequeños la fabricación de sistemas que combinan elementos mecánicos y electrónicos.

Este tipo de tecnología logra construir microestructuras móviles sobre un sustrato. Esto permite la creación de sistemas eléctricos y mecánicos muy complejos.

Utiliza un material piezoeléctrico de estado casi sólido, suele ser cuarzo, cargado eléctricamente tiene sobre sí una masa conocida y se comprime en función de la gravedad que actúa sobre él. Esta presión produce una alteración en la alineación de los electrones y protones en el material piezoeléctrico lo que provoca una acumulación de cargas opuestas en ambas superficies del material percibiéndose así una variación en la carga eléctrica que resulta proporcional al esfuerzo experimentado por el material, el cual es proporcional a la aceleración de la gravedad por la segunda ley de Newton. Esta variación correctamente tratada ayuda a tomar la medida de la cantidad de inclinación que tiene un eje, con una serie de cálculos trigonométricos se determina el giro del eje. (J. Adams, 2011)

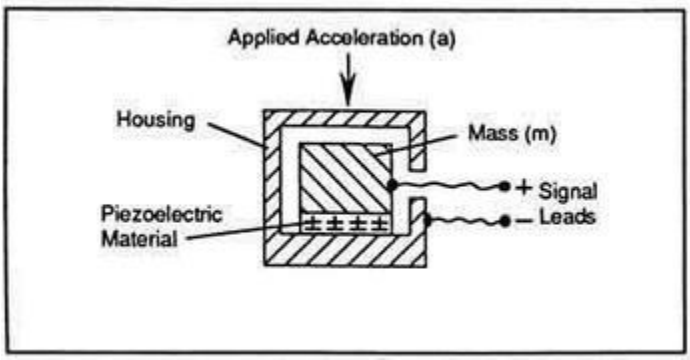

Ilustración 7: Esquema de construcción de un acelerómetro MEMS

El ángulo de giro de un eje, vendrá definido por una combinación del peso percibido en cada uno de los 3 ejes. A continuación, se va a explicar el procedimiento de cálculo.

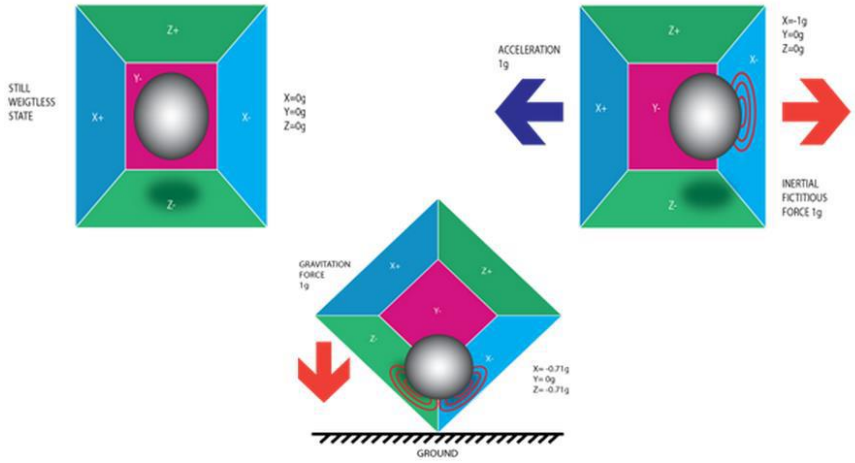

Ilustración 8: Representación del comportamiento de un acelerómetro MEMS

Imaginemos un cubo cuya base xy reposa sobre el plano de referencia xy e imaginemos un sistema de coordenadas xyz de referencia cuyo eje x de referencia coincide con una arista del cubo.

Ahora supongamos que giramos el cubo un ángulo θ con el eje x como centro de revolución, al terminar el giro la base del cubo xy forma un ángulo θ con el plano de referencia xy. La lectura del acelerómetro x, sería prácticamente 0 por lo tanto el cálculo del ángulo de giro sería:

$$\theta_x = tan^{-1}(\frac{lectura\ acelerómetro\ y}{lectura\ acelerómetro\ z})$$

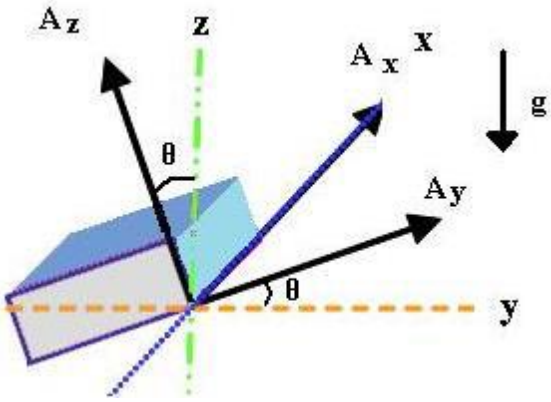

Ilustración 9: Representación del giro de un objeto respecto del eje X

Así como hemos inclinado el plano de la base del cubo un ángulo θ respecto al plano de referencia, el plano xz del cubo también se ha desplazado un ángulo θ_x respecto al plano de referencia.

En el momento en el que se haga un segundo giro, sobre el eje xy del cubo, por ejemplo, la lectura del acelerómetro y va a seguir siendo la misma ya que esto viene determinado por la inclinación del eje y respecto al plano xy de referencia y esta no se modifica.

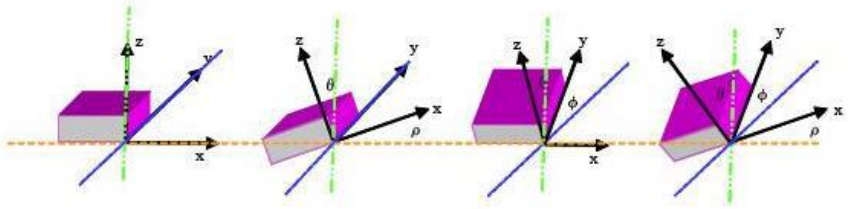

Ilustración 10: Representación del giro de un cuerpo respecto de los tres ejes de coordenadas

Los ejes z y x del cubo se desplazarán a lo largo del plano xz del cubo, recordemos que este se encuentra a θ grados de xz de referencia, la lectura del acelerómetro z va a disminuir al ritmo que aumenta la del acelerómetro x, sin embargo, la suma de los módulos de los acelerómetros z y x siempre va a ser constante e igual al valor que transmitía el acelerómetro z al completar el primer giro, ya que el valor en el eje x era 0.

$$\theta_x = tan^{-1}\frac{A_y}{\sqrt{{A_x}^2 + {A_z}^2}}$$

$$\theta_x = tan^{-1}\frac{A_x}{\sqrt{{A_y}^2 + {A_z}^2}}$$

4.7.1. Giroscopio

El giróscopio en un aparato que mide la orientación de un objeto en el espacio, fue desarrollado por Foucault en 1852 aunque hubo ideas parecidas desde 1813, con el alemán Johann Bohnenberger a quien se le atribuye el descubrimiento del efecto giroscópico. (Shane Colton, 2007)

En aquellas fechas estos aparatos eran sistemas mecánicos, lo que reducía sus aplicaciones al ámbito militar debido a su tamaño y peso. En los últimos años, con el desarrollo de la electrónica y mecánica, se han desarrollado giróscopos MEMS, basados

en el efecto coriolis para hallar sus medidas, eliminando el problema del tamaño y el peso. (K. Ogata, 2003)

Este efecto se da en todos los cuerpos de rotación, consiste en la distinta percepción del movimiento al observar desde un sistema de referencia rotatorio (no inercial) a un objeto que se encuentra fuera de este sistema de referencia.

La fuerza de coriolis no existe por sí misma, pero es necesario incluirla si deseamos explicar el funcionamiento del sistema con las leyes de Newton. Podría afirmarse que los sistemas inerciales no existen como tal, ya que la propia Tierra es un sistema no inercial al estar girando sobre sí misma y, a su vez, alrededor del Sol. Sin embargo, se aceptan ciertas consideraciones para simplificar los cálculos y en la mayoría de ocasiones la tierra se considera un sistema inercial.

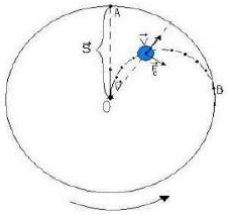

Ilustración 11: Representación del efecto coriolis

Como se puede observar en la ilustración, la fuerza coriolis aparece en perpendicular al eje de rotación y a la velocidad de desplazamiento del objeto. La velocidad de giro del sistema no inercial provoca una variación en la posición relativa del objeto. Este mismo principio utilizan los giróscopos MEMS.

El giróscopo MEMS dispone de 2 masas con cierta movilidad obtenida por medio de materiales flexibles. Para que las masas perciban el efecto coriolis deben desplazarse, esto se logra aplicando una vibración a las mismas mediante la interacción de campos electromagnéticos. Al actuar el efecto coriolis el recorrido previsto se ve alterado.

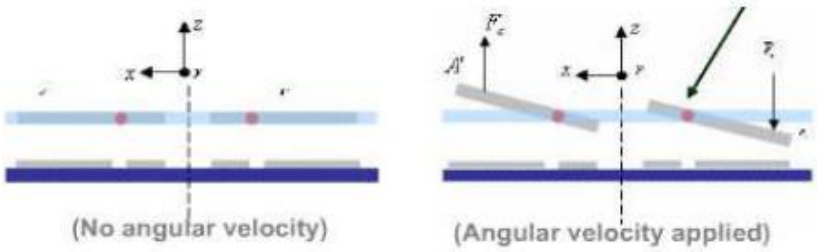

Ilustración 12: Representación de la variación de la posición de las massas internas del giroscopio

Al cambiar sus posiciones, las masas varían su distancia respecto a unos sistemas capacitores que tienen debajo obteniendo una variación capacitiva que pasa a través de un amplificador operacional para enviarlas por medio de variaciones eléctricas fácilmente cuantificables que finalmente serán traducidas a velocidades de giro.

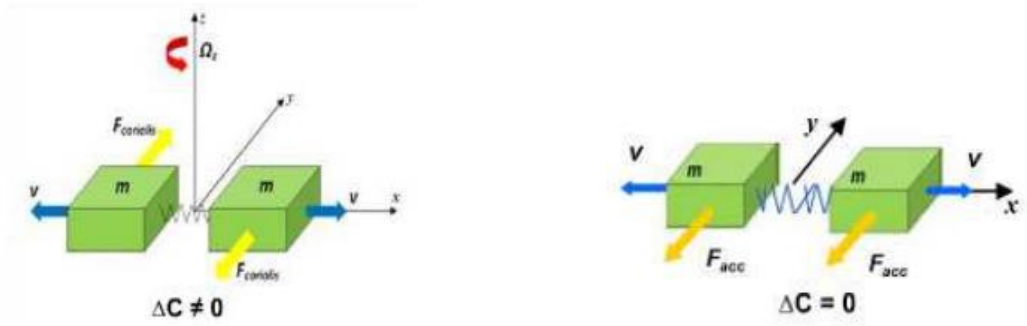

Ilustración 13: Efecto de los movimientos en giroscopio y acelerómetro

Aplicando la medida diferencial entre los resultados de las masas se consigue eliminar una falsa medida de giro que podría ser provocada por una aceleración lineal.

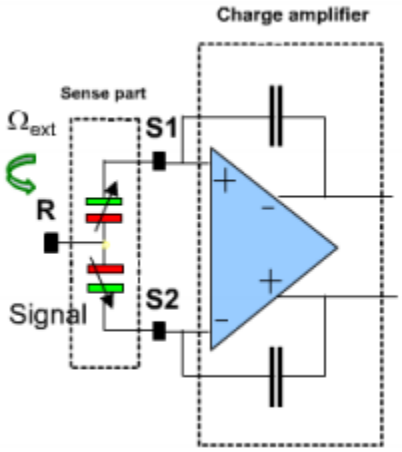

Ilustración 14: Medida diferencial y amplificación de señal

Para hacer los cálculos se debe observar que se obtiene una medida de la velocidad de giro, por lo que hay que traducir en ángulos la medida obtenida y conocer la inclinación, para lograr esto se integra la velocidad angular.

$$\omega = \frac{d\theta}{dt} \rightarrow \theta = d\omega \cdot dt$$

Traduciendo esta ecuación a programación, la integral se realiza obteniendo el valor de la velocidad y teniendo en cuenta el tiempo que le cuesta al programa completar un ciclo. Este tiempo de ciclo es el dt, cuanto menor sea más rápido obtendremos valores.

Conocido el tiempo de cada ciclo y la velocidad de giro que reporta el giróscopo se calcula la distancia angular recorrida desde la anterior medición. Este valor se añade al ángulo en el que se encontraba el sensor en el instante de muestreo anterior.

Tener que obtener los valores a través de realizar una integral provoca un pequeño error acumulativo en lo que se conoce como el "drift" propio del giróscopo, llegando a sacar valores que difieren mucho de la realidad. Este valor acumulativo se produce como consecuencia de sumar repetidamente el error estático del giróscopo a lo largo del tiempo. (Digi International Inc, 2015)

4.7.1. Magnetómetro

Un magnetómetro es un instrumento que mide la intensidad y, en ocasiones, la dirección de un campo magnético.

Los magnetómetros se usan, mayoritariamente, para la medición del campo magnético terrestre y en estudios geofísicos, para detectar anomalías magnéticas de diferentes tipos.

En la actualidad más reciente, los magnetómetros han sido miniaturizados, con el objetivo de ser incorporados en circuitos integrados a un coste muy bajo. También ha aumentado su uso como brújula en dispositivos electrónicos como móviles.

Los magnetómetros pueden ser divididos en dos tipos básicos:

Magnetómetros escalares, que miden la intensidad total del campo magnético resultante al cual están siendo sometidos en un punto, pero no aporta ningún dato sobre las componentes vectoriales de campo.

Magnetómetros vectoriales, que tienen la capacidad de medir la intensidad del campo magnético en una dirección particular, dependiendo de la colocación que le demos al dispositivo. Este tipo de magnetómetros va a ser el utilizado para el proyecto.

Un magnetómetro vectorial mide una o más componentes del campo magnético electrónicamente. Usando tres magnetómetros ortogonales se podría calcular todo el campo magnético en un punto. Realizando la raíz cuadrada de la suma de los cuadrados de los tres componentes, se halla el valor de la resultante en módulo mediante el teorema de Pitágoras.

$$B_T = \sqrt{{B_X}^2 + {B_Y}^2 + {B_Z}^2}$$

Los magnetómetros vectoriales están sujetos a cambios de temperatura y a la inestabilidad dimensional de núcleos férricos. Además, requieren de una buena nivelación para obtener la información.(García García, 2013)

4.7.1. GPS

4.7.1.1. Definición del sistema GPS

El Sistema de Posicionamiento Global (GPS) es un sistema de localización, diseñado por el Departamento de Defensa de los Estados Unidos con fines militares para proporcionar estimaciones precisas de posición, velocidad y tiempo; se encuentra operativo desde 1995 y utiliza conjuntamente una red de ordenadores y una constelación de 24 satélites para determinar por triangulación, la altitud, longitud y latitud de cualquier objeto en la superficie terrestre.(J.A. Fernández Rubio, 1997)

4.7.1.2. Arquitectura del sistema GPS

El sistema se descompone en tres segmentos, los dos primeros son de responsabilidad militar: segmento espacio, formado por 24 satélites GPS con una órbita de 26560 Km. de radio y un periodo de 12 h.; segmento control, que consta de cinco estaciones monitoras encargadas de mantener en órbita los satélites y de supervisar su correcto funcionamiento, tres antenas terrestres que envían a los satélites las señales que deben transmitir y una estación experta de supervisión de todas las operaciones; y segmento usuario, formado por las antenas y los receptores pasivos situados en tierra. Los receptores, a partir de los mensajes que provienen de cada satélite visible, calculan distancias y proporcionan una estimación de posición y tiempo.

4.7.1.3. Principios de funcionamiento del sistema GPS

El sistema GPS tiene como objetivo calcular la posición de un punto cualquiera en un espacio de coordenadas (x,y,z), partiendo del cálculo de las distancias del punto a un mínimo de tres satélites cuya localización es conocida. La distancia entre el usuario y un satélite se mide multiplicando el tiempo de vuelo de la señal emitida desde el satélite por su velocidad de propagación. Para medir el tiempo de vuelo de la señal de radio es necesario que los relojes de los satélites y de los receptores estén sincronizados, ya que deben generar simultáneamente el mismo código. Mientras que los relojes de los satélites son muy precisos los de los receptores son osciladores de cuarzo de bajo coste y por tanto imprecisos. Las distancias con errores debidos al sincronismo se denominan pseudodistancias. La desviación en los relojes de los receptores añade una incógnita más que hace necesario un mínimo de cuatro satélites para estimar correctamente las posiciones.(G.J. Sonnenberg, 1988)

En el cálculo de las pseudodistancias hay que observar que las señales GPS son muy débiles y se hallan inmersas en el ruido de fondo inherente al planeta en la banda de radio. Este ruido natural está formado por una serie de pulsos aleatorios, lo que motiva la generación de un código pseudo-aleatorio artificial por los receptores GPS como patrón de fluctuaciones. En cada instante un satélite transmite una señal con el mismo patrón que la serie pseudo-aleatoria generada por el receptor. En base a esta sincronización, el receptor calcula la distancia realizando un desplazamiento temporal de su código pseudo-aleatorio hasta lograr la coincidencia con el código recibido; este desplazamiento corresponde al tiempo de vuelo de la señal. Este proceso se realiza de forma automática, continua e instantánea en cada receptor.

Utilizar códigos pseudo-aleatorios permite el control de acceso al sistema de satélites, de forma que en situaciones conflictivas se podría cambiar el código, obligando a todos los satélites a utilizar una banda de frecuencia única sin interferencias pues cada satélite posee un código GPS propio.

Aunque la velocidad de los satélites es elevada (4 Km./s), la posición instantánea de los mismos puede estimarse con un error inferior a varios metros en base a una predicción sobre las posiciones anteriores en un período de 24 a 48 horas. Las estaciones terrestres revisan periódicamente los relojes atómicos de los satélites, dos de cesio y dos de rubidio, enviando las efemérides y las correcciones de los relojes, ya que la precisión de los relojes y la estabilidad de la trayectoria de los satélites son claves en el funcionamiento del sistema GPS.(Pozo-Ruz et al., 2000)

4.8. ACTUADORES

4.8.1.1. Motores DC

Los motores DC son los más usados en la actualidad debido a su facilidad de control. Están formados por dos devanados internos, inductor e inducido, que se alimentan con corriente continua:

El inductor, (devanado de excitación), está situado en el estator y crea un campo magnético de dirección fija, denominado de excitación.

El inducido, situado en el rotor, hace girar al mismo debido a la fuerza de Lorentz que aparece como combinación de la corriente circulante por él y del campo magnético de excitación. Recibe la corriente del exterior a través del colector de delgas, en el que se apoyan unas escobillas de grafito.

Los campos magnéticos del estator y del rotor deben permanecer estáticos entre sí para que se pueda convertir la energía eléctrica en energía mecánica. Esta transformación es máxima cuando ambos campos se encuentran en cuadratura.

El colector de delgas es un conmutador sincronizado con el rotor encargado de que se mantenga el ángulo relativo entre el campo del estator y el creado por las corrientes circulantes por el rotor. De esta forma se consigue transformar automáticamente, en función de la velocidad de la máquina, la corriente continua que alimenta al motor en corriente alterna de frecuencia variable en el inducido. Su funcionamiento se conoce con el nombre de auto pilotado.

Al aumentar la tensión del inducido aumenta la velocidad de la máquina. Si el motor está alimentado a tensión constante, se puede aumentar la velocidad disminuyendo el flujo de excitación. Pero cuanto más débil sea el flujo, menor será el par motor que se puede desarrollar para una intensidad de inducido constante. En el caso de control por inducido, la intensidad del inductor se mantiene constante, mientras que la tensión del inducido se utiliza para controlar la velocidad de giro. En los controlados por excitación se actúa, al contrario.

Se obtiene que la relación entre tensión de control y velocidad de giro (función de transferencia), responde a un sistema de primer orden en los controlados por inducido, mientras que, en el caso de los motores controlados por excitación, esta relación es la de un segundo orden.

Además, en los motores controlados por inducido se produce un efecto estabilizador de la velocidad de giro originado por la realimentación intrínseca que posee a través de la fuerza contra electromotriz.

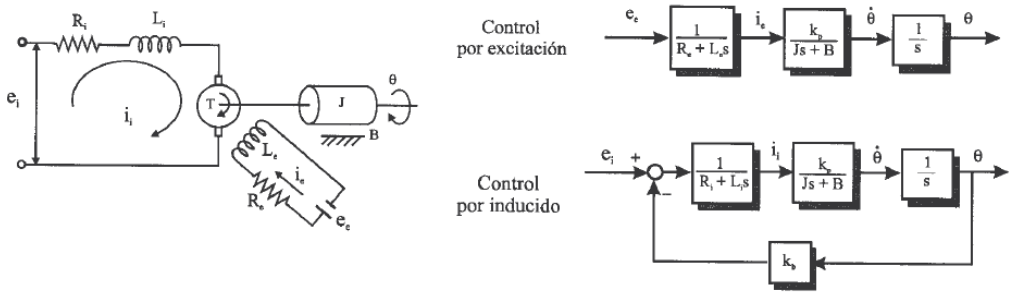

Ilustración 15: Motor DC. Esquema y funciones de transferencia

Para mejorar el comportamiento de este tipo de motores, el campo de excitación se genera mediante imanes permanentes con el fin de evitar fluctuaciones del mimo. Estos imanes son de aleaciones especiales como samario-cobalto. Las velocidades de rotación que se consiguen con estos motores son del orden de 1000 a 3000 r.p.m., con

un comportamiento muy lineal y bajas constantes de tiempo. Las potencias que pueden manejar pueden llegar a los 10 KW.

Los motores DC son controlados mediante referencias de velocidad. Estas normalmente son seguidas mediante un bucle de realimentación de velocidad analógico que se cierra mediante una electrónica específica. Sobre este bucle de velocidad se coloca otro de posición, en el que las referencias son generadas por la unidad de control en base al error entre la posición deseada y la real.

4.8.1.1. Motor Brushless:

El motor de corriente continua presenta el inconveniente del obligado mantenimiento de las escobillas. Por otra parte, no es posible mantener el par con el rotor parado más de unos segundos, debido a los calentamientos que se producen en el colector.

Para evitar estos problemas, se han desarrollado en los últimos años motores sin escobillas o también llamados Brushless. Los imanes de excitación se sitúan en el rotor y el devanado de inducido en el estator, con lo que es posible convertir la corriente mediante interruptores estáticos, que reciben la señal de conmutación a través de un detector de posición del rotor.

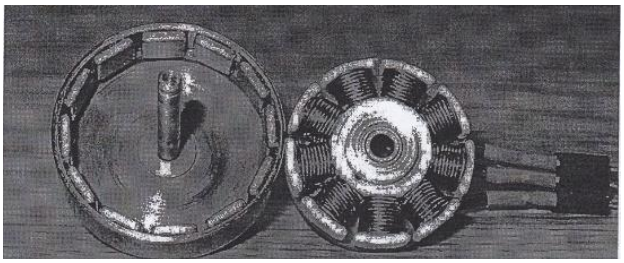

Ilustración 16: Motor Brushless

4.8.2. Motor paso a paso:

Las aplicaciones de los motores paso a paso están limitadas a controles de posición simples, debido a que los pares para los que estaban disponibles eran muy pequeños y los pasos entre posiciones consecutivas eran grandes.

Existen tres tipos de motores paso a paso:

De imanes permanentes.

De reluctancia variable.

Híbridos.

En los imanes permanentes, el rotor, que posee una polarización magnética constante, gira para orientar sus polos de acuerdo al campo magnético creado por las fases del estator.

En los motores de reluctancia variable, el rotor está formado por un material ferro-magnético que tiende a orientarse de modo que facilite el camino de las líneas de fuerza del campo magnético generado por las bobinas de estator. Los motores híbridos combinan el modo de funcionamiento de los dos tipos anteriores.

En los motores paso a paso la señal de control son trenes de pulsos que van actuando rotativamente sobre una serie de electroimanes dispuestos en el estator. Por cada pulso recibido, el rotor del motor gira un determinado número discreto de grados.

Para conseguir el giro del rotor en un determinado número de grados, las bobinas del estator deben ser excitadas secuencialmente a una frecuencia que determina la velocidad de giro. Las inercias propias del arranque y parada (aumentadas por las fuerzas magnéticas en equilibrio que se dan cuando está parado), impiden que el rotor alcance la velocidad nominal instantáneamente, por lo que ésta, y tanto la frecuencia de los pulsos que la fija, debe ser aumentada progresivamente.

Para simplificar el control de estos motores existen circuitos especializados que a partir de tres señales (tren de pulsos, sentido de giro e inhibición) generan, a través de una etapa lógica, las secuencias de pulsos que un circuito de conmutación distribuye a cada fase.

Su principal ventaja con respecto a los motores tradicionales es su capacidad para asegurar un posicionamiento simple y exacto. Pueden girar además de forma continua, con velocidad variable, como motores síncronos, ser sincronizados entre sí, obedecer a secuencias complejas de funcionamiento, etc. Se trata al mismo tiempo de motores muy ligeros, fiables y fáciles de controlar, pues el ser cada estado de excitación del estator estable, el control se realiza en bucle abierto, sin la necesidad de sensores de realimentación.

Entre los inconvenientes se puede citar que su funcionamiento a bajas velocidades no es suave, y que existe el peligro de pérdida de una posición por trabajar en bucle abierto. Tienden a sobrecalentarse trabajando a velocidades elevadas y presentan un límite en el tamaño que pueden alcanzar.

Su potencia nominal es baja y su precisión (mínimo ángulo girado) llega típicamente hasta (1, 8º.), también son muy utilizados en dispositivos periféricos del robot, como mesad de coordenadas.

Es común encontrar en múltiples sistemas el uso de motores paso a paso y motores DC; sin embargo, debido a que cada uno presenta características distintas, la selección depende del sistema a desarrollar y de esta forma se adapte a sus requerimientos. (Carmelo José Borque Horna, 2014)

Comparando los diversos tipos de motores de corriente continua, se observa que primer lugar los motores de corriente continua con escobillas tienen un menor par y las escobillas suponen un peso añadido, por otro lado, los motores paso a paso tienen una buena relación potencia/peso, pero no tanto la relación velocidad/peso, ya que tienen mucha precisión de giro, pero para la aplicación buscada prima la velocidad.

La mayor relación potencia/peso y velocidad/peso para motores de corriente continua se encuentra en los motores sin escobillas, brushless, por lo que es el tipo de motores más idóneo para el proyecto a realizar.

4.9. BATERÍAS

Una batería es un elemento eléctrico capaz de transformar la energía química de las reacciones de sus componentes en energía eléctrica y viceversa (proceso electroquímico), en este caso pudiéndola usar para mover motores o producir movimientos.

Las baterías poseen diversas características que hacen declinarse por un tipo u otro según su uso:

4.9.1. La tensión nominal:

Pilas alcalinas y demás: 1.5V nominales por elemento.

Baterías de níquel cadmio (Ni-Cd): 1.2V. Descarga 1.1V y carga 1.4V nominales por elemento.

Baterías níquel metal hidruro (Ni-MH): 1.2V. Descarga 1.1V y carga 1.4V nominales por elemento.

Baterías de polímeros de litio (Li-Po): 3.7V. Descarga 3.2V y carga 4.2V nominales por elemento.

Baterías de Litio Hierro (LiFe-Po): 3.2V. Descarga 3V y carga 3.6V nominales por elemento.

4.9.2. Capacidad de la batería:

Está directamente relacionada con las horas que va a durar la batería antes de que se tenga que volver a cargar.

La capacidad de una batería se expresa en mAh (una batería de 1000mAh, podrá proporcionar una intensidad de 1000mA durante una hora antes de agotarse).

Por tanto, queda claro que la duración de una batería depende de dos cosas:

La capacidad de la batería (expresada en mAh).

El consumo del circuito que alimenta la batería.

Siendo la expresión matemática que lo calcula:

$$Duración\ de\ la\ batería = \frac{Capacidad\ de\ la\ batería\ (mAh)}{Consumo\ del\ circuito\ (mA)}$$

4.9.3. Tasa de descarga

Existe un límite máximo de corriente C, también llamado tasa de descarga que se puede entregar sin sufrir daños.

No todos los tipos de baterías admiten valores altos de C. Las baterías de níquel cadmio únicamente admiten valores de 1C. Sin embargo, existen baterías de polímeros de litio con valores muy altos de C hasta 50C

4.9.4. Peso:

La relación entre tamaño, peso e intensidad influye en los Amperios/hora.

4.9.5. Tipos de baterías:

4.9.5.1. Baterías de Níquel-Cadmio (Ni-Cd)

Una batería recargable de NiCd está formada por una placa positiva de hidróxido de níquel y una placa negativa de hidróxido de cadmio. Ambas placas están separadas por un electrolito, compuesto por una solución acuosa de potasio cáustico, contenida dentro de un tejido poroso.

Ilustración 17: Batería Ni-Cd

4.9.5.2. Baterías de Ni/MH

Las baterías de Ni/MH tienen una mayor densidad de carga (capacidad/peso superior, aproximadamente 40%-70% más capacidad), no contienen cadmio (tóxico) y aparentemente no tienen efectos de pérdida de capacidad por mal uso o de formación de dendritas (que se forman en las baterías de Ni-Cd al producirse la inversión de la polaridad de la celda).

Este tipo de baterías son más respetuosas con el medio ambiente además tienen una resistencia interna superior que limita su uso en aplicaciones de alta potencia.

Las baterías de Ni/MH no admiten una carga tan rápida como las de Ni-Cd, bajo riesgo de deteriorarlas. Son sensibles al calor dado que con un sobrecalentamiento puede producir gases internos y sobrepresiones dejando pasar escapes de electrolito y pérdidas de estanqueidad, reduciendo la vida útil de las celdas.

También es más difícil de detectar el estado de carga total en las baterías de Ni/MH, por lo que se recomienda el uso de cargadores que especifiquen su aptitud para cargar baterías de Ni/MH, evitando así sobrecalentamientos indeseados.

En estas baterías de Ni-Cd la cantidad de ciclos de carga y descarga oscila entre los 1.000 y 1.500, contra 500 en las de Ni/MH.

Ilustración 18: Batería Ni/MH

4.9.5.3. Baterías de Ión-Litio(Li-Ion)

Las baterías Li-Ion poseen una elevada densidad de energía. Por esta razón tienen menor peso en relación a baterías de otro tipo de la misma capacidad. Se presentan en placas rectangulares, de poco espesor, de menos de 0,5 cm, los que las hace especialmente interesantes para integrarlas en dispositivos portátiles con poco espacio.

Presentan un alto voltaje por celda (cada unidad proporciona 3,6 voltios), carecen de efecto memoria. Su descarga es lineal, es decir, que durante toda la descarga el voltaje de la batería apenas varía, lo que evita la necesidad de circuitos reguladores. (Se debe tener en cuenta que esto puede ser una desventaja en algunos casos, ya que hace difícil averiguar el estado de carga de la batería).

Tienen una baja tasa de autodescarga. Cuando se guarda una batería, ésta se descarga progresivamente, aunque no se use. En el caso de las baterías de Ni/Mh, esta autodescarga puede ser de un 20% mensual. En el caso de Li-Ion es de sólo un 6% (±0.01% diario).(Eduardo J. Carletti, 2016)

Ilustración 19: Batería Ión-Litio

4.10. MODELO MATEMÁTICO

El vuelo de un cuadricóptero se basa en la sustentación producida por el impulso del aire a través de sus hélices y en las maniobras logradas mediante el cambio de velocidad de sus rotores. Se pueden ver los cuadricópteros como máquinas voladoras con 6 grados de libertad, ya que se pueden desplazar y rotar sobre los tres ejes del espacio tridimensional. Aunque esto sea así, en un instante de tiempo dado, sólo se le puede indicar al cuadricóptero cuatro movimientos diferentes.

Para conocer su orientación espacial se necesitan tres valores, los ángulos de Euler (o ángulos de vuelo). Estos ángulos son la diferencia de orientación que hay entre el sistema de referencia terrestre (eje X apuntando al Norte, eje Y al Este y eje Z hacia abajo), y el sistema de referencia de vuelo (eje X apuntando a la cabeza de la aeronave,

eje Y a la derecha), y eje Z, perpendicular a ambos, apuntando hacia la parte de debajo de la aeronave).

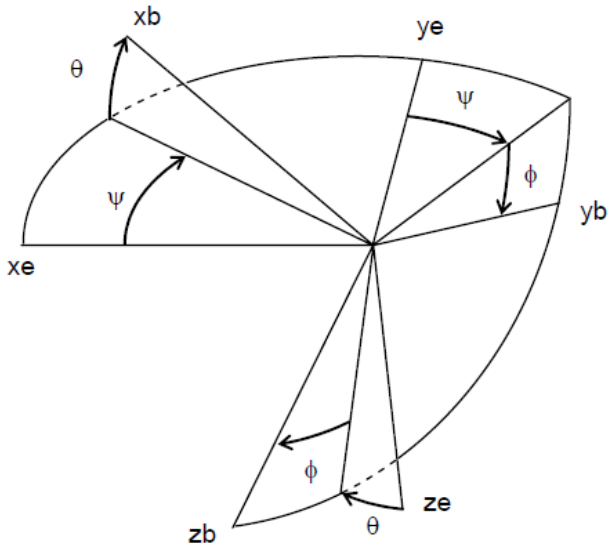

Ilustración 20: Ángulos de Euler

Se supone una situación inicial en la que los dos sistemas de referencia están alineados. El ángulo Yaw, ψ es el ángulo girado sobre el eje Z (de ambos sistemas pues están alineados), logrando girar los ejes X e Y del sistema de referencia de vuelo respecto al de tierra. De forma que se obtienen los ejes X_{v1} e Y_{v1}.

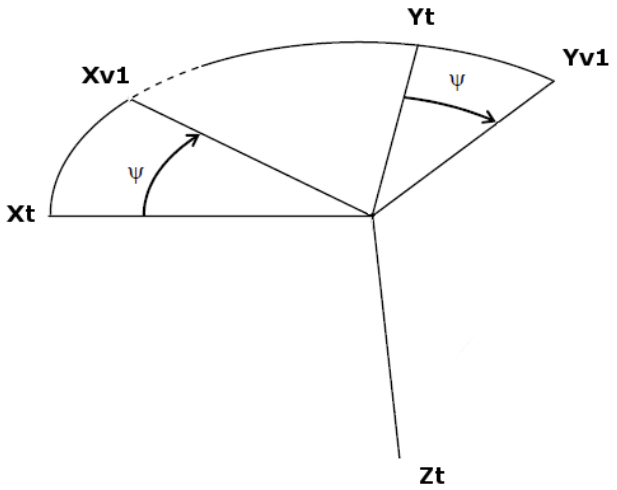

Ilustración 21: Giro en ángulo Yaw

A continuación, se procede a girar sobre el eje Y_{v1}, dando como resultado un determinado ángulo pitch (θ) y logrando girar los ejes X y Z del vuelo, dando como resultado los ejes X_{v2} y z_{v2}.

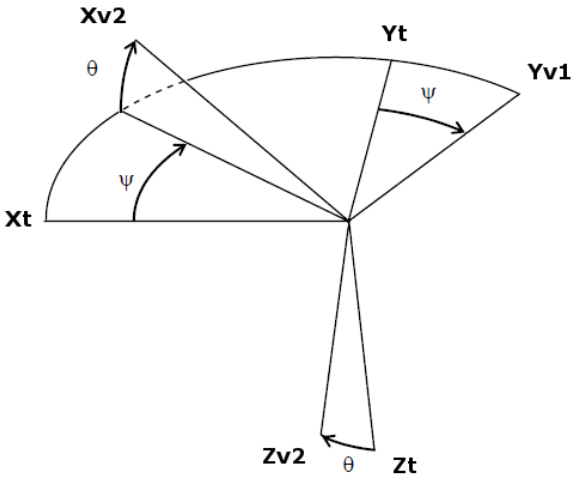

Ilustración 22: Giro en ángulo Pitch

Finalmente, se gira alrededor del eje X_{v2} dando como resultado un determinado ángulo Roll φ, y los ejes Y_{v3} y z_{v3}.

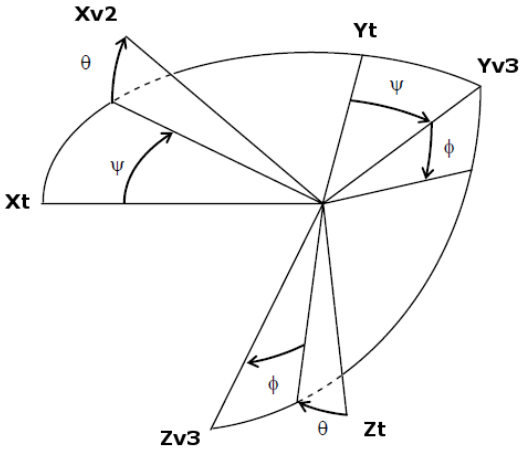

Ilustración 23: Giro en ángulo Roll

Las cuatro maniobras básicas de un cuadricóptero son las siguientes:

Desplazamiento vertical: Como su nombre indica, consiste en la traslación sobre el eje Z del espacio tridimensional (el eje vertical). Se logra incrementando o disminuyendo la velocidad de todos los rotores a la vez, siempre y cuando mantengamos la misma velocidad de rotación en los cuatro rotores. Para elevar el cuadricóptero se requiere incrementar la rotación, y para descenderlo, disminuirla.

Alabeo: Esta maniobra consiste en la rotación sobre el eje longitudinal de la aeronave (eje que va de la parte delantera a la parte trasera del cuadricóptero). En nuestro caso (configuración en +) se logra aplicando un determinado incremento en la velocidad del rotor contrario al lado hacia el que se quiere girar, y disminuyendo el mismo nivel de velocidad en el rotor contrario (el rotor del lado hacia el que queremos girar).

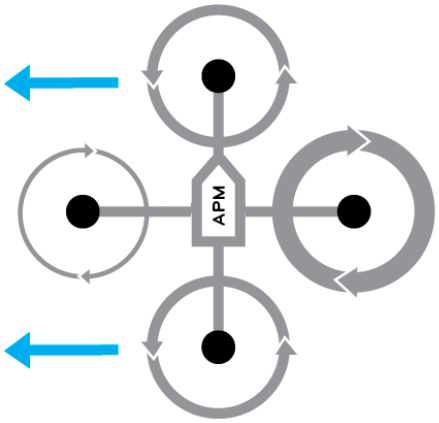

Ilustración 24: Desplazamiento lateral

Cabeceo: Esta maniobra consiste en la rotación sobre el eje transversal de la aeronave, aunque en el caso de un cuadricóptero, al ser simétrico, sólo se distingue del eje longitudinal por lo que consideremos como parte delantera del aparato, o elevar o bajar la cabeza (parte delantera) del cuadricóptero.

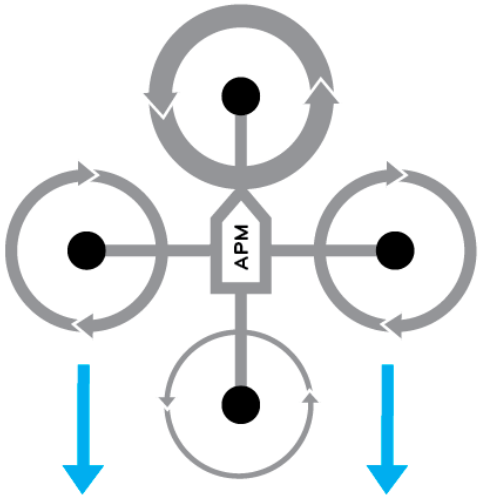

Ilustración 25: Desplazamiento longitudinal

Guiñada: Este movimiento consiste en rotar la aeronave sobre el eje vertical, haciéndola girar sobre sí misma a izquierda o derecha. Mientras giran a la misma velocidad, el efecto torque (o momento de fuerza) a derechas creado sobre el eje por los motores a izquierdas, es contrarrestado por el torque a izquierdas creado sobre el eje por los motores a derechas, logrando un momento de fuerza nulo sobre el conjunto del cuadricóptero. Por eso, para girar a la derecha, se debe incrementar la velocidad de los rotores que giran a la izquierda (ya que los ejes, y con ellos el conjunto, tienden a girar al lado contrario) y disminuir en la misma medida los rotores que giran a la derecha y viceversa para girar a la izquierda.

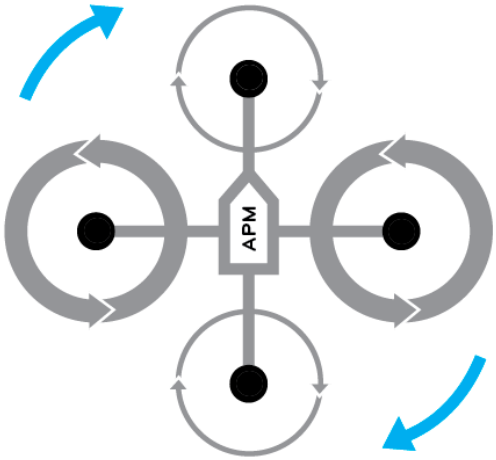

Ilustración 26: Guiñada

Estos son los giros y el desplazamiento que se puede indicar al cuadricóptero que haga en un determinado instante de tiempo, pero ¿cómo se hace para desplazar el drone hacia adelante, atrás o hacía los lados? Se tiene que mantener inclinado el aparato durante un espacio de tiempo para lograrlo. Para el desplazamiento sobre el eje longitudinal (adelante/atrás), se debe mantener un cabeceo en el sentido en el que se quiera desplazar (cabecear hacía abajo para avanzar, hacía arriba para retroceder), y volver a una posición horizontal cuando se desee detener el desplazamiento. Lo mismo ocurre con el desplazamiento sobre el eje transversal (izquierda/derecha), aunque en este caso, lo que se debe mantener es un alabeo a izquierdas o a derechas, dependiendo del sentido en el que queramos desplazarnos. Con todas las estas maniobras, se puede desplazar el cuadricóptero con total libertad por el aire.

Para calcular el Pitch y el Roll inicial, se tiene en cuenta que el cuadricóptero empieza alineado con el sistema de referencia global. Primero es girado un determinado

ángulo Yaw (ψ), luego un ángulo Pitch(θ) y luego un ángulo Roll(φ). Una vez hecho esto se da la siguiente situación:

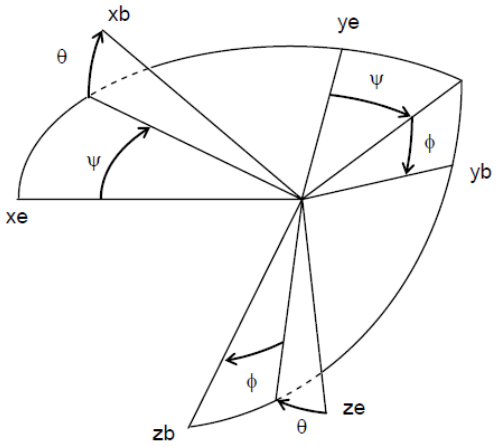

Ilustración 27: Sistemas de referencia siendo e la tierra y b el cuerpo del dron

El acelerómetro proporciona los componentes del vector de gravedad en el sistema de referencia del cuadricóptero, por lo que se puede comprobar que sen(180°+θ) es la proyección de la gravedad sobre el eje X, y cos(θ) la proyección sobre el plano YZ. Conociendo estos dos valores, se puede hallar el ángulo θ gracias al uso del arctan, puesto que ya se conoce el valor de tan(θ) gracias al seno y al coseno. Por tanto, se calcula el ángulo Pitch de la siguiente forma:

$$\theta = \arctan\left(\frac{sen(-\theta)}{\cos(\theta)}\right) = \arctan(\frac{acelX}{|0, acelY, acelZ|})$$

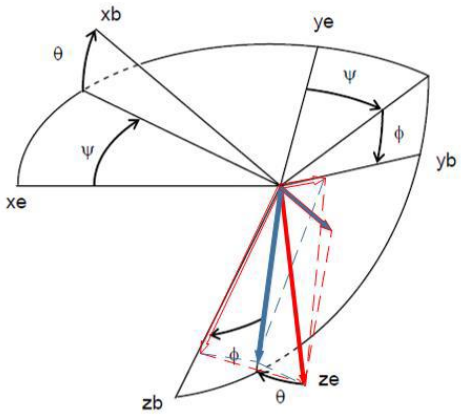

Ilustración 28: Proyecciones para el cálculo de Pitch

Para el cálculo del Roll se sigue un proceso similar, pero en este caso se debe tener en cuenta que el giro del Roll se ha hecho sobre un plano YZ desplazado del plano vertical por la inclinación causada por Pitch. Por tanto, no se puede usar directamente

las proyecciones del vector gravedad pues ninguna es del ángulo φ que se quiere hallar. De forma que, para contrarrestar la inclinación de Pitch, se usa la proyección del vector gravedad sobre el plano YZ (en adelante, gravedadYZ, cuyo módulo es cos(θ)) como vector gravedad, y podemos ver que el componente Y del vector gravedad es cos(θ)*sen(φ), y el componente Z es a su vez cos(θ)·cos(φ). Por lo tanto, se obtiene el ángulo Roll como se hizo antes con el Pitch:

$$\phi = \arctan\left(\frac{\cos(\theta)\, sen(\phi)}{\cos(\theta)\cos(\theta)}\right) = \arctan(\frac{acelY}{acelZ})$$

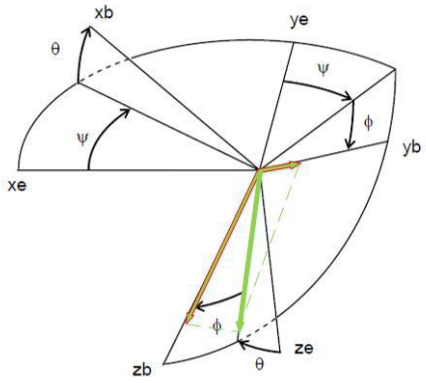

Ilustración 29: Proyecciones para el cálculo de Roll

Para calcular el valor de Yaw inicial, como el giro sobre el eje vertical no afecta a las proyecciones del vector gravedad en el sistema de referencia del cuadricóptero, se necesita la información proporcionada por el Magnetómetro. Sin embargo, aunque el magnetómetro señala al norte, lo hace en tres dimensiones, por lo que los valores que proporciona no sirven directamente para conocer la desviación existente en el plano horizontal. Además, el norte tridimensional, no es un vector sobre el plano, si no que apunta en parte hacía abajo; por lo tanto, aun no habiendo ni Pitch ni Roll, no se podrían utilizar directamente los valores dados por el magnetómetro.

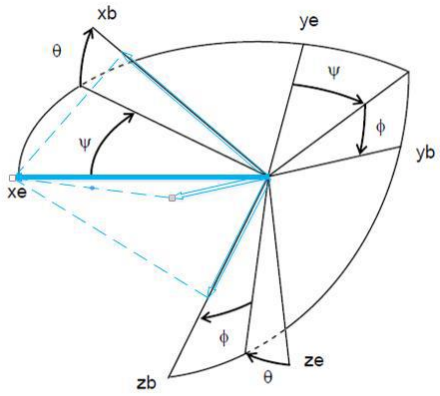

Ilustración 30: Vector Norte en el sistema de referencia del cuadricóptero

Para poder usar los valores del magnetómetro, se debe proyectar el norte tridimensional sobre el plano horizontal rotado por el ángulo Yaw. Es decir, se deben obtener los componentes X e Y del vector norte sobre el plano horizontal logrado al girar el de la tierra por un ángulo ψ. Para ello se proyectan todos los componentes del vector norte sobre el eje XV1:

$$ProyNorteX = magneX \cdot \cos(\theta) + magneY \cdot Sen(\phi) \cdot \mathrm{Sen}(\theta) + \mathrm{magneZ} \cdot \mathrm{Cos}(\phi) \cdot \mathrm{Sen}(\theta)$$

A continuación, se realiza el mismo proceso sobre el eje Yv1:

$$ProyNorteY = magneY \cdot Cos(\phi) - \mathrm{magneX} \cdot \mathrm{Sin}(\phi)$$

Una vez obtenidos los componentes del vector norte sobre el plano girado, se puede obtener el ángulo que hace el vector norte proyectado con el eje Xv1 por medio del uso de la arcotangente. El ángulo Yaw es el negativo de este ángulo:

$$\psi = -\arctan\left(\frac{ProyNorteY}{ProyNorteX}\right)$$

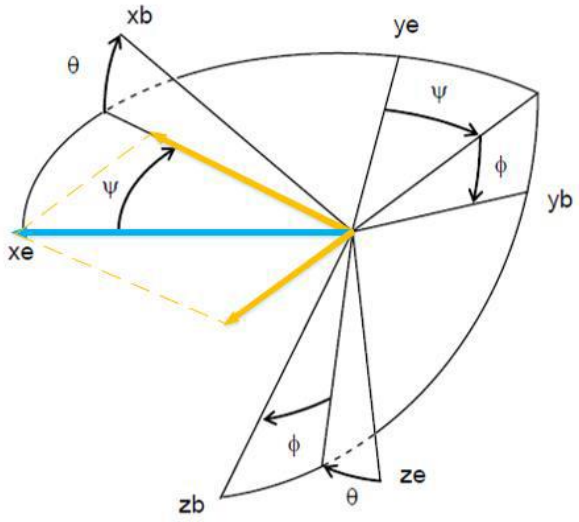

Ilustración 31: Proyecciones para el cálculo de Yaw

Una vez se tiene la posición inicial, se puede calcular la orientación actual mediante la matriz de cosenos directores (DCM).

El algoritmo de la matriz DCM tiene como finalidad acumular todos los giros realizados y dar la orientación actual mediante ángulos de Euler.

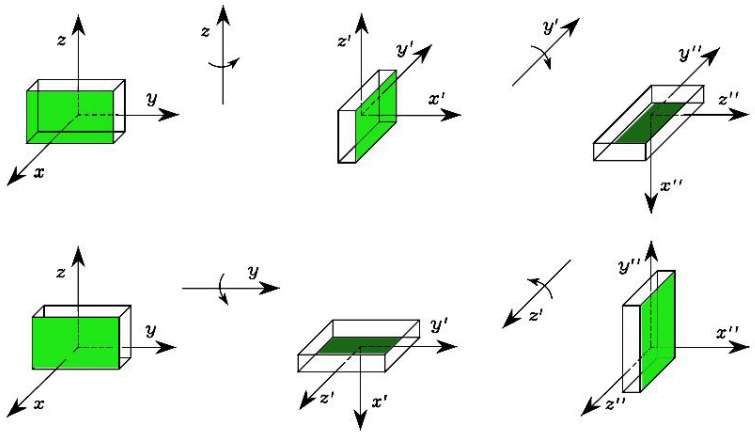

Ilustración 32: Rotaciones no conmutativas

Las matrices de rotación son matrices 3x3 que al ser multiplicadas por un vector tridimensional sirven para girarlo en el espacio. Las básicas para el giro en los ejes X, Y y Z son las siguientes:

$$Gx = \begin{pmatrix} 1 & 0 & 0 \\ 0 & \cos(\phi) & -\text{sen}(\phi) \\ 0 & \text{sen}(\phi) & \cos(\phi) \end{pmatrix}$$

$$Gy = \begin{pmatrix} \cos(\theta) & 0 & \text{sen}(\theta) \\ 0 & 1 & 0 \\ -\text{sen}(\theta) & 0 & \cos(\theta) \end{pmatrix}$$

$$Gx = \begin{pmatrix} \cos(\psi) & -\text{sen}(\psi) & 0 \\ \text{sen}(\psi) & \cos(\psi) & 0 \\ 0 & 0 & 1 \end{pmatrix}$$

Si se gira el sistema de referencia primero en Z, luego en Y y luego en X, se obtiene la siguiente matriz:

$$R = \begin{pmatrix} \cos\theta\cos(\psi) & \text{sen}(\phi)\text{sen}\,\theta\cos\psi - \cos(\phi)\,\text{sen}(\psi) & \cos(\phi)\,\text{sen}\,\theta\cos(\psi) + \text{sen}(\phi)\text{sen}(\psi) \\ \cos\theta\,\text{sen}(\psi) & \text{sen}(\phi)\text{sen}\,\theta\,\text{sen}\,\psi + \cos(\phi)\cos(\psi) & \cos(\phi)\text{sen}\,\theta\,\text{sen}\,\psi - \text{sen}(\phi)\cos(\psi) \\ -\text{sen}\,(\theta) & \text{sen}(\phi)\cos(\theta) & \cos(\phi)\cos(\theta) \end{pmatrix}$$

Esa es la matriz de cosenos directores, y aunque se multipliquen más matrices de giro por ella, siempre mantiene esta estructura, pudiendo obtener los ángulos de vuelo (en cualquier momento) de la siguiente manera:

$$\psi = \arctan\left(\frac{\cos\theta\,\text{sen}\,\psi}{\cos\theta\cos(\psi)}\right)$$

$$\theta = -\arcsin(-\text{sen}\,\theta)$$

$$\phi = \arctan\left(\frac{\text{sen}(\phi)\cos(\theta)}{\cos(\phi)\cos(\theta)}\right)$$

Esta ecuación sirve para pasar vectores del sistema de referencia de vuelo al de tierra y viceversa; siendo las columnas de la matriz los ejes X, Y y Z de vuelo en el sistema de referencia de tierra, y las filas los ejes X, Y y Z de tierra en el sistema de referencia de vuelo. Por tanto, para representar un vector del sistema de referencia de tierra en el sistema de vuelo, se debe multiplicar por la DCM; y en caso de querer pasar un vector del sistema de vuelo al de tierra, se debe multiplicar por la inversa de la DCM.(Omar Luque Rodríguez, 2014)

4.11. LEGISLACIÓN

4.11.1. Marco regulatorio

La primera norma reguladora del uso de drones en España se recoge en el Real Decreto-ley 8/2014, de 4 de julio.

Sin embargo, dicho Real Decreto-ley dio lugar a la tramitación parlamentaria de un proyecto de ley que ha acabado siendo la Ley 18/2014, de 15 de octubre, de aprobación de medidas urgentes para el crecimiento, la competitividad y la eficiencia ("Ley 18/2014").

La Ley 18/2014 incluye en su art. 50 determinadas disposiciones respecto de las aeronaves civiles pilotadas por control remoto ("UAVs", en sus siglas en inglés).

Asimismo, la Ley 18/2014 modifica la Ley 48/1960, de 21 de julio, de Navegación Aérea para incluir en la definición de aeronaves las UAVs.

4.11.2. Regulación de las UAV y operaciones

Las principales cuestiones relativas a las UAVs que se regulan en el art. 50 de la Ley 18/2014 son las siguientes:

4.11.3. Inscripción e identificación:

Las UAVs con masa máxima de despegue superior a 25 kg deberán constar en el Registro de Matrícula de Aeronaves y contar con una placa de identificación de la aeronave y su operador.

4.11.4. Destino:

Las UAVs podrán destinarse a operaciones especializadas (también conocidas como trabajos aéreos), tales como investigación, fumigación, fotografía, vigilancia, patrulla, publicidad, lucha contra incendios o salvamento, así como a trabajos científicos.

4.11.5. Condiciones de operación:

Dependiendo de la masa de despegue y de si la operación está dentro del campo visual del piloto, se establecen determinados límites de distancias y de altura, así como restricciones para su uso en núcleos urbanos y en las proximidades de aeropuertos y aeródromos.

En todo caso, los vuelos deberán realizarse de día y en condiciones meteorológicas visuales.

Las operaciones requieren de una determinada documentación, incluyendo un manual de operaciones, un estudio aeronáutico de seguridad, la superación de vuelos de prueba, programas de mantenimiento, medidas de protección frente a interferencias ilícitas y medidas de protección de las personas y los bienes.

Estos requisitos se relajan en parte en determinadas condiciones si se trata de vuelos de prueba, de demostración, de investigación, de desarrollo o de I+D.

4.11.6. Acreditación de pilotos:

Los pilotos deben obtener la correspondiente licencia y demostrar conocimientos teóricos, además de cumplir con otra serie de requisitos (edad mínima, según el tipo de UAV y el tipo de operación deberán recabar un certificado básico o un certificado avanzado, certificado médico).

4.11.7. Habilitación para las operaciones:

Dependiendo del tipo de UAV, se precisará un tipo de habilitación distinto:

UAVs con masa de despegue que no exceda de 25 kg: bastará una comunicación previa, junto con una declaración responsable, a presentar con 5 días de antelación al inicio de la operación. La documentación deberá presentarse ante la Agencia Estatal de Seguridad Aérea ("AESA").

UAVs con una masa de despegue superior a 25 kg: se requiere autorización previa. La autorización debe solicitarse a AESA y, en caso de no obtener resolución expresa, se entenderá desestimada por silencio administrativo.

En ambos casos, la vigencia de la habilitación será por tiempo indefinido, salvo modificación de las características de la operación.

4.11.8. Vuelos en caso de situaciones de riesgo, catástrofes o calamidades públicas:

Se permite la operación de UAVs sin habilitación siempre que se cumplan las condiciones de operación, bajo responsabilidad del operador y cuando así le sea requerido por la autoridad competente.

4.11.9. Otras cuestiones

Al margen de las cuestiones reguladas en la Ley 18/2014, la operación de las UAVs requiere, además, del uso del espectro radioeléctrico, debiendo estar a las disposiciones contenidas en la normativa sectorial de telecomunicaciones. Asimismo, deberán observarse las cuestiones relativas a la normativa de protección de datos personales.

5. DISEÑO MECÁNICO

5.1. CÁLCULOS Y ELECCIÓN DE HÉLICE Y MOTOR

A continuación, se va a proceder a realizar el diseño mecánico del dron. Para ello, se va a hallar el empuje necesario para levantar el peso total de la estructura y, en función de ello, escoger un motor comercial y unas hélices para incorporarlos al sistema.

En primer lugar, se determina el empuje necesario, para ello se multiplica el peso de la estructura por la relación empuje/peso del dron, en este caso la misma es 0,6 ya que realiza un vuelo a escala, siendo 3 Kg la masa que debería levantarse para que no hubiera ningún problema, al haber 4 motores (cuadricóptero) se divide el empuje para 4:

$$empuje = (peso \cdot \left(relación \frac{empuje}{peso}\right))/4 = (3Kg \cdot 0{,}6)/4 = 0{,}45Kg$$

Posteriormente, se determina la relación potencia/empuje, de forma que la velocidad estimada para este tipo de vuelos es de 60 Km/h como máximo:

$$Relación \frac{potencia}{empuje} = 0{,}0023 \cdot velocidad + 0{,}021 = 0{,}0023 \cdot \frac{60Km}{h} + 0{,}021 = 1{,}401$$

Con los resultados obtenidos se halla la potencia:

$$Potencia = Empuje \cdot (Relación\ potencia/empuje) = 0{,}45Kg \cdot 1{,}401 = 0{,}63W$$

Con la velocidad escogida, se escoge un paso, en este caso 3 y una tensión de alimentación que será 12 V, de este modo se halla el Kv del motor:

$$Kv = \frac{Velocidad \cdot 1000}{60 \cdot V \cdot Paso} = \frac{60 \cdot 1000}{60 \cdot 12 \cdot 3} = 27{,}77Kv$$

Por último, se halla la relación diámetro x paso de las hélices:

$$D \cdot P = 17{,}9 \cdot \sqrt{\frac{empuje}{Kv \cdot V}} = 17{,}9 \cdot \sqrt{\frac{0{,}45}{27{,}77 \cdot 12}} = 20{,}8$$

De este modo se ha elegido para el dron los siguientes motores y hélices:

- Motor DYS BE 1806 2300Kv(DYS, 2016)
- Hélices Gemfan 6030 de fibra de carbono, paso 3 y 6”(Gemfan, 2016)

  De tal forma que se genera un empuje de 0,485 Kg cada motor, suficiente para el dron a diseñar.

5.2. DISEÑO EN 3D

Una vez realizados los cálculos necesarios para hallar motor y hélices, se va a realizar un diseño en 3D del dron, para ello se ha utilizado el software Autodesk Inventor.

Se ha utilizado una estructura en forma de aspa, ya que es la más adecuada para tomar imágenes con una cámara y alojar la electrónica en la parte central. El diseño está basado en otros cuadricópteros con cámara del mercado, como son:

- Syma X8C (Syma, 2016)
- XK X251(Perlman, 2016)
- HiSky HMX260(Drone Flyers, 2015)

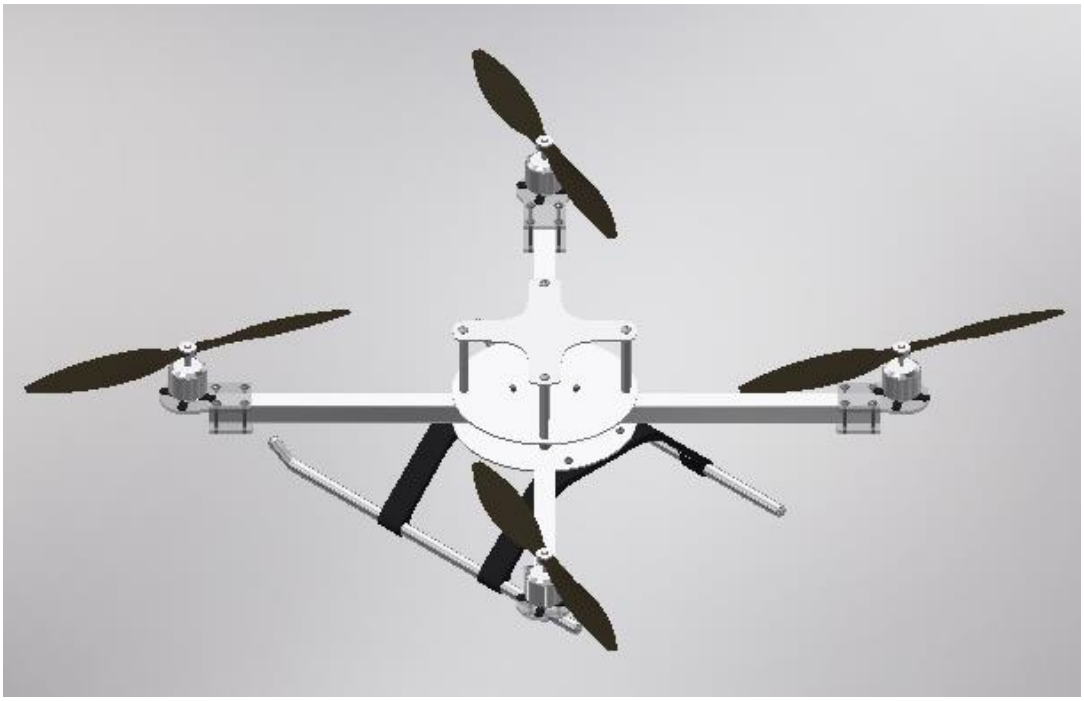

Ilustración 33: Diseño en 3D del dron

La estructura en su mayor parte será de aluminio 6061, ya que este material aporta tanto ligereza como resistencia. Las dimensiones y la disposición de componentes electrónicos y cámara serán las siguientes:

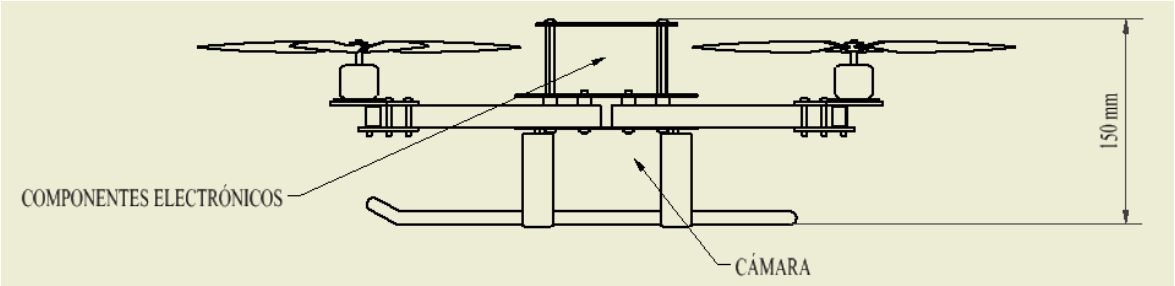

Ilustración 34: Disposición de componentes electrónicos y altura dron

Como se puede observar, la parte electrónica irá alojada en la parte superior del dron, mientras que la cámara, que irá conectada a la misma, se situará en el espacio situado entre los brazos estructurales y el tren de aterrizaje. La altura es de 150 mm, se ha buscado que no sea excesivamente alto para ser más eficiente aerodinámicamente y disminuir su resistencia al aire.

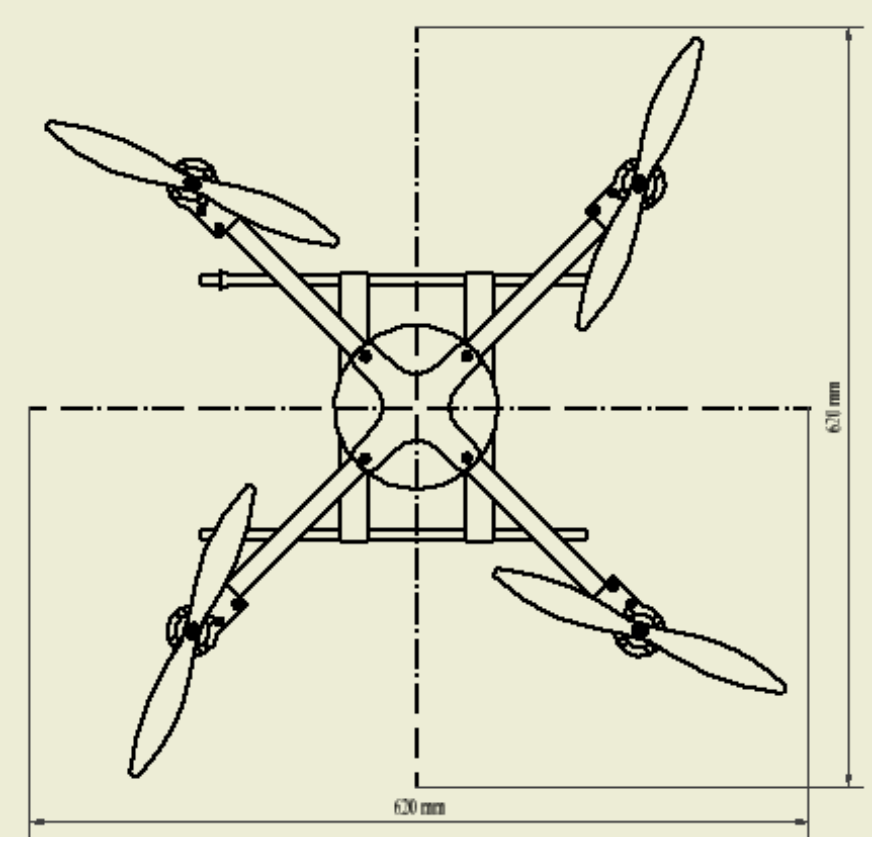

Ilustración 35: Dimensiones ancho y largo dron

Las dimensiones de ancho y alto son de 620 mm, de este modo se intenta, junto con su altura, conseguir un dron lo más estable posible para favorecer las maniobras necesarias una vez se encuentre el mismo en el aire.

De este modo, la estructura del dron consta de las siguientes partes:

5.2.1. Brazos del cuadricóptero

Una de los elementos más importantes en la estructura son los brazos del dron, donde se sitúan a un extremo el soporte para motores, que a su vez van acoplados a las hélices y el otro extremo va roscado a la parte central donde se sitúa la parte electrónica.

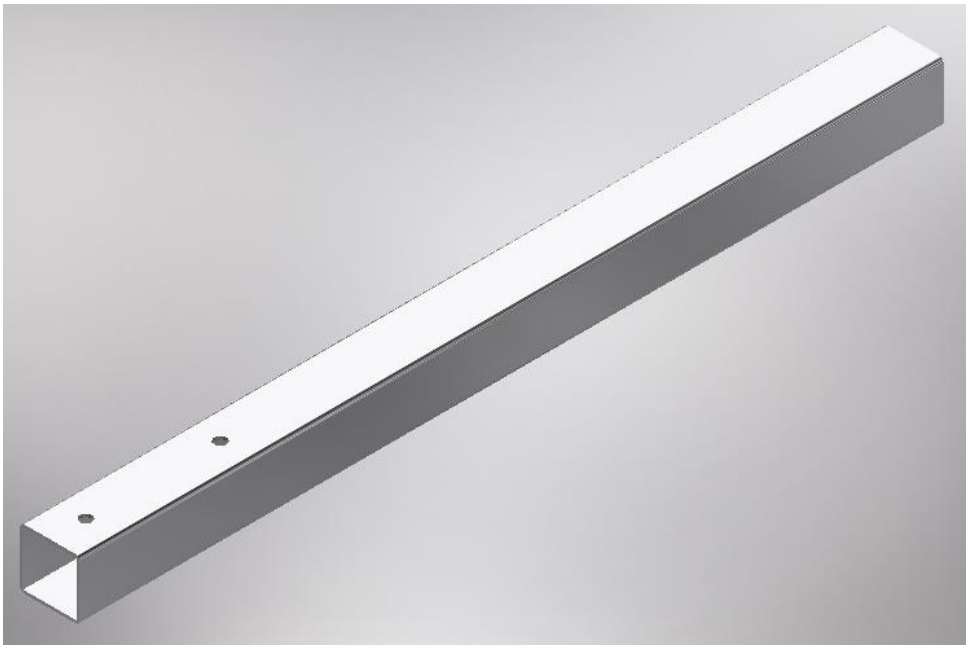

Ilustración 36: Brazo del cuadricóptero

El dron consta de cuatro brazos, siendo perfiles de Aluminio 6061 fabricados por extrusión, cada uno consta de las siguientes dimensiones:

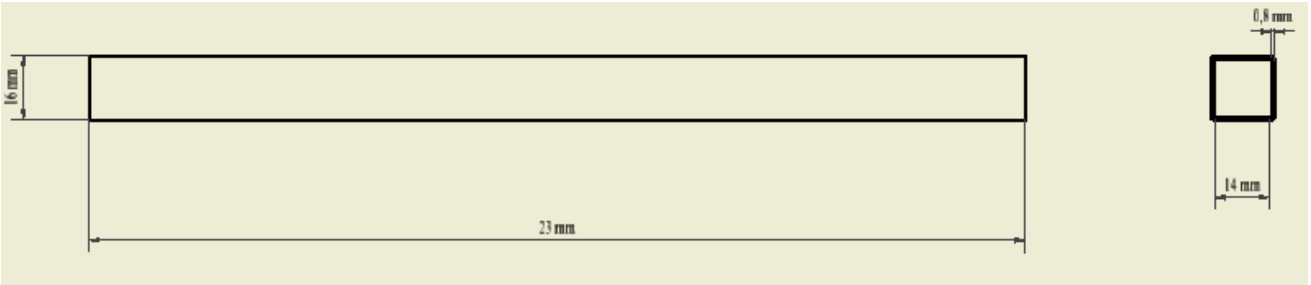

Ilustración 37: Dimensiones brazos cuadricóptero

5.2.2. Base superior

Esta pieza se sitúa en el centro de la estructura, encima de la misma se sitúa la parte electrónica y en ella van atornillados tanto los brazos como las varillas que sujetan la cruceta superior.

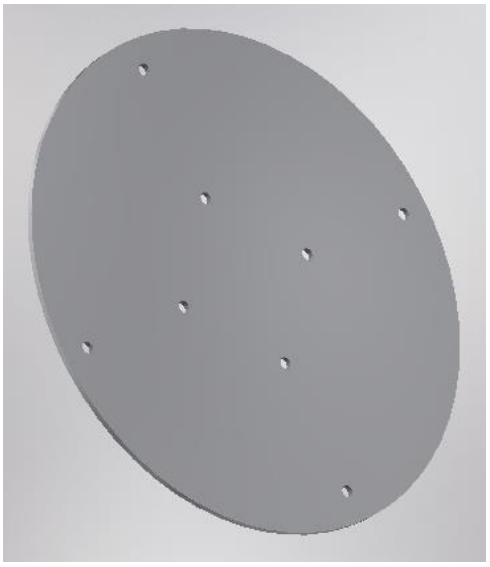

Ilustración 38: Base superior

Al igual que la mayoría de la estructura, su material es Aluminio 6061 y está fabricada mediante corte por chorro de agua. Dispone de las siguientes dimensiones:

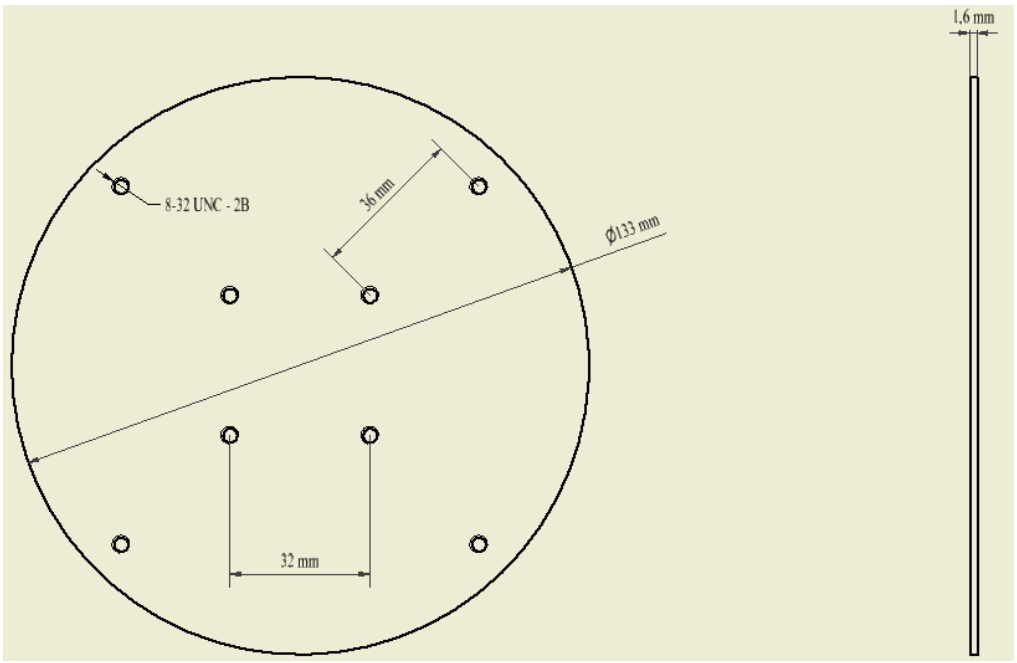

Ilustración 39: Dimensiones base superior

5.2.3. Base inferior

Este componente va atornillado tanto al tren de aterrizaje como a los brazos, actuando como unión de ambos al resto de la estructura.

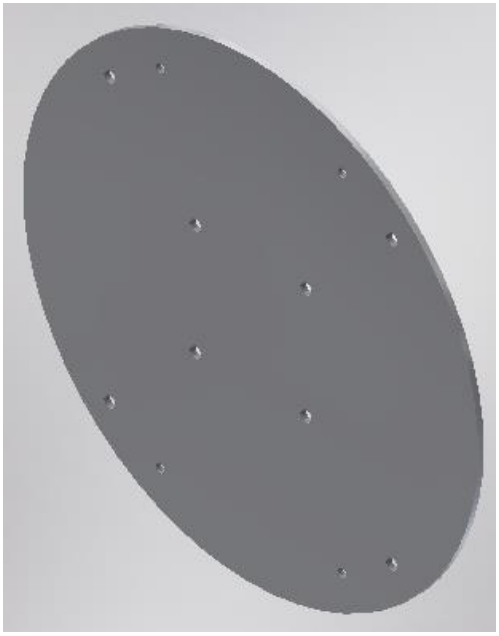

Ilustración 40: Base inferior

Al igual que la base superior, está fabricada de Aluminio 6061 mediante corte por chorro de agua teniendo las siguientes dimensiones:

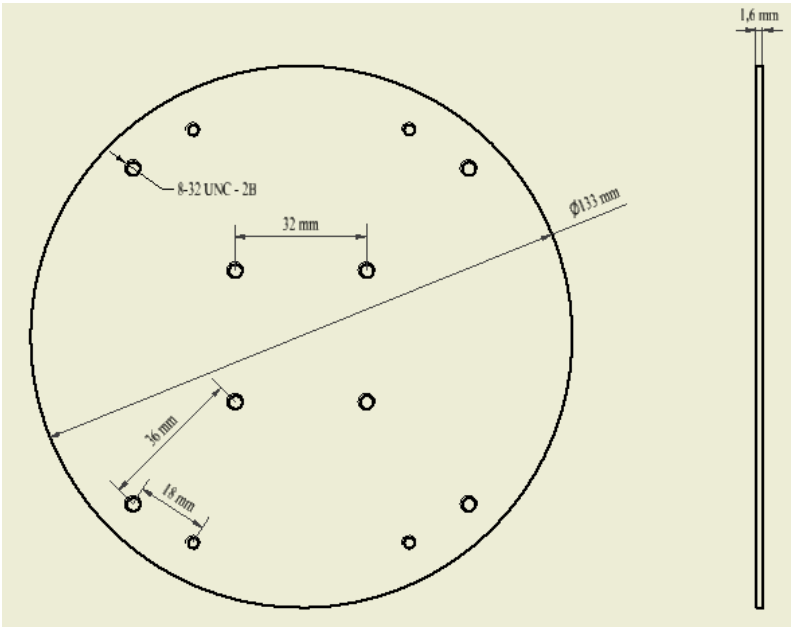

Ilustración 41: Dimensiones base inferior

5.2.4. Soporte de motores

Son las piezas que se sitúan en los extremos de cada brazo del cuadricóptero y sobre las que se sitúan los motores.

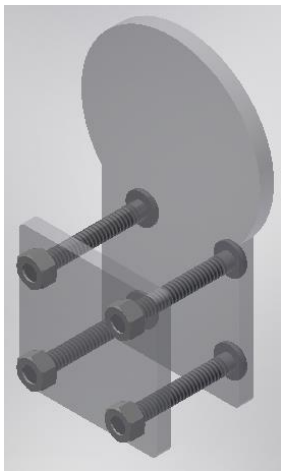

Ilustración 42: Soporte motores

Cada soporte consta de dos piezas de polietileno de alta densidad fabricadas por extrusión, estando atornilladas entre ellas y al brazo del dron. Estos componentes tienen estas dimensiones:

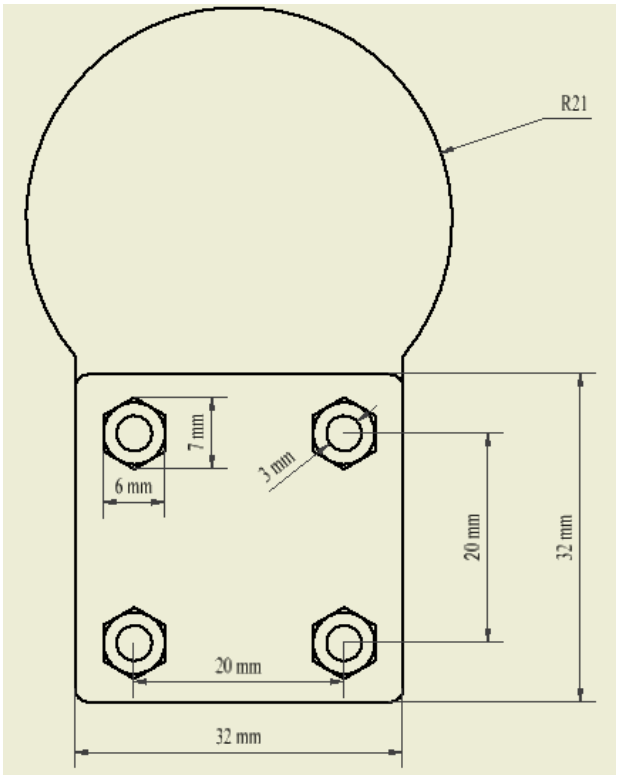

Ilustración 43: Dimensiones alzado soporte motores

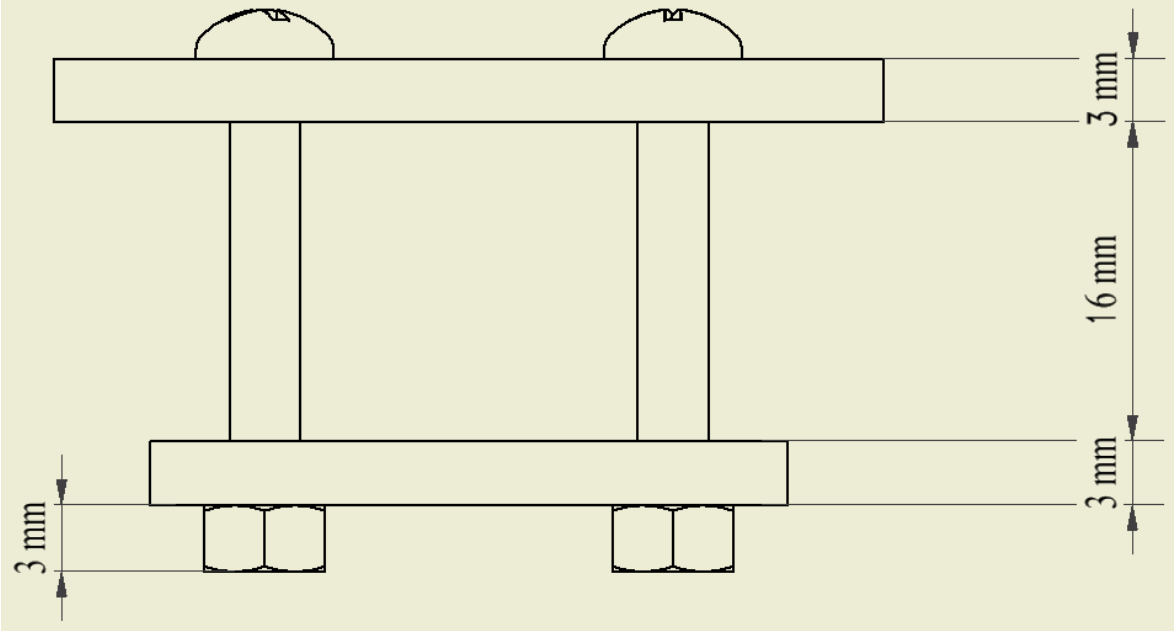

Ilustración 44: Dimensiones planta soporte motores

5.2.5. Tren de aterrizaje

Es la parte inferior de la estructura del cuadricóptero, se encuentra atornillado a la base inferior central de la estructura y está formada por dos piezas.

Ilustración 45: Tren de aterrizaje

De esta forma, tanto el material del tren inferior como de los soportes que lo unen atornillado a la base inferior de la estructura están fabricados a través de un proceso de extrusión, siendo unidos mediante soldadura, ambos son de aluminio 6061 al igual que la mayoría de la estructura. Sus dimensiones son:

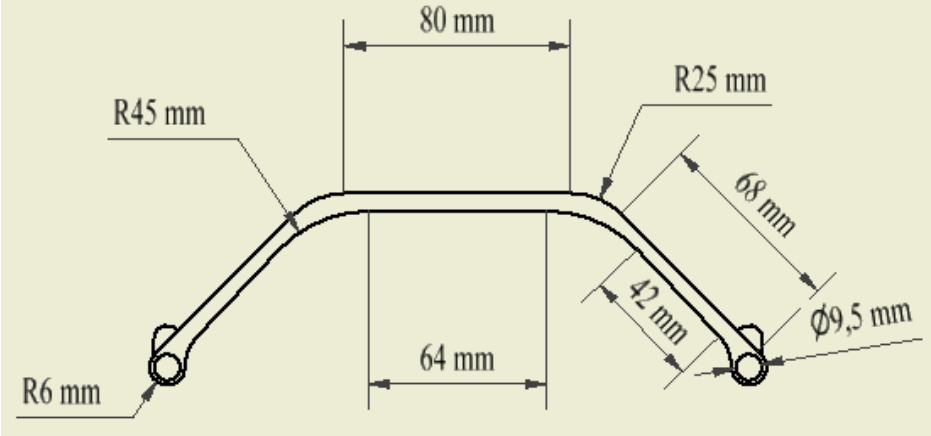

Ilustración 46: Dimensiones alzado tren de aterrizaje

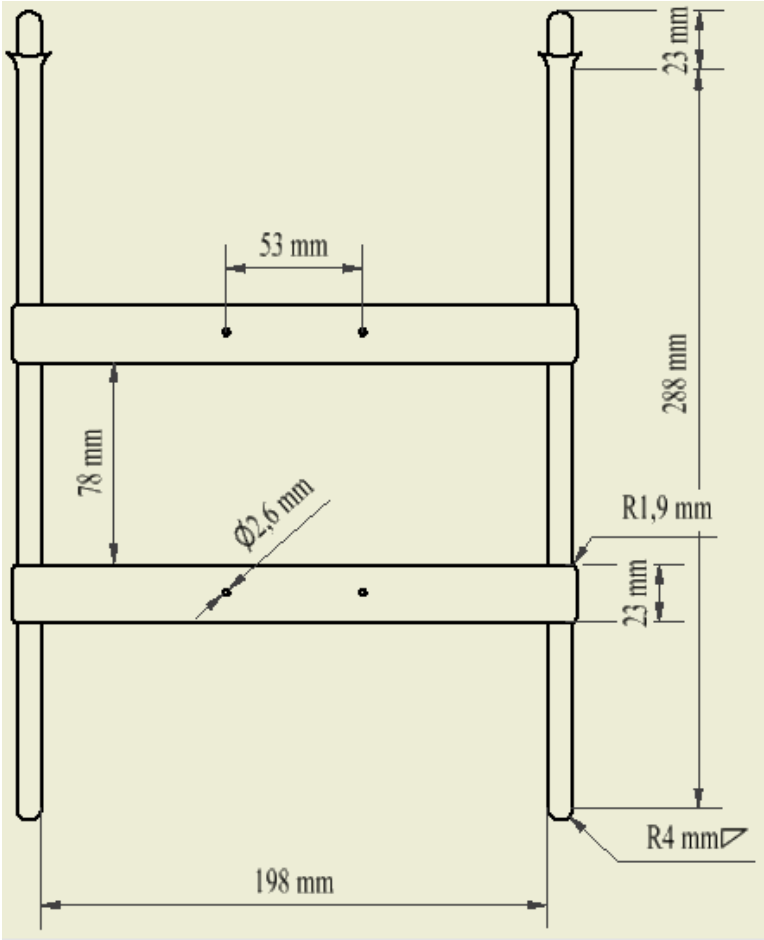

Ilustración 47: Dimensiones planta tren de aterrizaje

5.2.6. Cruceta superior

Esta pieza se sitúa encima de la estructura, atornillada a las varillas roscadas que a su vez van atornilladas a la base superior, sirve como protección de la parte electrónica que se situará debajo.

Ilustración 48: Cruceta superior

Esta pieza está fabricada de aluminio 6061 mediante corte por chorro de agua, a continuación, se observan sus dimensiones:

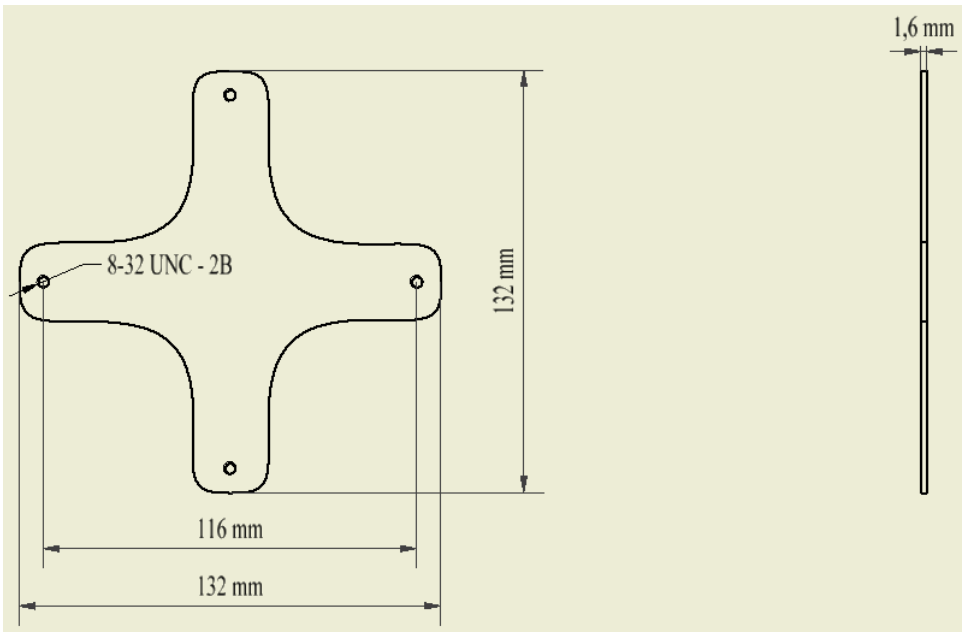

Ilustración 49: Dimensiones cruceta superior

6. DISEÑO ELECTRÓNICO

6.1. SELECCIÓN DE COMPONENTES ELECTRÓNICOS

El siguiente proceso que se va a llevar a cabo en el diseño es el correspondiente a la parte electrónica del cuadricóptero. Para ello en primer lugar se escogen los componentes electrónicos que más se ajusten a las características buscadas, de esta forma se han seleccionado los siguientes:

- Microcontrolador: NodeMCU, kit basado en el módulo ESP8266(Prat Vera, 2016).
- GPS: Neo-6M(Ublox, 2016) junto con una EEPROM 24AA32A1 para lectura de datos(ST, 2009)
- Acelerómetro, giroscopio y magnetómetro: LSM 9DS0(ST, 2013)
- Cámara Wi-Fi Xiaomi YiCam(Xiaomi, 2016)

6.2. DISEÑO DE CIRCUITO ELECTRÓNICO

Una vez realizada la selección de componentes, se procede a realizar el diseño del circuito electrónico del cuadricóptero, teniendo en cuenta las salidas de los pines del kit NodeMCU:

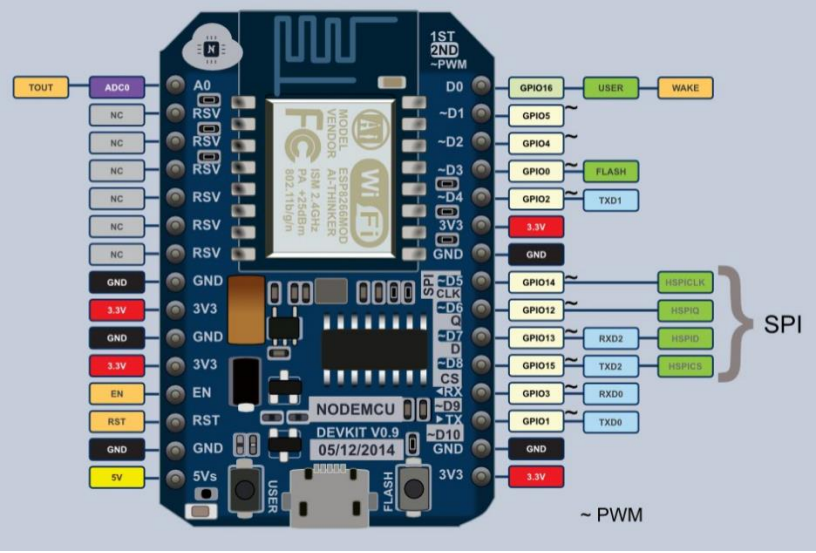

Ilustración 50: Salidas de pines de NodeMCU

En la siguiente tabla se recogen las diferentes formas de inicio de la placa dependiendo de añadir un 1 o 0 lógico a GPIO0, GPIO2 y GPIO13.

	Función		
Puerta	GPIO0	GPIO2	GPIO13
UART Download	0	1	0
Flash Startup	1	1	0
SD-Card Boot	0	0	1

Tabla 1: Configuración de inicio de NodeMCU

Para este caso, el inicio necesitado es Flash Startup, de tal forma que se añade en el circuito la combinación necesaria para el mismo.

Para conectar los drivers de los cuatro motores, se necesitan unos buffer que van a las salidas PWM del microcontrolador, las mismas son:

- IO12: PWM0
- IO13: PWM1
- IO14: PWM2
- IO4:PWM3

Siendo los buffer seleccionados unos Texas SN74LV1T34(Texas Instruments, 2014) y los drivers de motores unos DYS SN36A(DYS, 2016)

La salida PWM13 al ir a masa para insertar un 0 lógico, se conecta también a una entrada de buffer.

Estos requisitos hacen que no se disponga de entradas digitales suficientes para conectar el acelerómetro, necesitando un módulo de expansión de entradas y salidas, para ello se ha seleccionado un Microchip MCP23008(Microchip, 2007).

Para la alimentación del circuito, se han seleccionado los siguientes componentes:

- Cargador de baterías MAX 1926(Maxim, 2002)
- Convertidor 3V3 LP2980(Texas Instruments, 2016)
- Convertidor 5V Tracopower TEN5-1211(TracoPower, 2015)
- Fuente de alimentación Meanwell P5-35-13.5(Meanwell, 2007)
- Baterías Zippy FlightMax 8000mAh(ZIPPY, 2016)

El convertidor 3V3 tiene dos modos para ajustar la salida de tensión del circuito: el modo ajustable y el modo fijo a 3,3V, en el modo ajustable se tiene el siguiente circuito:

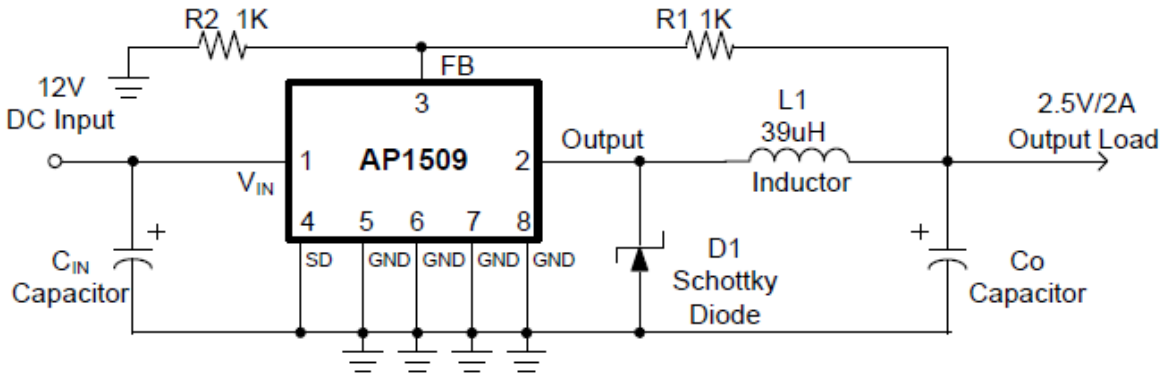

Ilustración 51: Circuito tensión de salida ajustable convertidor 3V3

De forma que mediante la siguiente ecuación se puede modificar la tensión de salida en función de los valores escogidos para las resistencias R1 y R2:

$$V_{Out} = V_{FB} \cdot (1 + \frac{R1}{R2})$$

Como en este caso se busca tener una tensión de salida de 3,3V, que es la obtenida por el modo de circuito fijo, se utiliza este tipo de circuito, eliminando las resistencias R1 y R2:

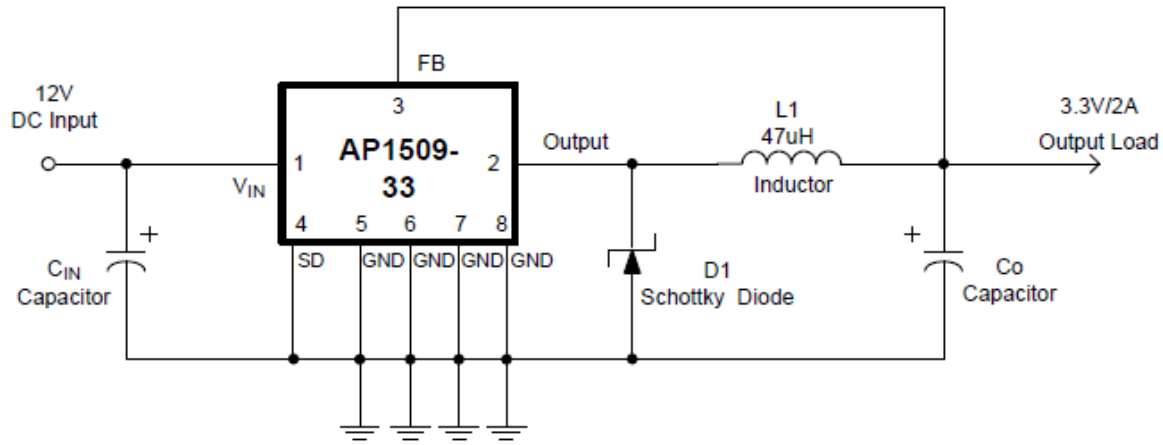

Ilustración 52: Modo de tensión fijada a 3,3V convertidor

El cargador de baterías viene dado por el siguiente circuito, por medio del cual se van a seleccionar diversos componentes para adaptarlo a las características buscadas y haciendo que su funcionamiento sea el correcto:

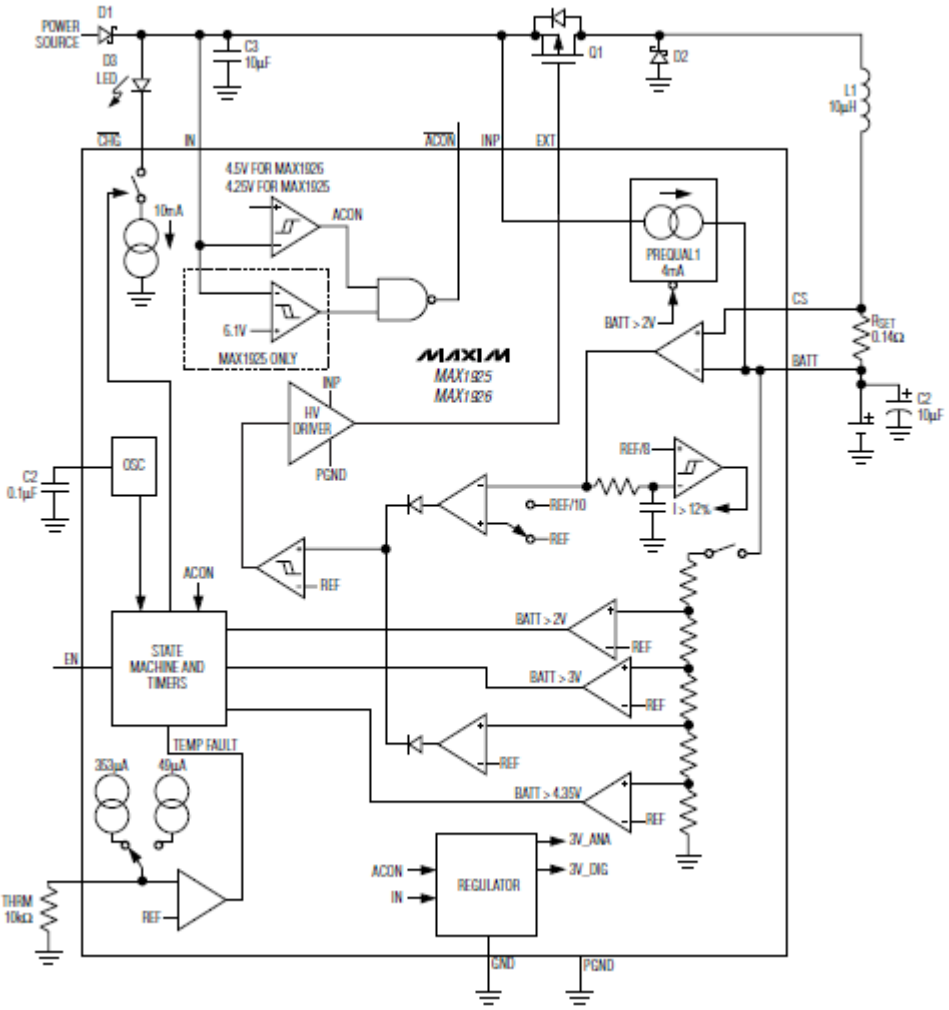

Ilustración 53: Circuito cargador de baterías

En primer lugar, se va a hallar el incremento de corriente de carga, para ello se sabe que la tensión de entrada Vin es 13,5V y la de las baterías Vbatt es 12V, siendo la L seleccionada de 10 uH y el tiempo de retardo (delay) 300 ns se tiene:

$$\Delta I_{Chg} = \frac{(V_{in} - 2 \cdot V_{batt}) \cdot t_{delay}}{2 \cdot L} = \frac{(13{,}5V - 2 \cdot 12V) \cdot 300 \cdot 10^{-9}s}{2 \cdot 10 \cdot 10^{-6}H} = -1{,}575A$$

Al ser negativo el resultado, la corriente de carga ha disminuido 1,575 A.

Ahora se va a comprobar que la inductancia seleccionada es compatible con el circuito a través de la siguiente ecuación:

$$L > \frac{(V_{in} - 2 \cdot V_{bat}) \cdot t_{delay}}{2 \cdot \Delta I_{Chg}}; L > \frac{(13{,}5V - 2 \cdot 12V) \cdot 300 \cdot 10^{-9}s}{2 \cdot (-1{,}575A)}; L > 1 \cdot 10^{-6}H$$

De forma que la inductancia escogida de 10 uH cumple las condiciones.

En el condensador de salida se recomienda uno de 10 uF que es el seleccionado para este caso.

Para el transistor MOSFET se ha elegido uno con baja resistencia drenador-fuente, en este caso 1,2 Ohmios.

Para alargar el tiempo de vuelo del dron, se ha decidido colocar dos baterías en paralelo teniendo 16000 mAh, de forma que se mejora la autonomía sin verse comprometido el peso, siendo el consumo de los motores de 64 A y el de la cámara 750 mA se obtiene:

$$Autonomía = \frac{Capacidad\ batería}{Consumo\ componentes} = \frac{16000\ mAh}{64000mA + 750\ mA} = 0{,}247\ h = 14\ \text{min}\ 49\ s$$

A continuación se halla el tiempo de carga, siendo la corriente de entrada de la fuente de alimentación de 2,3 A:

$$Tiempo\ de\ carga = \frac{Capacidad\ batería}{Corriente\ de\ entrada} = \frac{16000\ mAh}{2600\ mA} = 6{,}15\ h = 6\ h\ 9\ \text{min}\ 13\ s$$

Posteriormente, se procede a realizar el diseño del circuito mediante el software KiCAD, quedando de la siguiente manera:

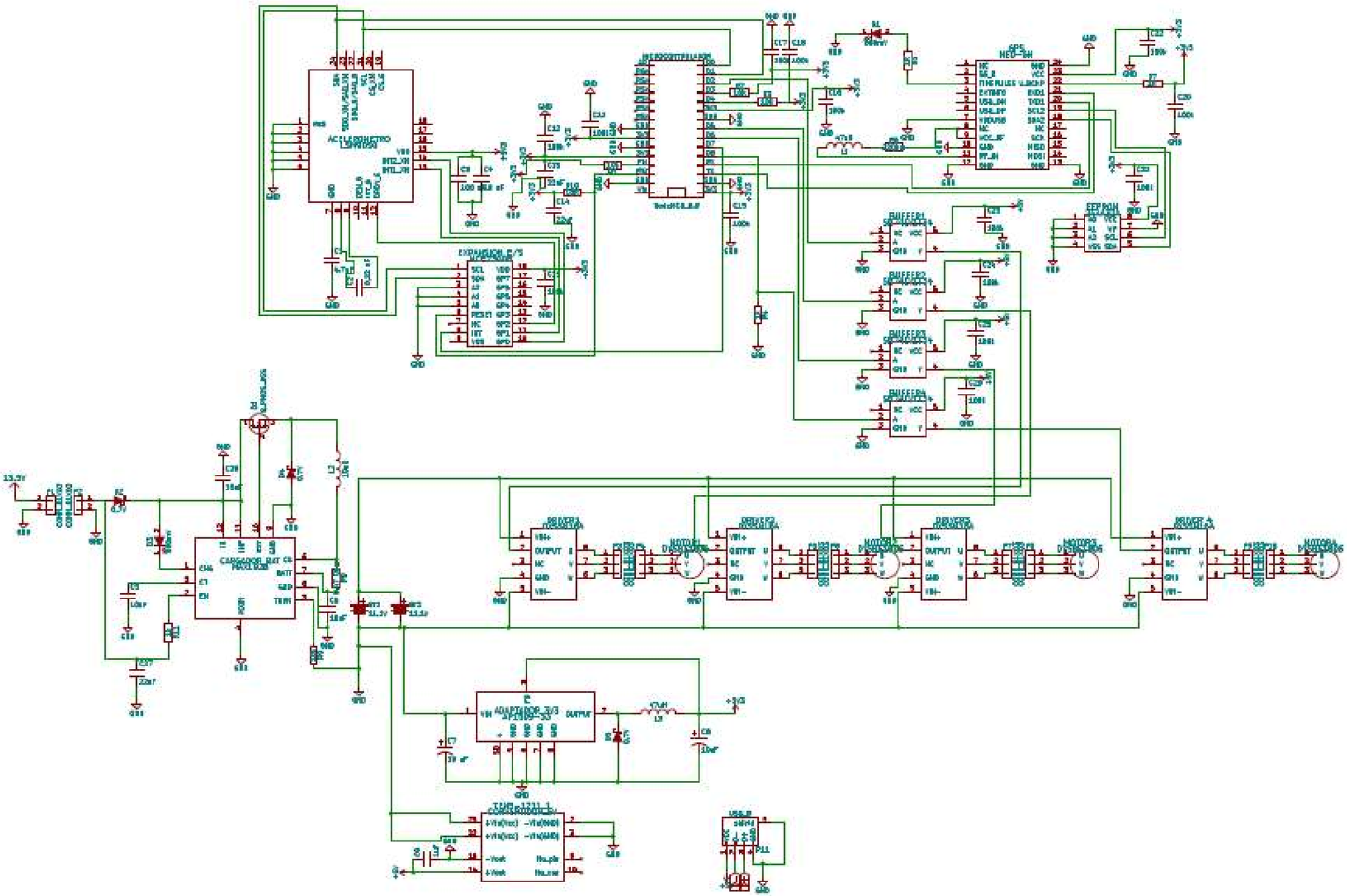

Ilustración 54: Circuito electrónico cuadricóptero

6.3. DISEÑO DE PLACA DE CIRCUITO IMPRESO

Una vez realizado el diseño del circuito electrónico con KiCAD, se realiza a través del mismo la PCB (Placa de Circuito Impreso), para ello se acude a la herramienta PCBNew, donde se realiza el conexionado de las mismas, obteniendo la siguiente placa:

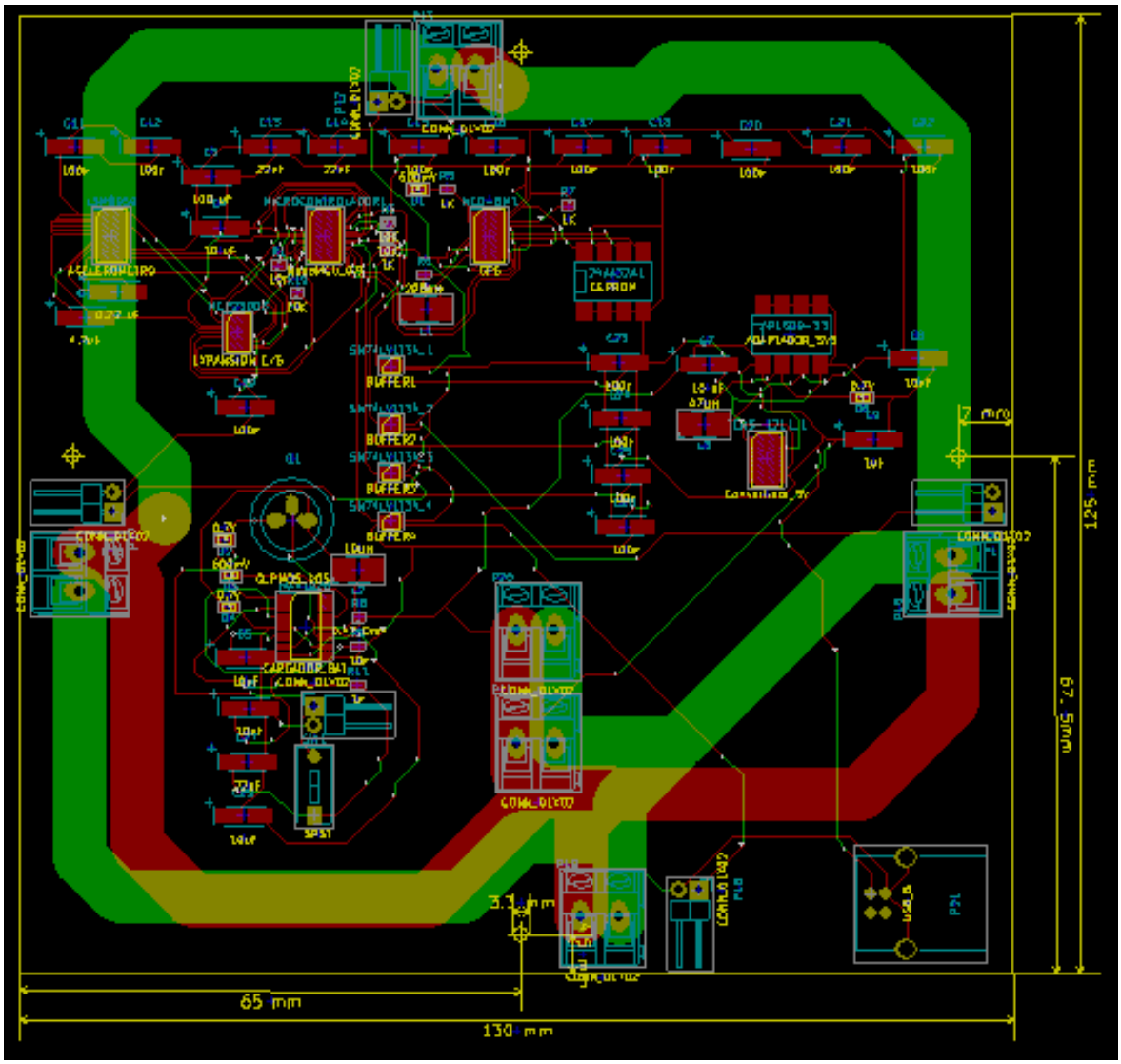

Ilustración 55: PCB Cuadricóptero

En la placa pueden apreciarse las dimensiones y agujeros en los que va atornillada a la base superior del dron. Las pistas de los componentes electrónicos son de 0,3 mm, suficientes ya que es muy baja la corriente de funcionamiento de estos elementos, mientras que las de alimentación de motores son de 7 mm para soportar la corriente de 16 A necesaria. La misma se ha hallado por medio de la siguiente fórmula, donde K es un coeficiente que vale 0,048, H el grosor fijado a 0,07mm y dT el aumento de temperatura en grados C:

$$I = K \cdot dT^{0,44} \cdot (\frac{W}{40} \cdot H)^{0,725}; 16A = 0,048 \cdot 10C^{0,44} \cdot (\frac{W}{40} \cdot 0,07mm)^{0,725}; W = 6,87mm \rightarrow 7mm$$

6.4. BASE DE CARGA

El dron irá situado en una base que permitirá cargar las baterías mientras el sistema se encuentre en reposo, de esta forma se busca optimizar el tiempo de espera y que el cuadricóptero se encuentre con la batería suficiente en el momento de realizar cualquier tipo de ruta. La base será de madera e incluirá dos pistas conectadas al transformador de corriente anteriormente seleccionado, de modo que, al situar el dron encima, éste se cargue al disponer de un tren de aterrizaje metálico cableado directamente al cargador de baterías.

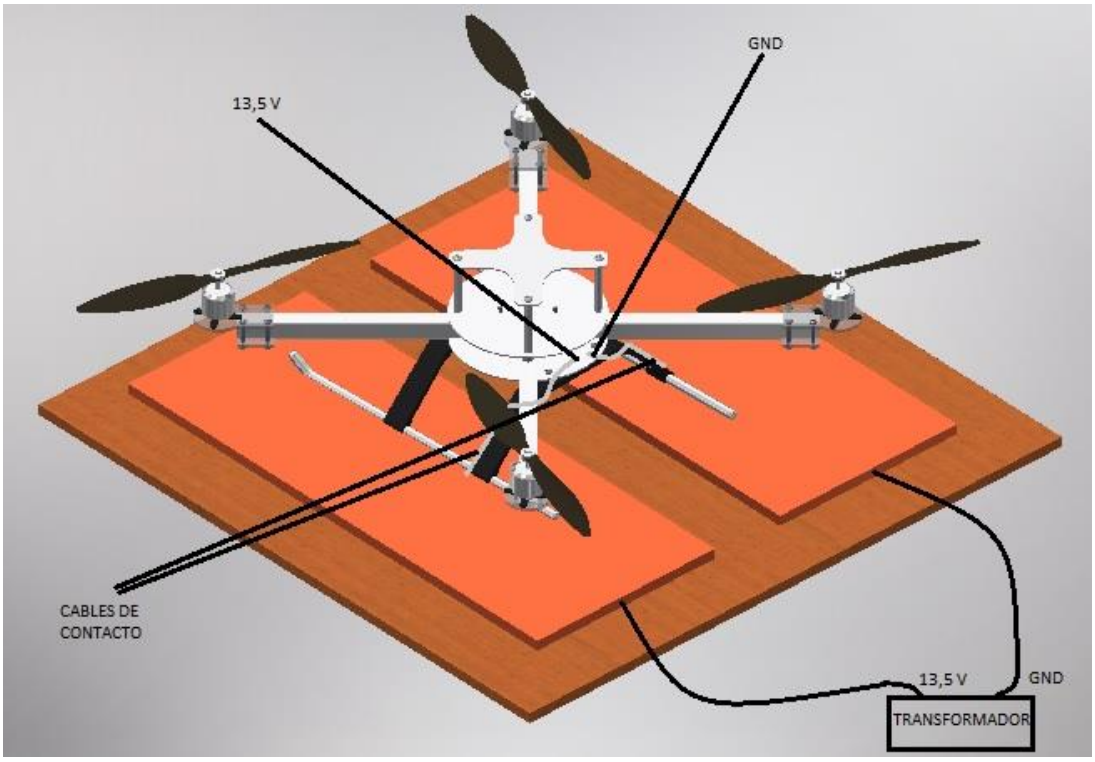

Ilustración 56: Cuadricóptero y base de carga

La base de carga dispondrá de las siguientes dimensiones:

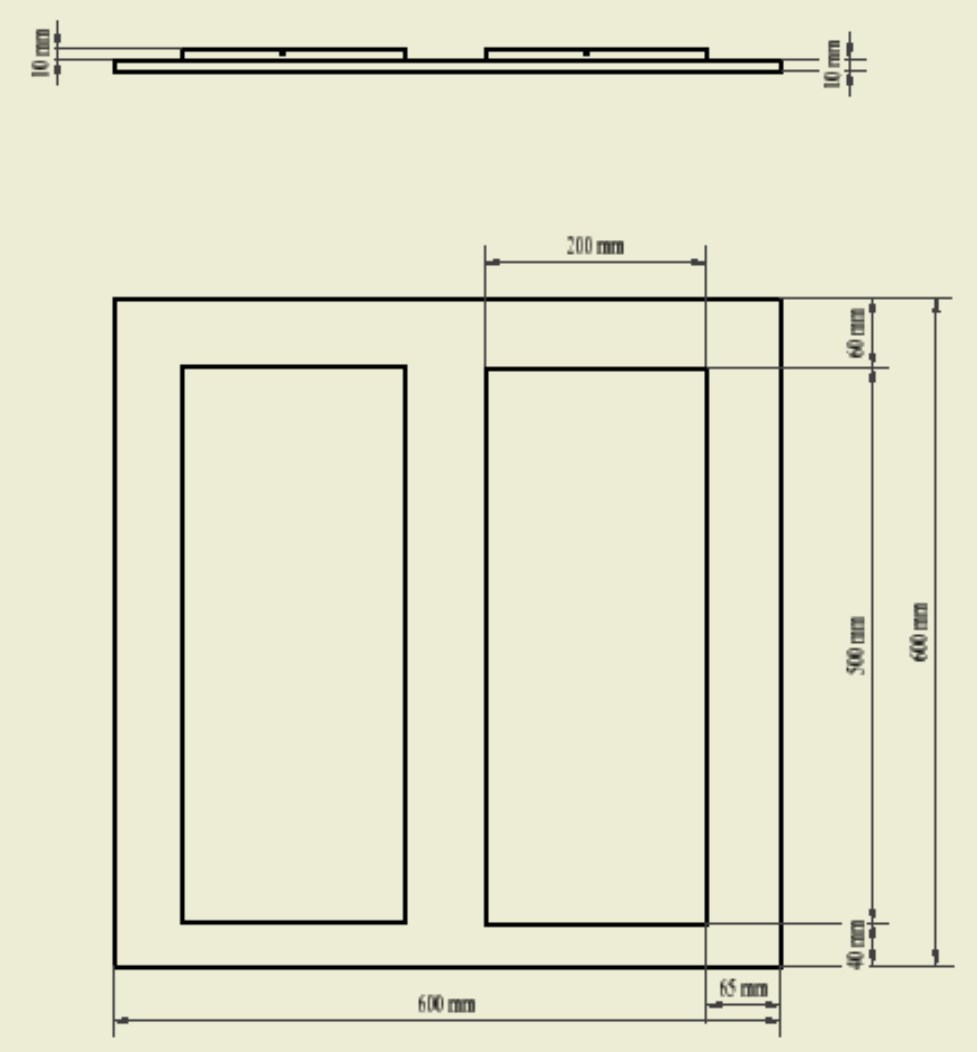

Ilustración 57: Dimensiones base de carga

6.5. DISEÑO DE SOFTWARE DE CONTROL

Por último, se va a realizar el diseño de software del cuadricóptero, para ello en primer lugar se diseña los UML de casos de uso, posteriormente los UML correspondientes a diagramas de actividad y finalmente el diseño de la aplicación en Android.

6.5.1. Diagramas de casos de uso

Estos diagramas UML se han dividido en tres bloques principales: Dron, Smartphone y Sistema de Seguridad.

6.5.1.1. Dron

En primer lugar, se ha reflejado el proceso llevado a cabo por el dron cuadricóptero en su interacción con el usuario a la hora de realizar su procedimiento habitual de funcionamiento

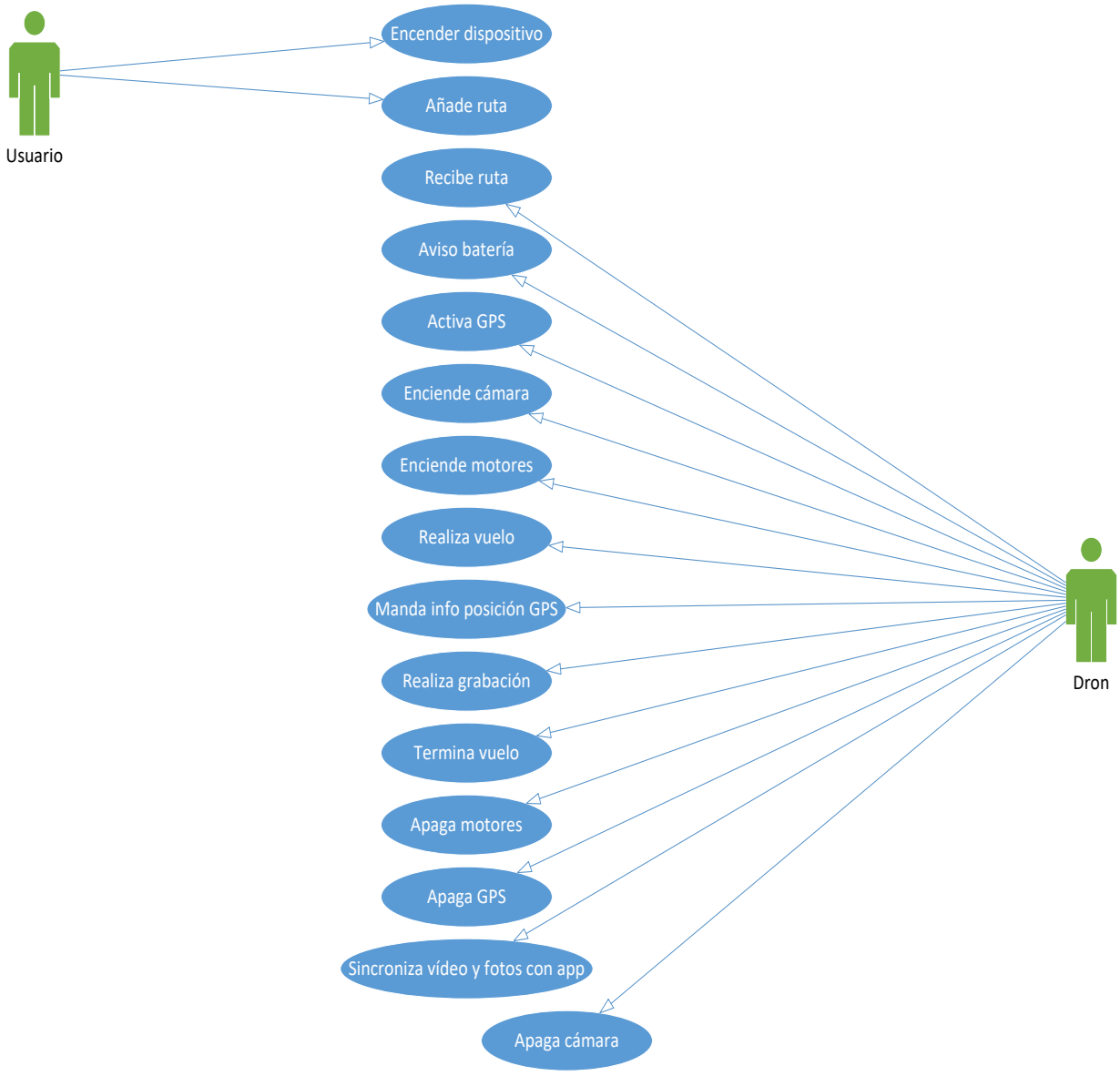

Ilustración 58: Diagrama de casos de uso Dron

6.5.1.2. Smartphone

Posteriormente, se ha diseñado el proceso de interacción del dron cuadricóptero con el Smartphone en el que se encuentra la aplicación mediante la cual se realiza el proceso de vigilancia remota.

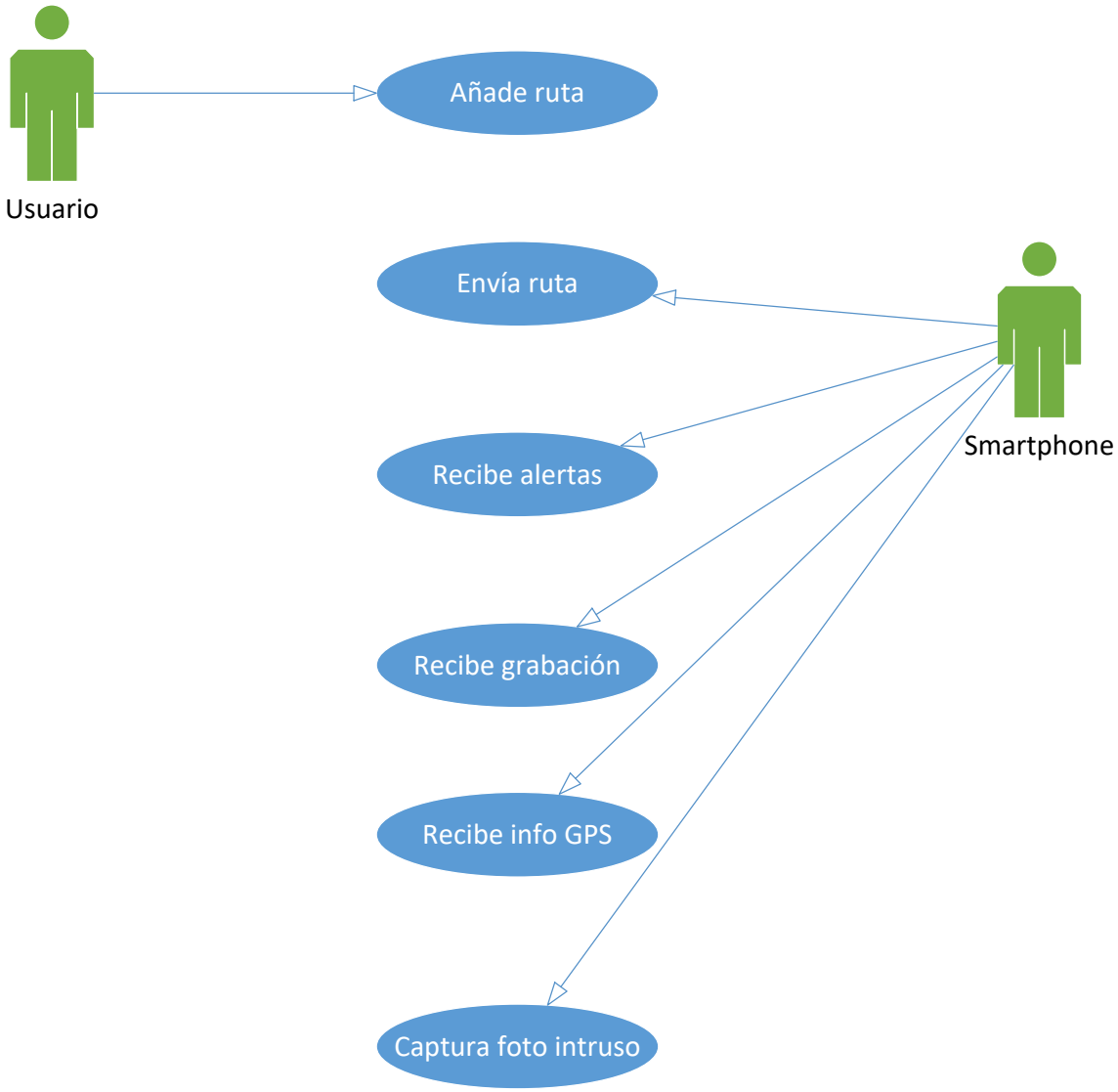

Ilustración 59: Diagrama de casos de uso Smartphone

6.5.1.3. Sistema de seguridad

Por último, se ha descrito el proceso llevado a cabo por el sistema de vigilancia que realiza habitualmente el cuadricóptero interactuando con las barreras infrarrojas instaladas en el recinto a vigilar.

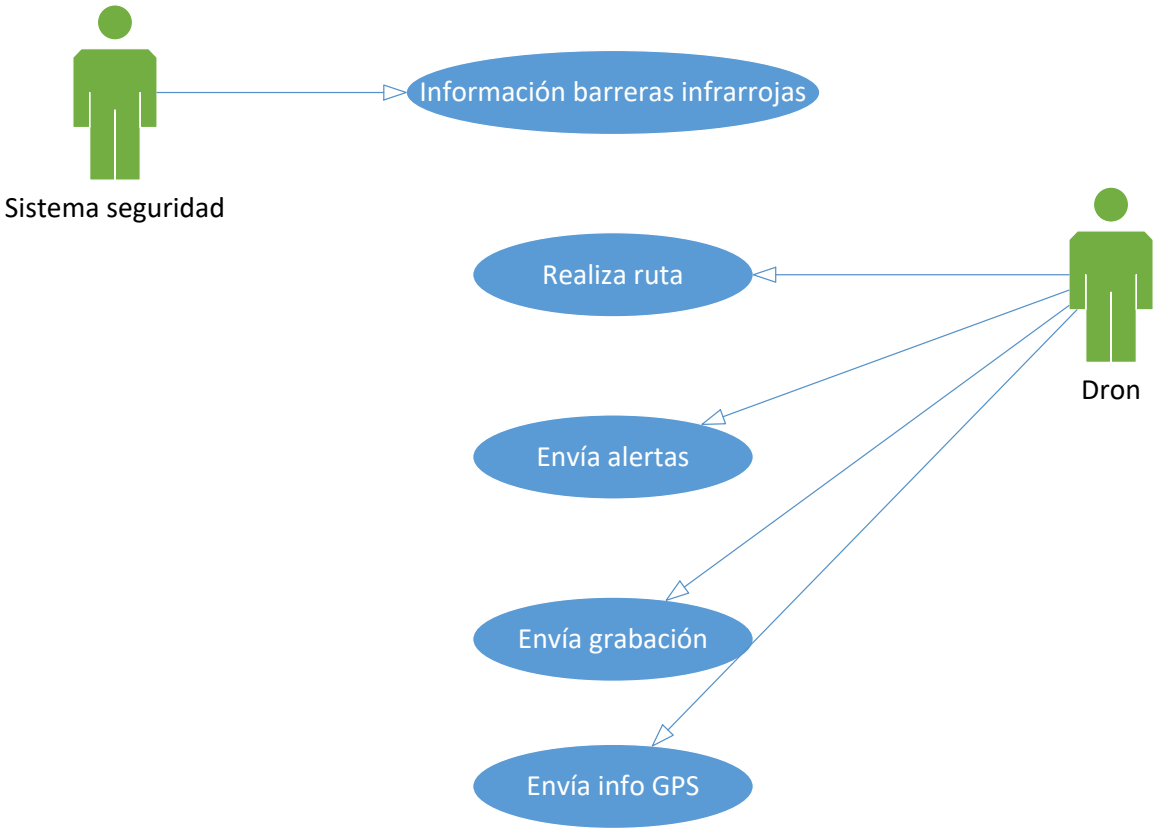

Ilustración 60: Diagrama de casos de uso Sistema de seguridad

6.5.2. Diagramas de actividad

Una vez realizados de forma general los UML de casos de uso, se realizan los diagramas de actividad detallando cada proceso existente en los mismos.

6.5.2.1. Encender dispositivo

Encender dispositivo	
Nombre: Encender dispositivo Descripción: El usuario activa el sistema situado en su base de carga (home). Actores: Usuario, dron (sistema). Casos de uso relacionados: Dron	
Usuario: 1.-El usuario activa el dispositivo	Sistema: 2.-El sistema carga

Tabla 2: Diagrama de actividad Encender dispositivo

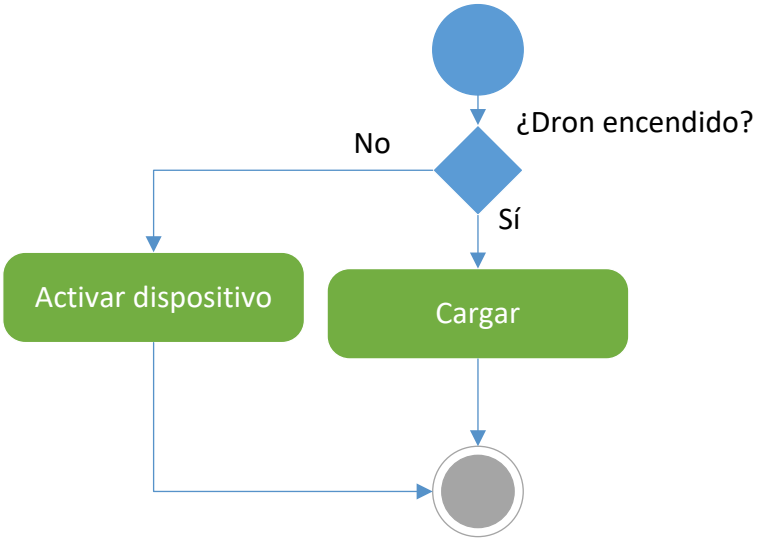

Ilustración 61: Diagrama de actividad Encender dron

6.5.2.2. Añadir ruta

Añadir ruta	
Nombre: Añadir ruta Descripción: El usuario añade una ruta GPS mediante el smartphone y ésta es asignada a una barrera infrarroja del sistema de seguridad, a continuación es enviada al dron. Actores: Usuario, smartphone, dron (sistema). Casos de uso relacionados: Dron, smartphone, sistema de seguridad	
Usuario: 1.-Añade ruta 2.-Asigna ruta Smartphone: 3.-Envía ruta	Sistema: 4.-Recibe ruta

Tabla 3: Diagrama de actividad Añadir ruta

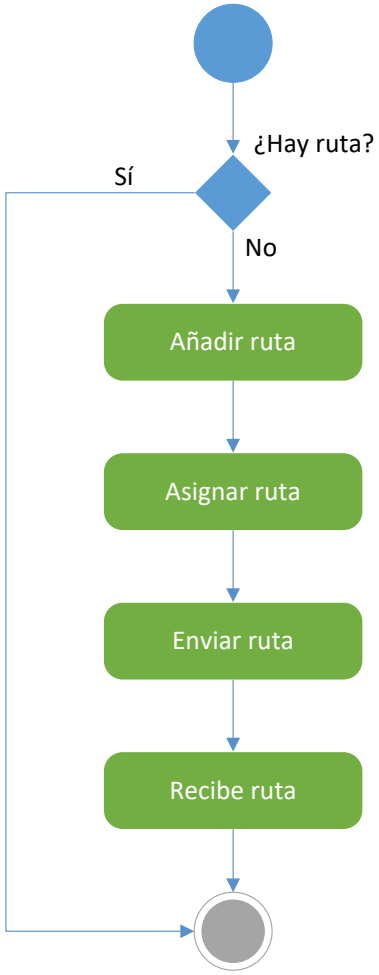

Ilustración 62: Diagrama de actividad Añadir ruta

6.5.2.3. *Aviso de batería*

Aviso batería	
Nombre: Aviso batería Descripción: Cuando la batería no es suficiente envía un aviso al smartphone del usuario, ordenando al dron, en caso de encontrarse en pleno vuelo , a volver a la base de carga. Actores: Smartphone, dron (sistema). Casos de uso relacionados: Dron	
Smartphone: 3.-Recibe aviso	Sistema: 1.-Batería baja 2.-Manda aviso

Tabla 4: Diagrama de actividad Aviso de batería

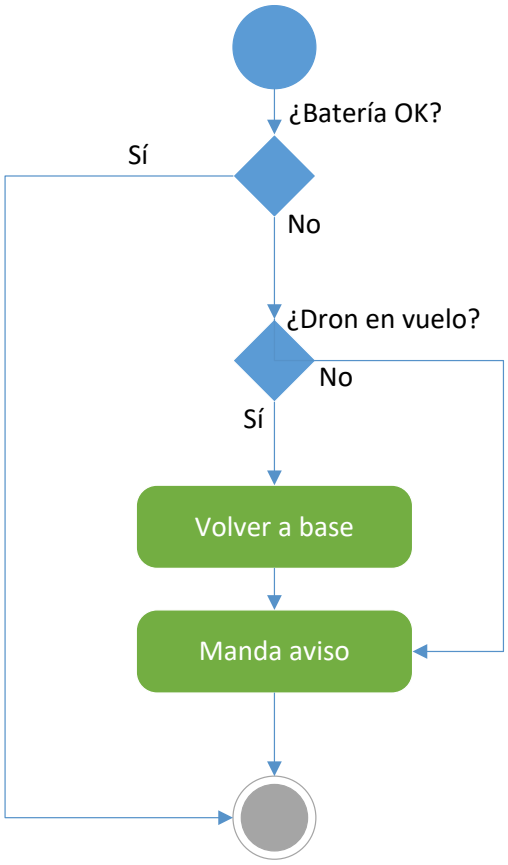

Ilustración 63: Diagrama de actividad Aviso de batería

6.5.2.4. Información GPS

Información GPS	
Nombre: Información GPS. Descripción: En todo momento, el sistema envía información vía GPS sobre su posición en ese instante. Actores: Usuario, dron (sistema). Casos de uso relacionados: Smartphone, sistema de seguridad.	
Smartphone: 2.-Recibe info GPS	Sistema: 1.-Envía info GPS

Tabla 5: Diagrama de actividad Información GPS

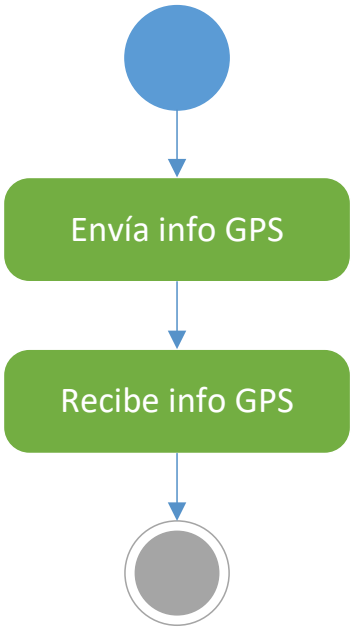

Tabla 6: Diagrama de actividad Información GPS

6.5.2.5. Grabación

Grabación	
Nombre: Grabación Descripción: La cámara incluida en el dron filma la ruta y, una vez terminada ésta la envía mediante Wi-Fi al smartphone. Actores: Smartphone, dron (sistema). Casos de uso relacionados: Smartphone, sistema de seguridad	
Smartphone: 3.-Recibe grabación	Sistema: 1.-Realiza grabación 2.-Envía grabación

Tabla 7: Diagrama de actividad grabación

Ilustración 64: Diagrama de actividad Grabación

6.5.2.6. Realizar ruta

Realizar ruta
Nombre: Realizar ruta Descripción:El dron, una vez recibe información de las barreras infrarrojas, enciende los motores y comienza el vuelo de la ruta correspondiente por puntos GPS a la barrera asignada. Actores: Dron (sistema). Casos de uso relacionados: Sistema de seguridad.
Sistema: 1.-Lee punto GPS 2.-Sube o baja hasta la altura del próximo punto 3.-Realiza el giro necesario para ir al siguiente punto 4.-Acude al siguiente punto en línea recta

Tabla 8: Diagrama de actividad Realizar ruta

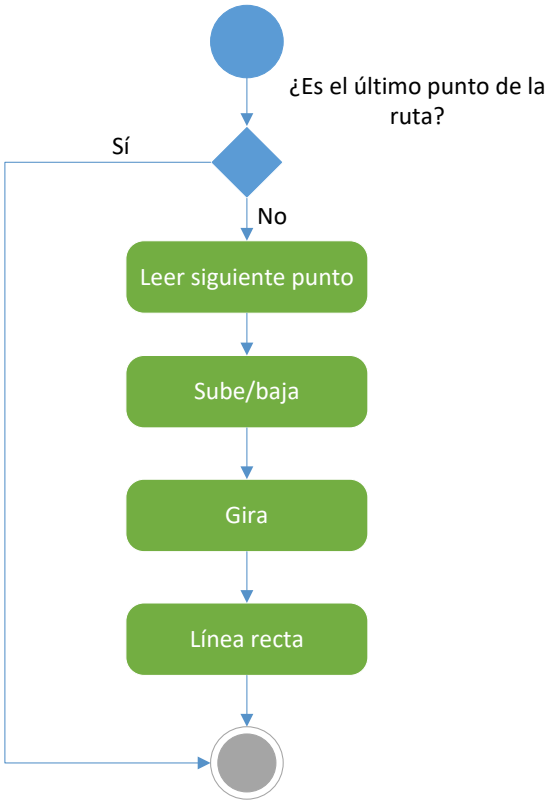

Ilustración 65: Diagrama de actividad Realizar ruta

6.5.2.6.1. Distribución de motores

Para realizar los movimientos de sube/baja, giro y línea recta, se ha de tener en cuenta que la disposición de motores del dron es la siguiente:

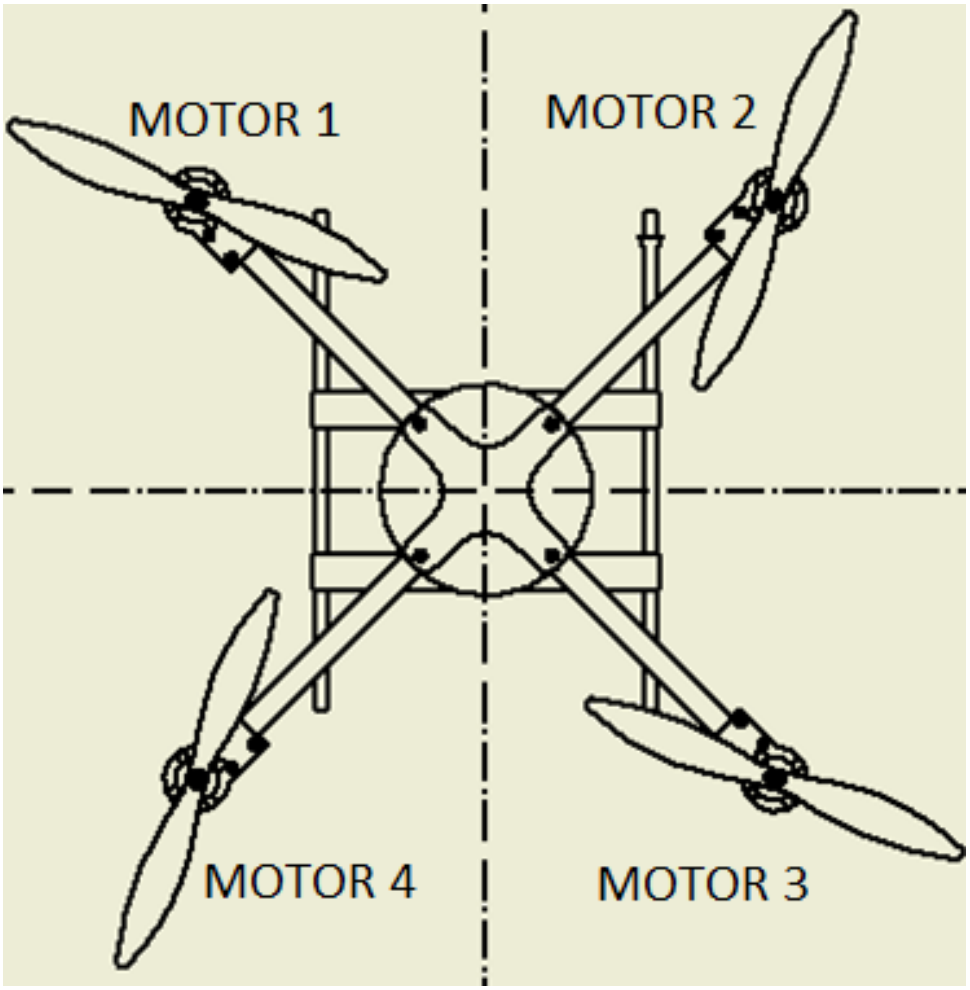

Ilustración 66: Disposición motores cuadricóptero

6.5.2.6.2. Sube/Baja

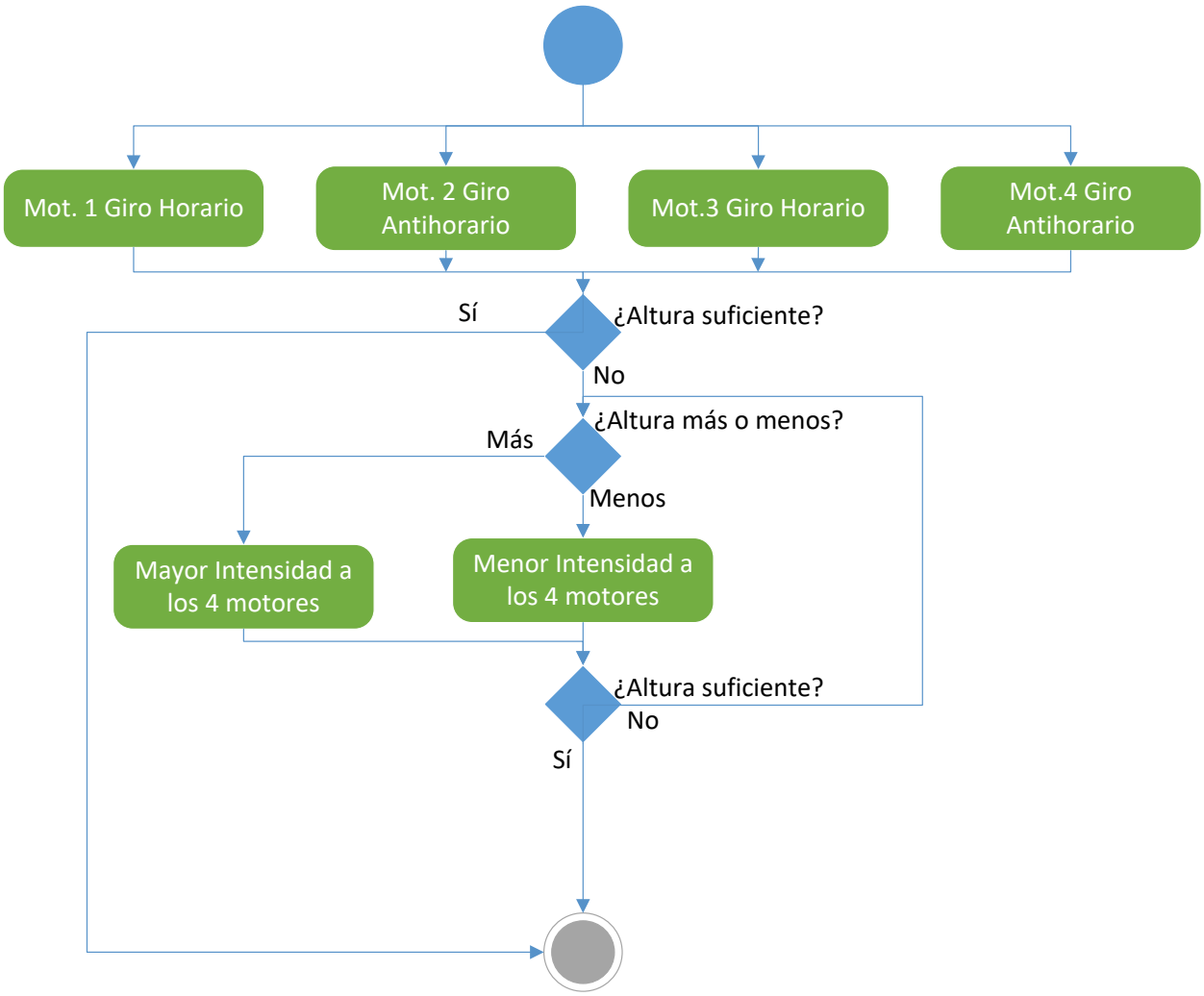

Ilustración 67: Diagrama de actividad sube/baja

6.5.2.6.3. Girar

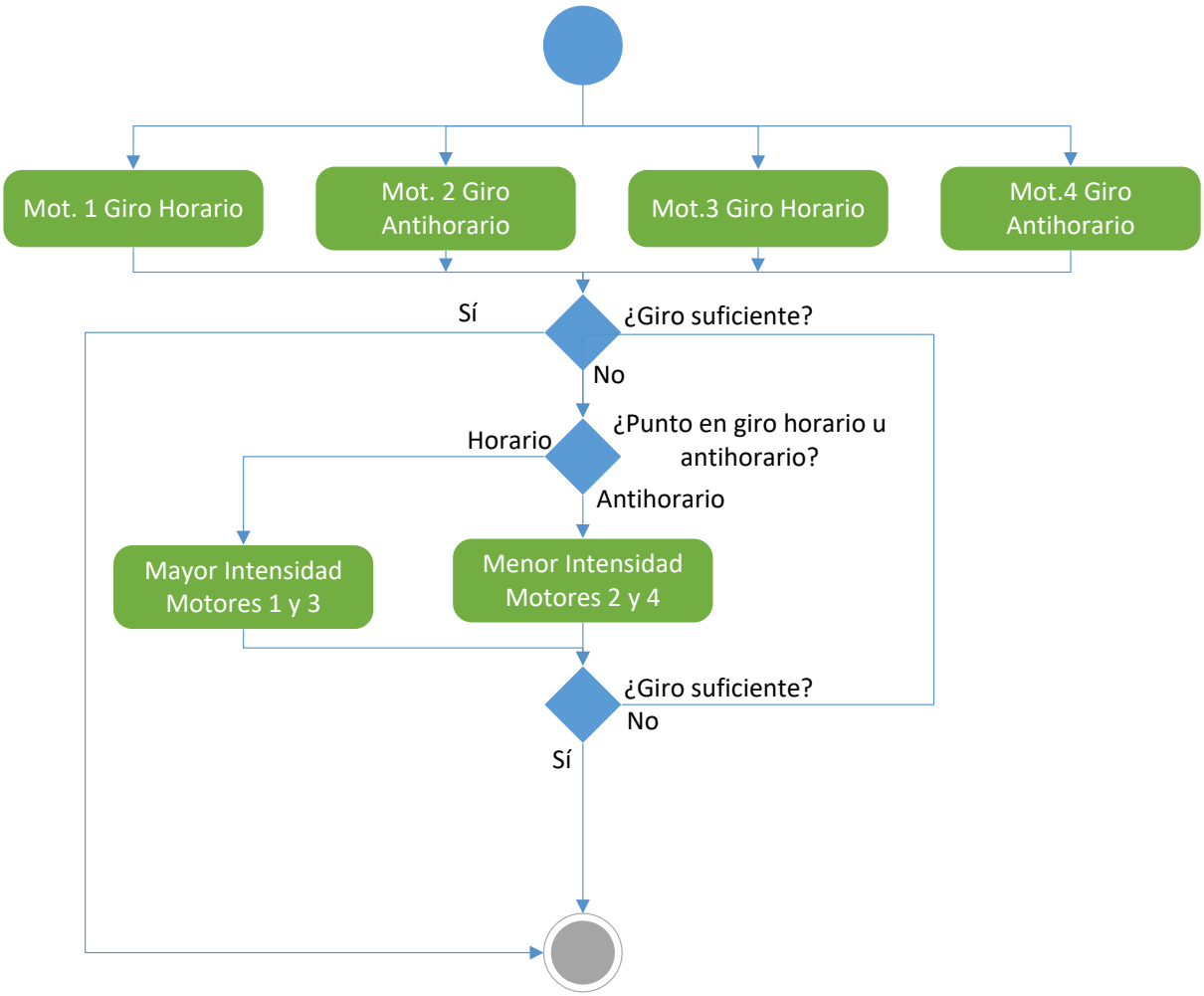

Ilustración 68: Diagrama de actividad Girar

6.5.2.6.4. Línea recta

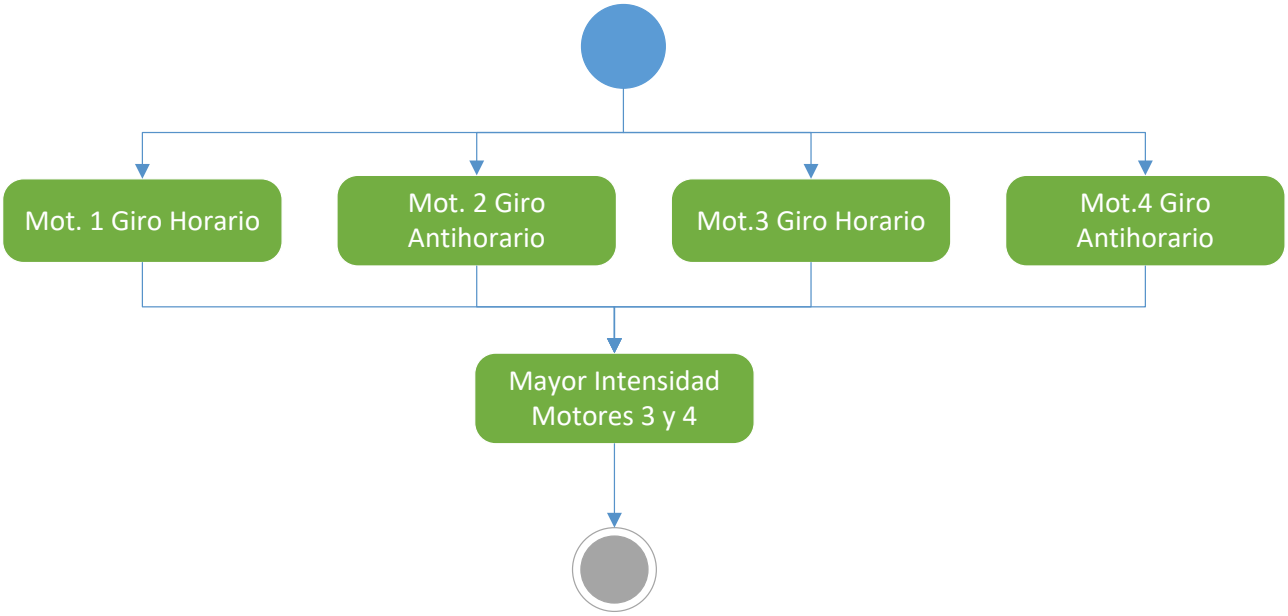

Ilustración 69: Diagrama de actividad Línea recta

6.5.2.7. Alertas

Alertas	
Nombre: Encender dispositivo Descripción: Al observar intruso envía alerta al smartphone del usuario. Actores: Smartphone, dron (sistema). Casos de uso relacionados: Smartphone, sistema seguridad	
Smartphone: 2.-Recibe alertas	Sistema: 1.-Envía alertas

Tabla 9: Diagrama de actividad Alertas

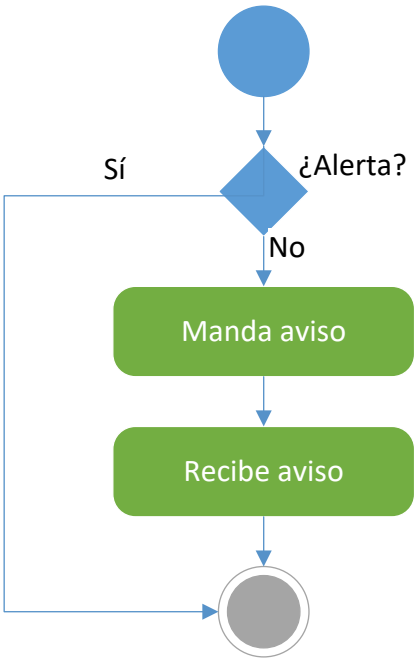

Ilustración 70: Diagrama de actividad Alertas

6.5.2.8. *Información barreras infrarrojas*

Info barreras infrarrojas	
Nombre: Info barreras infrarrojas Descripción: Las barreras infrarrojas del recinto tienen asignada cada una de ellas una ruta por parte del usuario, una vez haya sido atravesada, esa barrera se comunica vía Wi-Fi con el dron, de forma que éste establece la ruta. Actores: Sistema de seguridad, dron (sistema). Casos de uso relacionados: Sistema de seguridad.	
Sistema de seguridad: 1.-Envía info barrera	Sistema: 2.-Recibe info 3.-Establece ruta

Tabla 10: Diagrama de actividad Información barreras infrarrojas

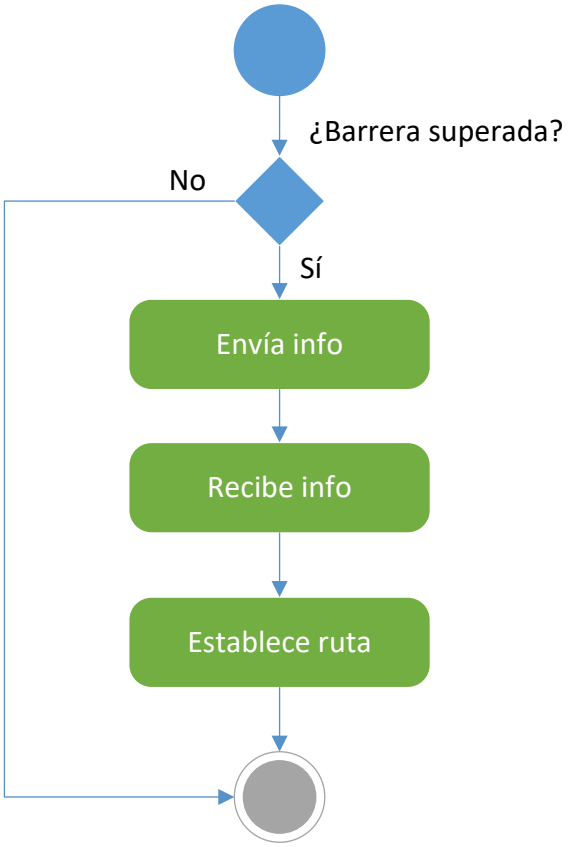

Ilustración 71: Diagrama de actividad Información barreras infrarrojas

6.5.2.9. Foto intruso

Foto intruso	
Nombre: Foto intruso Descripción: Al realizar la ruta, y en caso de detectar un extraño, realiza una fotografía del mismo, que una vez terminada la ruta es enviada vía Wi-Fi al smartphone del usuario.. Actores: Smartphone, dron (sistema). Casos de uso relacionados: Smartphone, sistema seguridad.	
Smartphone: 3.-Recibe foto intruso	Sistema: 1.-Toma foto intruso 2.-Envía foto intruso

Tabla 11: Diagrama de actividad Foto intruso

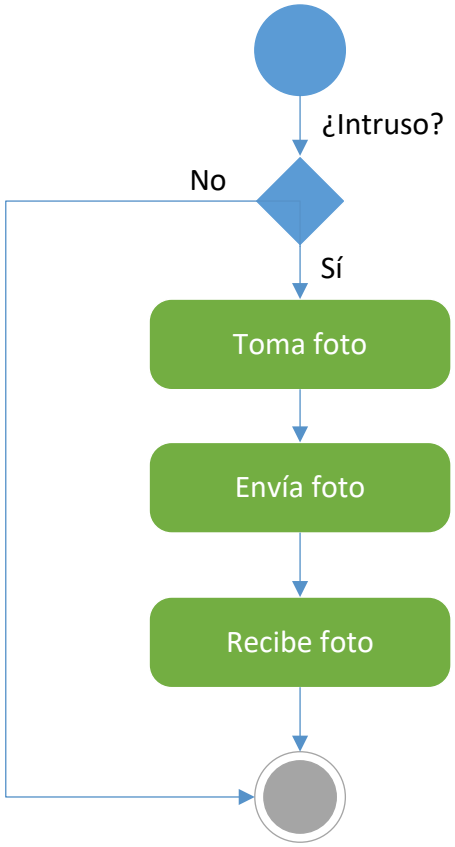

Tabla 12: Diagrama de actividad Foto intruso

6.5.3. Diseño de aplicación móvil Android

Finalmente, se ha realizado el diseño de la aplicación móvil de vigilancia del cuadricóptero, en la cual se podrá controlar la zona de forma remota por medio de un Smartphone con Android que se sincronizará vía Wi-Fi con el cuadricóptero.

6.5.3.1. Menú inicial

En él se puede acceder a diferentes funciones, tales como encender y apagar el sistema, consultar el estado de la ruta, ver las alertas recibidas, acceder a las rutas que realiza el sistema así como a las fotos de intrusos tomadas o los vídeos grabados.

Ilustración 72: Menú inicial App Android

6.5.3.2. Estado ruta

En esta pantalla se puede observar en tiempo real la situación del dron respecto a la ruta que está realizando por medio de GPS.

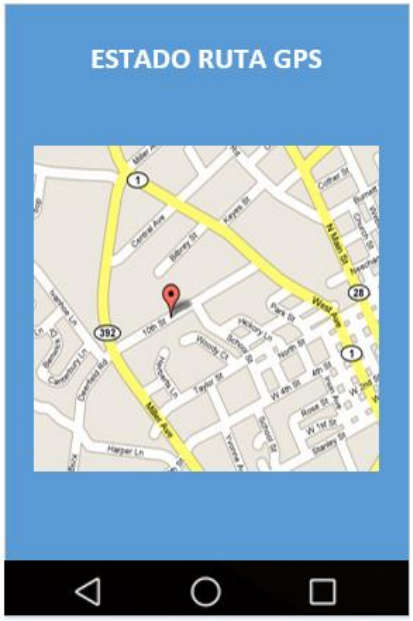

Ilustración 73: Estado ruta GPS Aplicación Android

6.5.3.3. Alertas

A través de esta sección se puede observar las alertas enviadas por el sistema, como puede ser el momento en el que ha encontrado un intruso o si la batería es insuficiente para el recorrido a realizar.

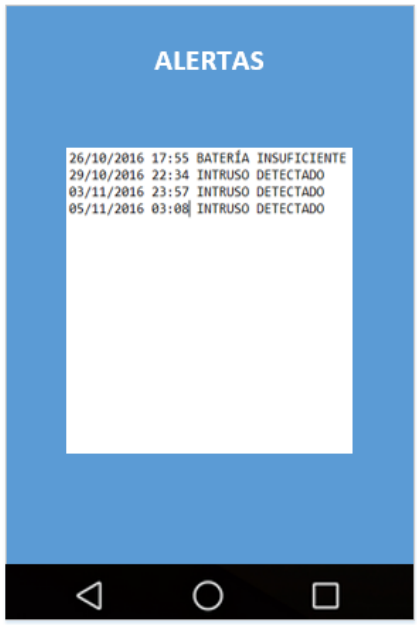

Ilustración 74: Alertas Aplicación Android

6.5.3.4. Rutas

En esta pantalla el usuario tiene la opción de añadir una nueva ruta o asignar una ruta al verse atravesada una barrera infrarroja del recinto.

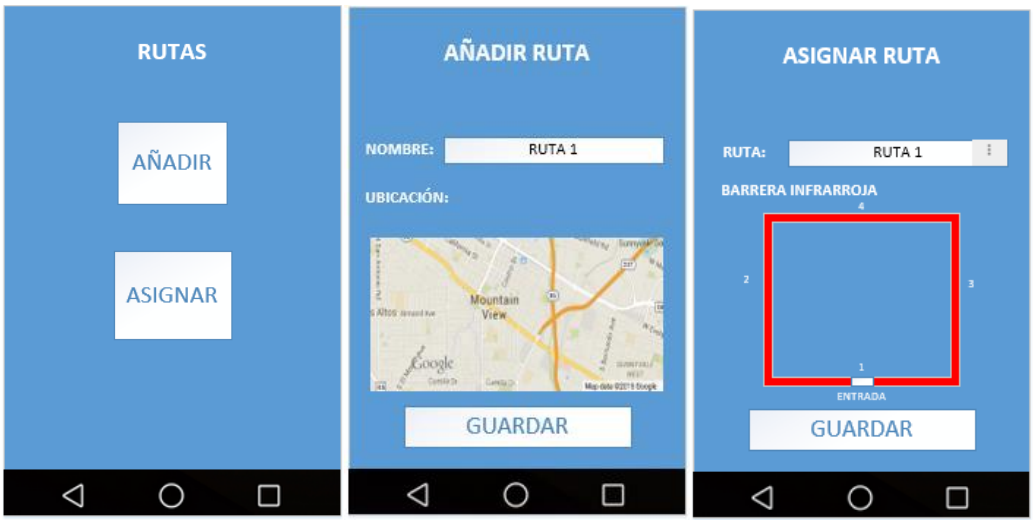

Ilustración 75: Rutas Aplicación Android

6.5.3.5. Fotografías

A través de esta opción se pueden observar las fotografías que ha tomado el sistema al observar un intruso.

Ilustración 76: Fotografías Aplicación Android

6.5.3.6. Vídeos

Por último, por medio de este menú se accede a las grabaciones realizadas por la cámara durante el recorrido realizado.

Ilustración 77: Vídeos Aplicación Android

7. CONCLUSIONES Y LÍNEAS FUTURAS

7.1. CONCLUSIONES

Las conclusiones que se han podido extraer de este trabajo fin de grado (TFG) han sido las siguientes:

- Se ha diseñado el sistema completo de un dron cuadricóptero de vigilancia con el análisis de componentes y funciones y la cohesión entre ellos.
- Se ha realizado el diseño mecánico del cuadricóptero, de tal forma que se ha estudiado el equilibrio entre durabilidad de sus componentes y ligereza, todo ello por medio del software Autodesk Inventor.
- El diseño de la placa de circuito impreso ha sido llevado a cabo mediante el software KiCad por medio de su herramienta PCBnew.
- La placa de circuito impreso irá atornillada en la base superior del cuadricóptero, y a su vez cableada a las patas del tren de aterrizaje que se encuentran en contacto con la base de carga, que a su vez irá conectada al transformador.
- A la hora de realizar la placa de circuito impreso se ha analizado cada componente para obtener los resultados y configuración más óptimos, de forma que se ha logrado un buen funcionamiento del conjunto de los mismos.
- El sistema de control ha sido diseñado de forma que el cuadricóptero, situado en su base de carga, recibe información por medio de barreras infrarrojas de seguridad para, a continuación, realizar la ruta programada mientras filma el recorrido.
- El software de control se ha especificado utilizando diagramas UML de actividad y de casos de control especificando cada una de las funciones y situaciones en las que puede desenvolverse el dron.
- La aplicación móvil para Android es la manera llevada a cabo por el usuario para comunicarse con el cuadricóptero, el cual realiza posteriormente el resto de situaciones de manera automática.

- Tanto para el diseño de las ventanas de la aplicación móvil como los diagramas UML pertenecientes al software de control han sido realizadas mediante el software Microsoft Visio.

7.2. LÍNEAS FUTURAS

Finalmente, las diversas tareas de cara a profundizar en este proyecto serían las siguientes:

- Fabricación del modelo en 3D, así como de su placa de circuito impreso, de cara a construirlo en la realidad y verificar el correcto funcionamiento de cada uno de sus componentes y el conjunto de los mismos.
- Programación de la aplicación Android y comprobación del correcto funcionamiento de la misma en un smartphone.
- Diseño del sistema de seguridad formado por barreras infrarrojas y de su comunicación con el cuadricóptero, por medio del cual se podría comprobar su funcionamiento tanto con el dron como con la aplicación móvil.

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Relación de documentos

(X) Memoria ..... 99 páginas

(_) Anexos .....283 páginas

La Almunia, a 29 de 11 de 2016

Firmado: Mario Urgel García

ESCUELA UNIVERSITARIA POLITÉCNICA

DE LA ALMUNIA DE DOÑA GODINA (ZARAGOZA)

ANEXOS

Diseño de un dron de vigilancia de forma remota controlado por teléfono móvil

Design of a surveillance drone remotely controlled by smartphone

424.16.31

Autor: Mario Urgel García

Director: Javier Esteban Escaño

Fecha: 29/11/2016

INDICE DE CONTENIDO

Autor: Mario Urgel García
424.16.31

1. ANEXO1 DOCUMENTACIÓN

En este anexo se va a exponer toda la información en forma de datasheet que se ha utilizado para llevar a cabo el desarrollo del cuadricóptero.

1.1. ÍNDICE ANEXOS

1. Módulo de expansión de entradas y salidas.
2. Transformador.
3. Convertidor 5V.
4. Convertidor 3V3.
5. Memoria EEPROM.
6. Acelerómetro, giroscopio y magnetómetro.
7. Cargador de baterías.
8. Módulo GPS.
9. Buffer.
10. Driver motores.

Autor: Mario Urgel García
424.16.31

MCP23008/MCP23S08

8-Bit I/O Expander with Serial Interface

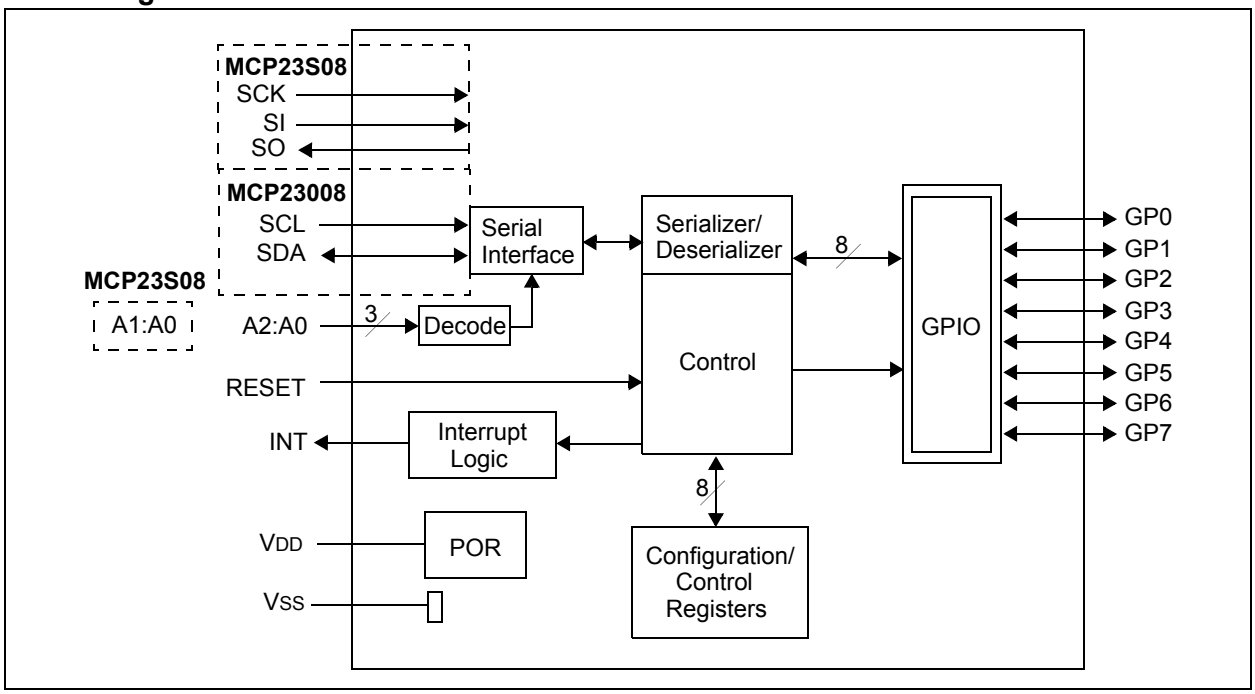
Features

- 8-bit remote bidirectional I/O port
  - I/O pins default to input
- High-speed I^2C™ interface (**MCP23008**)
  - 100 kHz
  - 400 kHz
  - 1.7 MHz
- High-speed SPI interface (**MCP23S08**)
  - 10 MHz
- Hardware address pins
  - Three for the MCP23008 to allow up to eight devices on the bus
  - Two for the MCP23S08 to allow up to four devices using the same chip-select
- Configurable interrupt output pin
  - Configurable as active-high, active-low or open-drain
- Configurable interrupt source
  - Interrupt-on-change from configured defaults or pin change
- Polarity Inversion register to configure the polarity of the input port data
- External reset input
- Low standby current: 1 µA (max.)
- Operating voltage:
  - 1.8V to 5.5V @ -40°C to +85°C
    I^2C @ 100 kHz
    SPI @ 5 MHz
  - 2.7V to 5.5V @ -40°C to +85°C
    I^2C @ 400 kHz
    SPI @ 10 MHz
  - 4.5V to 5.5V @ -40°C to +125°C
    I^2C @ 1.7 kHz
    SPI @ 10 MHz

Packages

- 18-pin PDIP (300 mil)
- 18-pin SOIC (300 mil)
- 20-pin SSOP
- 20-pin QFN

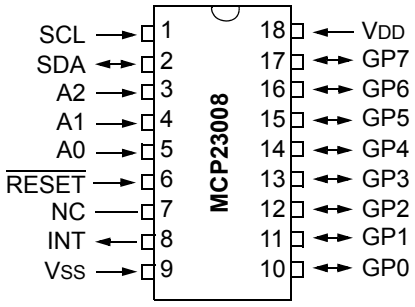
Block Diagram



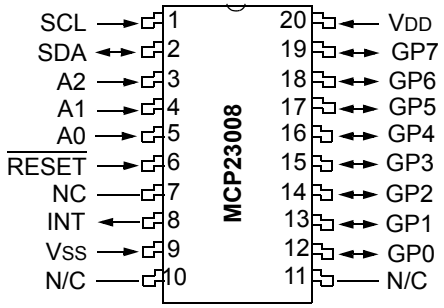
Package Types

MCP23008

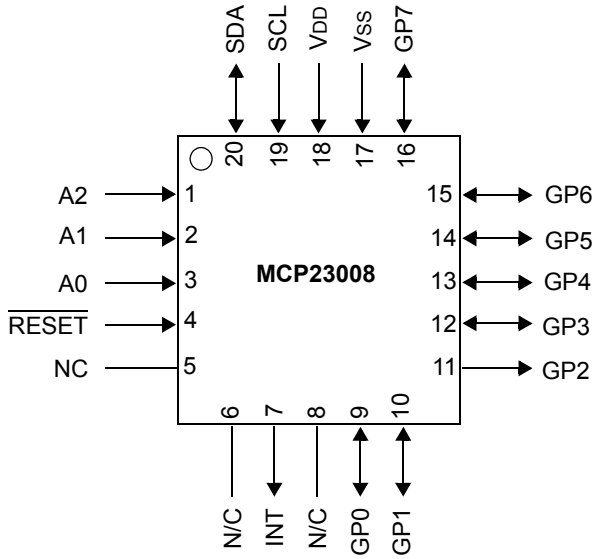
PDIP/SOIC



SSOP



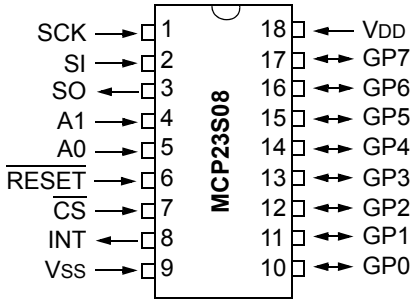
QFN



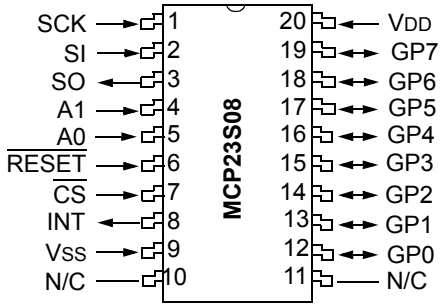
Package Types: (Continued)

MCP23S08

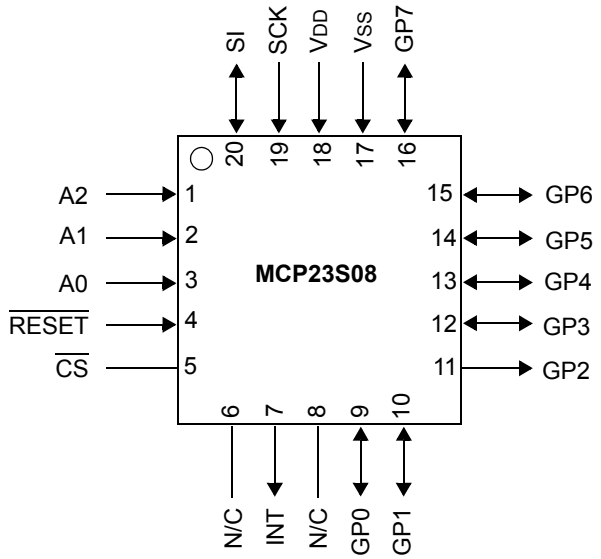
PDIP/SOIC



SSOP



QFN



NOTES:

1.0 DEVICE OVERVIEW

The MCP23X08 device provides 8-bit, general purpose, parallel I/O expansion for I^2C bus or SPI applications. The two devices differ in the number of hardware address pins and the serial interface:

- MCP23008 – I^2C interface; three address pins
- MCP23S08 – SPI interface; two address pins

The MCP23X08 consists of multiple 8-bit configuration registers for input, output and polarity selection. The system master can enable the I/Os as either inputs or outputs by writing the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The interrupt output can be configured to activate under two conditions (mutually exclusive):

1. When any input state differs from its corresponding input port register state, this is used to indicate to the system master that an input state has changed.
2. When an input state differs from a preconfigured register value (DEFVAL register).

The Interrupt Capture register captures port values at the time of the interrupt, thereby saving the condition that caused the interrupt.

The Power-on Reset (POR) sets the registers to their default values and initializes the device state machine.

The hardware address pins are used to determine the device address.

1.1 Pin Descriptions

TABLE 1-1: PINOUT DESCRIPTION

Pin Name	PDIP/ SOIC	QFN	SSOP	Pin Type	Function
SCL/SCK	1	19	1	I	Serial clock input.
SDA/SI	2	20	2	I/O	Serial data I/O (**MCP23008**)/Serial data input (**MCP23S08**).
A2/SO	3	1	3	I/O	Hardware address input (**MCP23008**)/ Serial data output (**MCP23S08**). A2 must be biased externally.
A1	4	2	4	I	Hardware address input. Must be biased externally.
A0	5	3	5	I	Hardware address input. Must be biased externally.
$\overline{\text{RESET}}$	6	4	6	I	External reset input. Must be biased externally.
NC/$\overline{\text{CS}}$	7	5	7	I	No connect (**MCP23008**)/External chip select input (**MCP23S08**).
INT	8	7	8	O	Interrupt output. Can be configured for active-high, active-low or open-drain.
V_{SS}	9	17	9	P	Ground.
GP0	10	9	12	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GP1	11	10	13	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GP2	12	11	14	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GP3	13	12	15	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GP4	14	13	16	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GP5	15	14	17	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GP6	16	15	18	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GP7	17	16	19	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
V_{DD}	18	18	20	P	Power.
N/C	—	6, 8	10, 11	—	—

1.2 Power-on Reset (POR)

The on-chip POR circuit holds the device in reset until V_{DD} has reached a high enough voltage to deactivate the POR circuit (i.e., release the device from Reset). The maximum V_{DD} rise time is specified in **Section 2.0 "Electrical Characteristics"**.

When the device exits the POR condition (releases reset), device operating parameters (i.e., voltage, temperature, serial bus frequency, etc.) must be met to ensure proper operation.

1.3 Serial Interface

This block handles the functionality of the I^2C (MCP23008) or SPI (MCP23S08) interface protocol. The MCP23X08 contains eleven registers that can be addressed through the serial interface block (Table 1-2):

TABLE 1-2: REGISTER ADDRESSES

Address	Access to:
00h	IODIR
01h	IPOL
02h	GPINTEN
03h	DEFVAL
04h	INTCON
05h	IOCON
06h	GPPU
07h	INTF
08h	INTCAP (Read-only)
09h	GPIO
0Ah	OLAT

1.3.1 SEQUENTIAL OPERATION BIT

The Sequential Operation (SEQOP) bit (IOCON register) controls the operation of the address pointer. The address pointer can either be enabled (default) to allow the address pointer to increment automatically after each data transfer, or it can be disabled.

When operating in **Sequential mode** (IOCON.SEQOP = 0), the address pointer automatically increments to the next address after each byte is clocked.

When operating in **Byte mode** (IOCON.SEQOP = 1), the MCP23X08 does not increment its address counter after each byte during the data transfer. This gives the ability to continually read the same address by providing extra clocks (without additional control bytes). This is useful for polling the GPIO register for data changes.

1.3.2 I^2C™ INTERFACE

1.3.2.1 I^2C Write Operation

The I^2C Write operation includes the control byte and register address sequence, as shown in the bottom of Figure 1-1. This sequence is followed by eight bits of data from the master and an Acknowledge (ACK) from the MCP23008. The operation is ended with a STOP or RESTART condition being generated by the master.

Data is written to the MCP23008 after every byte transfer. If a STOP or RESTART condition is generated during a data transfer, the data will not be written to the MCP23008.

Byte writes and sequential writes are both supported by the MCP23008. The MCP23008 increments its address counter after each ACK during the data transfer.

1.3.2.2 I^2C Read Operation

The I^2C Read operation includes the control byte sequence, as shown in the bottom of Figure 1-1. This sequence is followed by another control byte (including the START condition and ACK) with the R/W bit equal to a logic 1 (R/W = 1). The MCP23008 then transmits the data contained in the addressed register. The sequence is ended with the master generating a STOP or RESTART condition.

1.3.2.3 I^2C Sequential Write/Read

For sequential operations (Write or Read), instead of transmitting a STOP or RESTART condition after the data transfer, the master clocks the next byte pointed to by the address pointer (see **Section 1.3.1 "Sequential Operation Bit"** for details regarding sequential operation control).

The sequence ends with the master sending a STOP or RESTART condition.

The MCP23008 address pointer will roll over to address zero after reaching the last register address.

Refer to Figure 1-1.

1.3.3 SPI INTERFACE

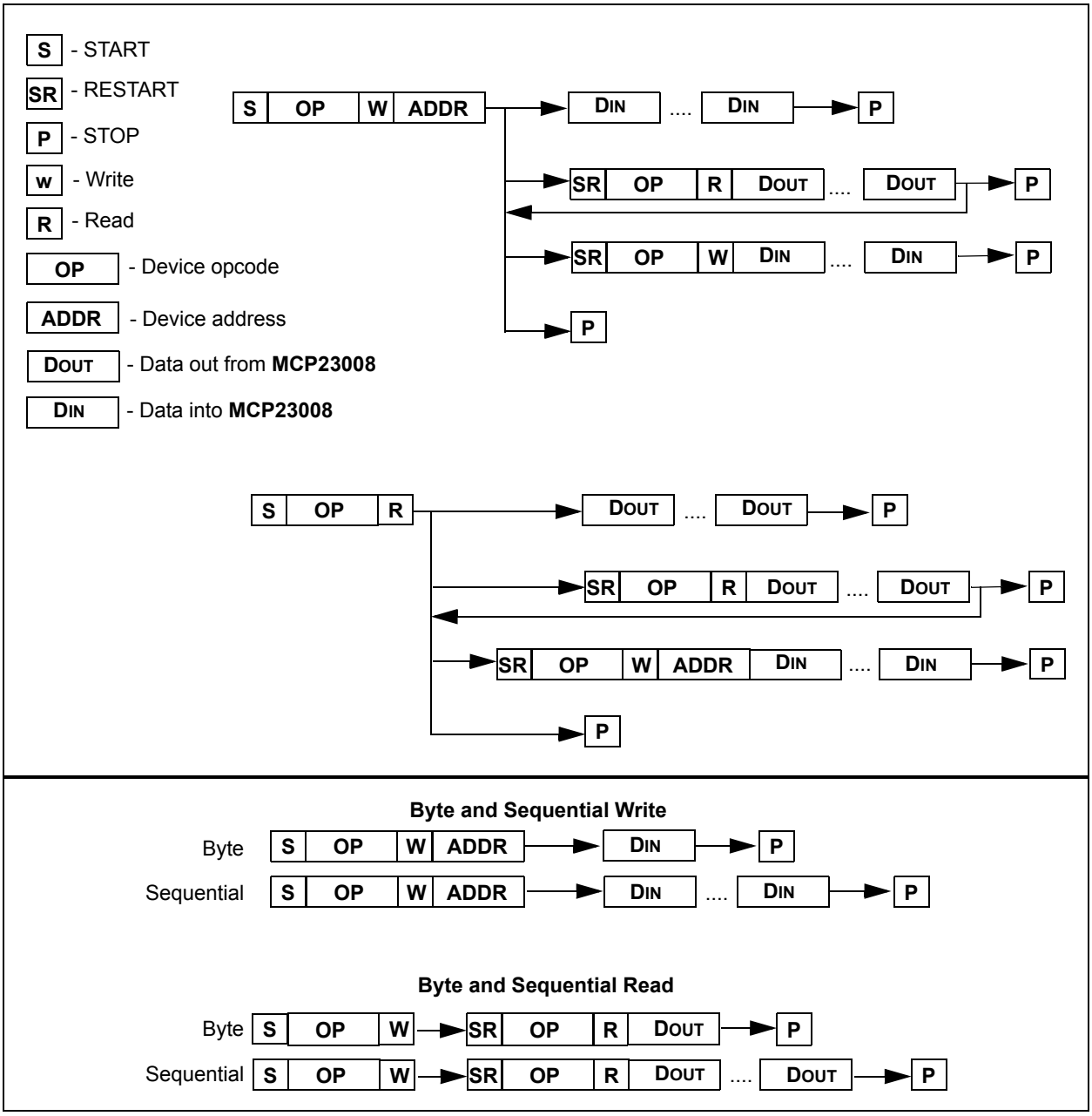
1.3.3.1 SPI Write Operation

The SPI Write operation is started by lowering $\overline{CS}$. The Write command (slave address with R/W bit cleared) is then clocked into the device. The opcode is followed by an address and at least one data byte.

1.3.3.2 SPI Read Operation

The SPI Read operation is started by lowering $\overline{CS}$. The SPI read command (slave address with R/W bit set) is then clocked into the device. The opcode is followed by an address, with at least one data byte being clocked out of the device.

FIGURE 1-1: MCP23008 I²C™ DEVICE PROTOCOL



1.3.3.3 SPI Sequential Write/Read

For sequential operations, instead of deselecting the device by raising $\overline{CS}$, the master clocks the next byte pointed to by the address pointer.

The sequence ends by the raising of $\overline{CS}$.

The MCP23S08 address pointer will roll over to address zero after reaching the last register address.

1.4 Hardware Address Decoder

The hardware address pins are used to determine the device address. To address a device, the corresponding address bits in the control byte must match the pin state.

- MCP23008 has address pins A2, A1 and A0.
- MCP23S08 has address pins A1 and A0.

The pins must be biased externally.

1.4.1 ADDRESSING I²C DEVICES (MCP23008)

The MCP23008 is a slave I²C device that supports 7-bit slave addressing, with the read/write bit filling out the control byte. The slave address contains four fixed bits and three user-defined hardware address bits (pins A2, A1 and A0). Figure 1-2 shows the control byte format.

1.4.2 ADDRESSING SPI DEVICES (MCP23S08)

The MCP23S08 is a slave SPI device. The slave address contains five fixed bits and two user-defined hardware address bits (pins A1 and A0), with the read/write bit filling out the control byte. Figure 1-3 shows the control byte format.

FIGURE 1-2: I²C™ CONTROL BYTE FORMAT

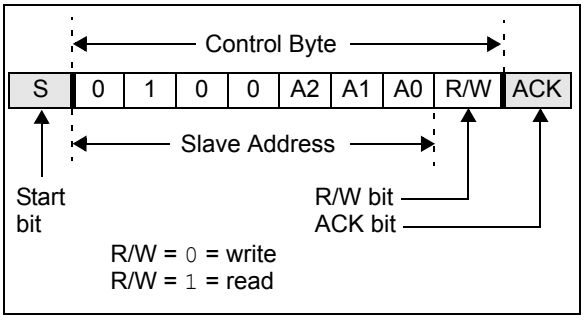


FIGURE 1-3: SPI CONTROL BYTE FORMAT

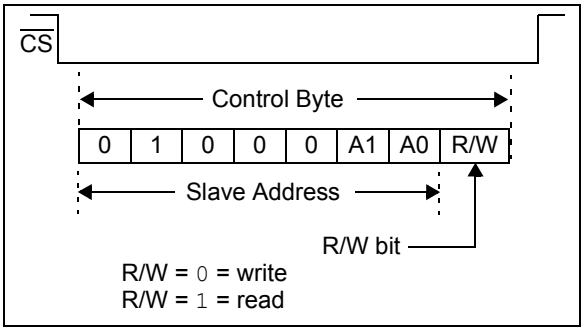


FIGURE 1-4: I²C™ ADDRESSING REGISTERS

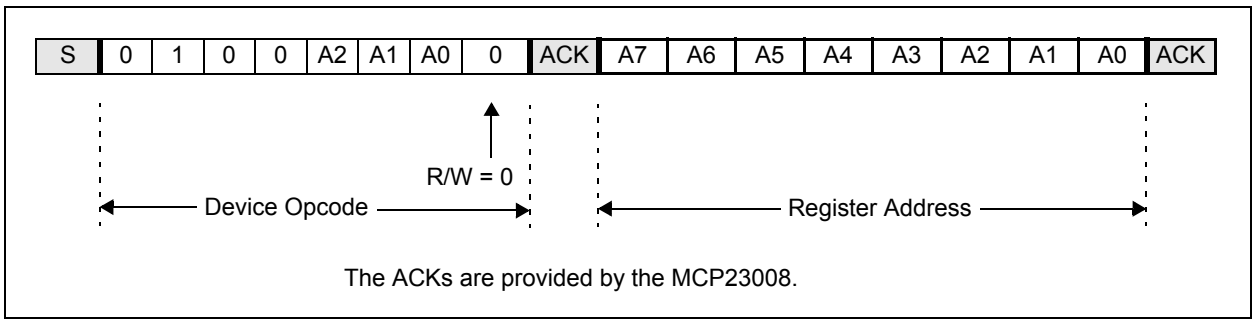
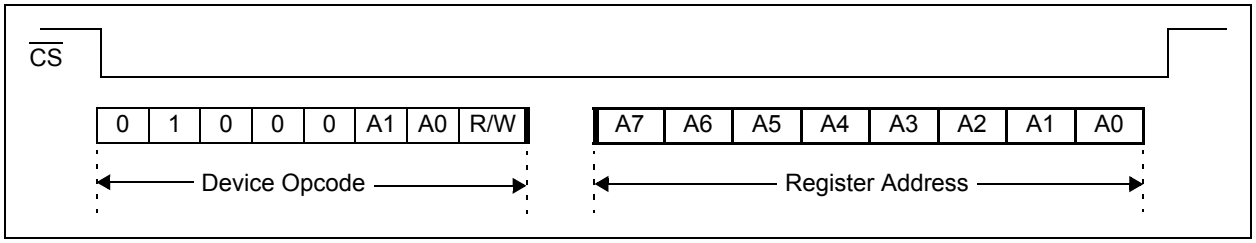


FIGURE 1-5: SPI ADDRESSING REGISTERS



1.5 GPIO Port

The GPIO module contains the data port (GPIO), internal pull up resistors and the Output Latches (OLAT).

Reading the GPIO register reads the value on the port. Reading the OLAT register only reads the OLAT, not the actual value on the port.

Writing to the GPIO register actually causes a write to the OLAT. Writing to the OLAT register forces the associated output drivers to drive to the level in OLAT. Pins configured as inputs turn off the associated output driver and put it in high-impedance.

1.6 Configuration and Control Registers

The Configuration and Control blocks contain the registers as shown in Table 1-3.

TABLE 1-3: CONFIGURATION AND CONTROL REGISTERS

Register Name	Address (hex)	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	POR/RST value
IODIR	00	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	1111 1111
IPOL	01	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	0000 0000
GPINTEN	02	GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0	0000 0000
DEFVAL	03	DEF7	DEF6	DEF5	DEF4	DEF3	DEF2	DEF1	DEF0	0000 0000
INTCON	04	IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	0000 0000
IOCON	05	—	—	SREAD	DISSLW	HAEN*	ODR	INTPOL	—	--00 000-
GPPU	06	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0000 0000
INTF	07	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INTO	0000 0000
INTCAP	08	ICP7	ICP6	ICP5	ICP4	ICP3	ICP2	ICP1	ICP0	0000 0000
GPIO	09	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000
OLAT	0A	OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0	0000 0000

* Not used on the MCP23008.

1.6.1 I/O DIRECTION (IODIR) REGISTER

Controls the direction of the data I/O.

When a bit is set, the corresponding pin becomes an input. When a bit is clear, the corresponding pin becomes an output.

REGISTER 1-1: IODIR – I/O DIRECTION REGISTER (ADDR 0x00)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **IO7:IO0:** These bits control the direction of data I/O <7:0>

1 = Pin is configured as an input.

0 = Pin is configured as an output.

1.6.2 INPUT POLARITY (IPOL) REGISTER

The IPOL register allows the user to configure the polarity on the corresponding GPIO port bits.

If a bit is set, the corresponding GPIO register bit will reflect the inverted value on the pin.

REGISTER 1-2: IPOL – INPUT POLARITY PORT REGISTER (ADDR 0x01)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **IP7:IP0:** These bits control the polarity inversion of the input pins <7:0>

1 = GPIO register bit will reflect the opposite logic state of the input pin.

0 = GPIO register bit will reflect the same logic state of the input pin.

1.6.3 INTERRUPT-ON-CHANGE CONTROL (GPINTEN) REGISTER

The GPINTEN register controls the interrupt-on-change feature for each pin.

If a bit is set, the corresponding pin is enabled for interrupt-on-change. The DEFVAL and INTCON registers must also be configured if any pins are enabled for interrupt-on-change.

REGISTER 1-3: GPINTEN – INTERRUPT-ON-CHANGE PINS (ADDR 0x02)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **GPINT7:GPINT0:** General purpose I/O interrupt-on-change bits <7:0>

1 = Enable GPIO input pin for interrupt-on-change event.
0 = Disable GPIO input pin for interrupt-on-change event.

Refer to INTCON and GPINTEN.

1.6.4 DEFAULT COMPARE (DEFVAL) REGISTER FOR INTERRUPT-ON-CHANGE

The default comparison value is configured in the DEFVAL register. If enabled (via GPINTEN and INTCON) to compare against the DEFVAL register, an opposite value on the associated pin will cause an interrupt to occur.

REGISTER 1-4: DEFVAL – DEFAULT VALUE REGISTER (ADDR 0x03)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DEF7	DEF6	DEF5	DEF4	DEF3	DEF2	DEF1	DEF0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **DEF7:DEF0:** These bits set the compare value for pins configured for interrupt-on-change from defaults <7:0>. Refer to INTCON.
If the associated pin level is the opposite from the register bit, an interrupt occurs.

Refer to INTCON and GPINTEN.

1.6.5 INTERRUPT CONTROL (INTCON) REGISTER

The INTCON register controls how the associated pin value is compared for the interrupt-on-change feature. If a bit is set, the corresponding I/O pin is compared against the associated bit in the DEFVAL register. If a bit value is clear, the corresponding I/O pin is compared against the previous value.

REGISTER 1-5: INTCON – INTERRUPT-ON-CHANGE CONTROL REGISTER (ADDR 0x04)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **IOC7:IOC0:** These bits control how the associated pin value is compared for interrupt-on-change <7:0>

1 = Controls how the associated pin value is compared for interrupt-on-change.
0 = Pin value is compared against the previous pin value.

Refer to INTCON and GPINTEN.

1.6.6 CONFIGURATION (IOCON) REGISTER

The IOCON register contains several bits for configuring the device:

- The Sequential Operation (SEQOP) controls the incrementing function of the address pointer. If the address pointer is disabled, the address pointer does not automatically increment after each byte is clocked during a serial transfer. This feature is useful when it is desired to continuously poll (read) or modify (write) a register.
- The Slew Rate (DISSLW) bit controls the slew rate function on the SDA pin. If enabled, the SDA slew rate will be controlled when driving from a high to a low.
- The Hardware Address Enable (HAEN) control bit enables/disables the hardware address pins (A1, A0) on the MCP23S08. This bit is not used on the MCP23008. The address pins are always enabled on the MCP23008.
- The Open-Drain (ODR) control bit enables/ disables the INT pin for open-drain configuration.
- The Interrupt Polarity (INTPOL) control bit sets the polarity of the INT pin. This bit is functional only when the ODR bit is cleared, configuring the INT pin as active push-pull.

REGISTER 1-6: IOCON – I/O EXPANDER CONFIGURATION REGISTER (ADDR 0x05)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
—	—	SEQOP	DISSLW	HAEN	ODR	INTPOL	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’.

bit 5 **SEQOP:** Sequential Operation mode bit.
1 = Sequential operation disabled, address pointer does not increment.
0 = Sequential operation enabled, address pointer increments.

bit 4 **DISSLW:** Slew Rate control bit for SDA output.
1 = Slew rate disabled.
0 = Slew rate enabled.

bit 3 **HAEN:** Hardware Address Enable bit (MCP23S08 only).
Address pins are always enabled on MCP23008.
1 = Enables the MCP23S08 address pins.
0 = Disables the MCP23S08 address pins.

bit 2 **ODR:** This bit configures the INT pin as an open-drain output.
1 = Open-drain output (overrides the INTPOL bit).
0 = Active driver output (INTPOL bit sets the polarity).

bit 1 **INTPOL:** This bit sets the polarity of the INT output pin.
1 = Active-high.
0 = Active-low.

bit 0 **Unimplemented:** Read as ‘0’.

1.6.7 PULL-UP RESISTOR CONFIGURATION (GPPU) REGISTER

The GPPU register controls the pull-up resistors for the port pins. If a bit is set and the corresponding pin is configured as an input, the corresponding port pin is internally pulled up with a 100 kΩ resistor.

REGISTER 1-7: GPPU – GPIO PULL-UP RESISTOR REGISTER (ADDR 0x06)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PU7:PU0:** These bits control the weak pull-up resistors on each pin (when configured as an input) <7:0>.

1 = Pull-up enabled.
0 = Pull-up disabled.

1.6.8 INTERRUPT FLAG (INTF) REGISTER

The INTF register reflects the interrupt condition on the port pins of any pin that is enabled for interrupts via the GPINTEN register. A 'set' bit indicates that the associated pin caused the interrupt.

This register is 'read-only'. Writes to this register will be ignored.

Note:	INTF will always reflect the pin(s) that have an interrupt condition. For example, one pin causes an interrupt to occur and is captured in INTCAP and INF. If before clearing the interrupt another pin changes, which would normally cause an interrupt, it will be reflected in INTF, but not INTCAP.

REGISTER 1-8: INTF – INTERRUPT FLAG REGISTER (ADDR 0x07)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **INT7:INT0:** These bits reflect the interrupt condition on the port. Will reflect the change only if interrupts are enabled (GPINTEN) <7:0>.

1 = Pin caused interrupt.

0 = Interrupt not pending.

1.6.9 INTERRUPT CAPTURE (INTCAP) REGISTER

The INTCAP register captures the GPIO port value at the time the interrupt occurred. The register is 'read-only' and is updated only when an interrupt occurs. The register will remain unchanged until the interrupt is cleared via a read of INTCAP or GPIO.

REGISTER 1-9: INTCAP – INTERRUPT CAPTURED VALUE FOR PORT REGISTER (ADDR 0x08)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ICP7	ICP6	ICP5	ICP4	ICP3	ICP2	ICP1	ICP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ICP7:ICP0:** These bits reflect the logic level on the port pins at the time of interrupt due to pin change <7:0>

1 = Logic-high.
0 = Logic-low.

1.6.10 PORT (GPIO) REGISTER

The GPIO register reflects the value on the port. Reading from this register reads the port. Writing to this register modifies the Output Latch (OLAT) register.

REGISTER 1-10: GPIO – GENERAL PURPOSE I/O PORT REGISTER (ADDR 0x09)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **GP7:GP0:** These bits reflect the logic level on the pins <7:0>

1 = Logic-high.

0 = Logic-low.

1.6.11 OUTPUT LATCH REGISTER (OLAT)

The OLAT register provides access to the output latches. A read from this register results in a read of the OLAT and not the port itself. A write to this register modifies the output latches that modify the pins configured as outputs.

REGISTER 1-11: OLAT – OUTPUT LATCH REGISTER 0 (ADDR 0x0A)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **OL7:OL0:** These bits reflect the logic level on the output latch <7:0>

1 = Logic-high.
0 = Logic-low.

1.7 Interrupt Logic

The interrupt output pin will activate if an internal interrupt occurs. The interrupt block is configured by the following registers:

- GPINTEN – enables the individual inputs
- DEFVAL – holds the values that are compared against the associated input port values
- INTCON – controls if the input values are compared against DEFVAL or the previous values on the port
- IOCON (ODR and INPOL) – configures the INT pin as push-pull, open-drain and active-level

Only pins configured as inputs can cause interrupts. Pins configured as outputs have no affect on INT.

Interrupt activity on the port will cause the port value to be captured and copied into INTCAP. The interrupt will remain active until the INTCAP or GPIO register is read. Writing to these registers will not affect the interrupt.

The first interrupt event will cause the port contents to be copied into the INTCAP register. Subsequent interrupt conditions on the port will not cause an interrupt to occur as long as the interrupt is not cleared by a read of INTCAP or GPIO.

1.7.1 INTERRUPT CONDITIONS

There are two possible configurations to cause interrupts (configured via INTCON):

1. Pins configured for **interrupt-on-pin-change** will cause an interrupt to occur if a pin changes to the opposite state. The default state is reset after an interrupt occurs. For example, an interrupt occurs by an input changing from `1` to `0`. The new initial state for the pin is a logic `0`.
2. Pins configured for **interrupt-on-change from register value** will cause an interrupt to occur if the corresponding input pin differs from the register bit. The interrupt condition will remain as long as the condition exists, regardless if the INTAP or GPIO is read.

See Figure 1-6 and Figure 1-7 for more information on interrupt operations.

FIGURE 1-6: INTERRUPT-ON-PIN-CHANGE

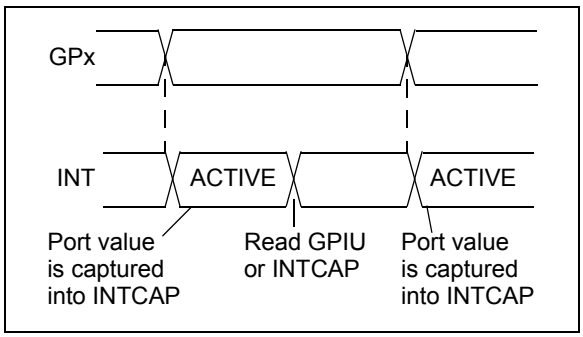
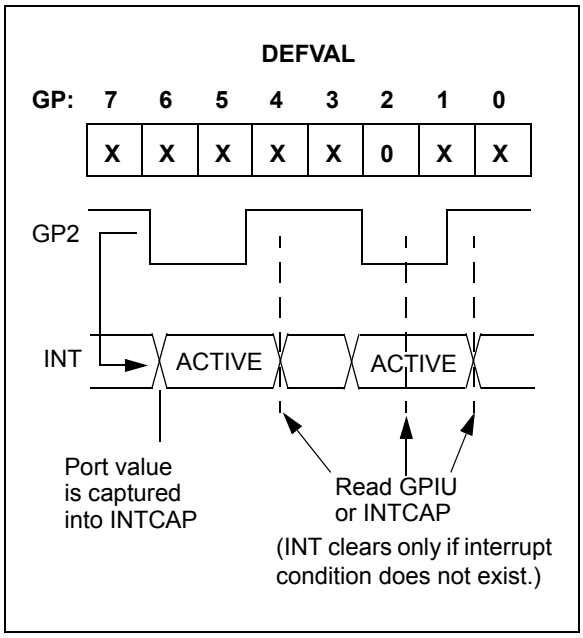


FIGURE 1-7: INTERRUPT-ON-CHANGE FROM REGISTER DEFAULT



NOTES:

2.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +5.5V
Voltage on all other pins with respect to V_{SS} (except V_{DD}) ..... -0.6V to (V_{DD} + 0.6V)
Total power dissipation (**Note**) ..... 700 mW
Maximum current out of V_{SS} pin ..... 150 mA
Maximum current into V_{DD} pin ..... 125 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Maximum output current sunk by any output pin ..... 25 mA
Maximum output current sourced by any output pin ..... 25 mA

Note: Power dissipation is calculated as follows:
$P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2.1 DC Characteristics

DC Characteristics		Operating Conditions (unless otherwise indicated): 1.8V ≤ V_{DD} ≤ 5.5V at -40°C ≤ T_A ≤ +85°C (I-Temp) 4.5V ≤ V_{DD} ≤ 5.5V at -40°C ≤ T_A ≤ +125°C (E-Temp) **(Note 1)**					
Param No.	**Characteristic**	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	V_{DD}	1.8	—	5.5	V	
D002	V_{DD} Start Voltage to Ensure Power-on Reset	V_{POR}	—	V_{SS}	—	V	
D003	V_{DD} Rise Rate to Ensure Power-on Reset	SV_{DD}	0.05	—	—	V/ms	Design guidance only. Not tested.
D004	Supply Current	I_{DD}	—	—	1	mA	SCL/SCK = 1 MHz
D005	Standby current	I_{DDS}	—	—	1	µA	
			—	—	2	µA	4.5V - 5.5V @ +125°C **(Note 1)**
	Input Low-Voltage						
D030	A0, A1 (TTL buffer)	V_{IL}	V_{SS}	—	0.15 V_{DD}	V	
D031	$\overline{CS}$, GPIO, SCL/SCK, SDA, A2, $\overline{RESET}$ (Schmitt Trigger)		V_{SS}	—	0.2 V_{DD}	V	
	Input High-Voltage						
D040	A0, A1 (TTL buffer)	V_{IH}	0.25 V_{DD} + 0.8	—	V_{DD}	V	
D041	$\overline{CS}$, GPIO, SCL/SCK, SDA, A2, $\overline{RESET}$ (Schmitt Trigger)		0.8 V_{DD}	—	V_{DD}	V	For entire V_{DD} range.
	Input Leakage Current						
D060	I/O port pins	I_{IL}	—	—	±1	µA	V_{SS} ≤ V_{PIN} ≤ V_{DD}
	Output Leakage Current						
D065	I/O port pins	I_{LO}	—	—	±1	µA	V_{SS} ≤ V_{PIN} ≤ V_{DD}
D070	GPIO weak pull-up current	I_{PU}	40	75	115	µA	V_{DD} = 5V, GP Pins = V_{SS} –40°C ≤ T_A ≤ +85°C
	Output Low-Voltage						
D080	GPIO	V_{OL}	—	—	0.6	V	I_{OL} = 8.5 mA, V_{DD} = 4.5V
	INT		—	—	0.6	V	I_{OL} = 1.6 mA, V_{DD} = 4.5V
	SO, SDA		—	—	0.6	V	I_{OL} = 3.0 mA, V_{DD} = 1.8V
	SDA		—	—	0.8	V	I_{OL} = 3.0 mA, V_{DD} = 4.5V
	Output High-Voltage						
D090	GPIO, INT, SO	V_{OH}	V_{DD} – 0.7	—	—	V	I_{OH} = -3.0 mA, V_{DD} = 4.5V
			V_{DD} – 0.7	—	—		I_{OH} = -400 µA, V_{DD} = 1.8V
	Capacitive Loading Specs on Output Pins						
D101	GPIO, SO, INT	C_{IO}	—	—	50	pF	
D102	SDA	C_B	—	—	400	pF	

Note 1: This parameter is characterized, not 100% tested.

FIGURE 2-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

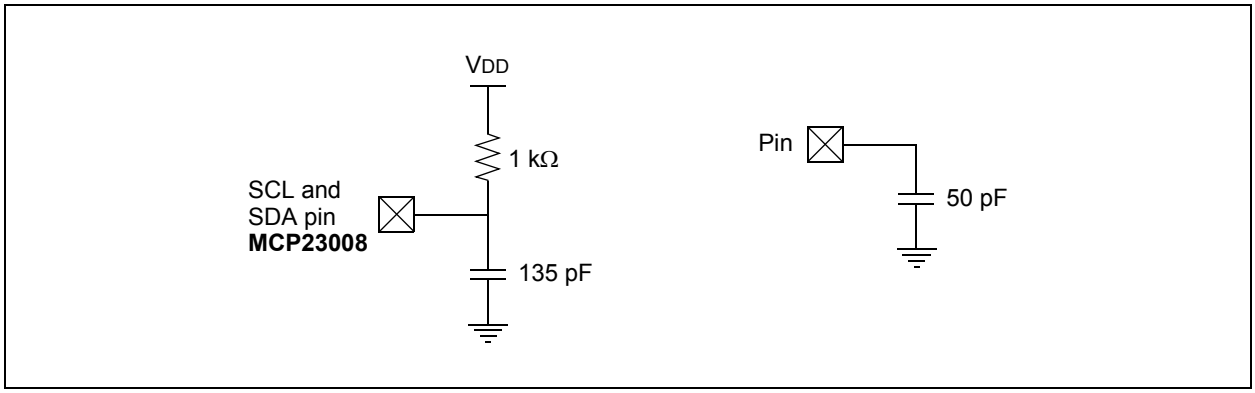


FIGURE 2-2: RESET AND DEVICE RESET TIMER TIMING

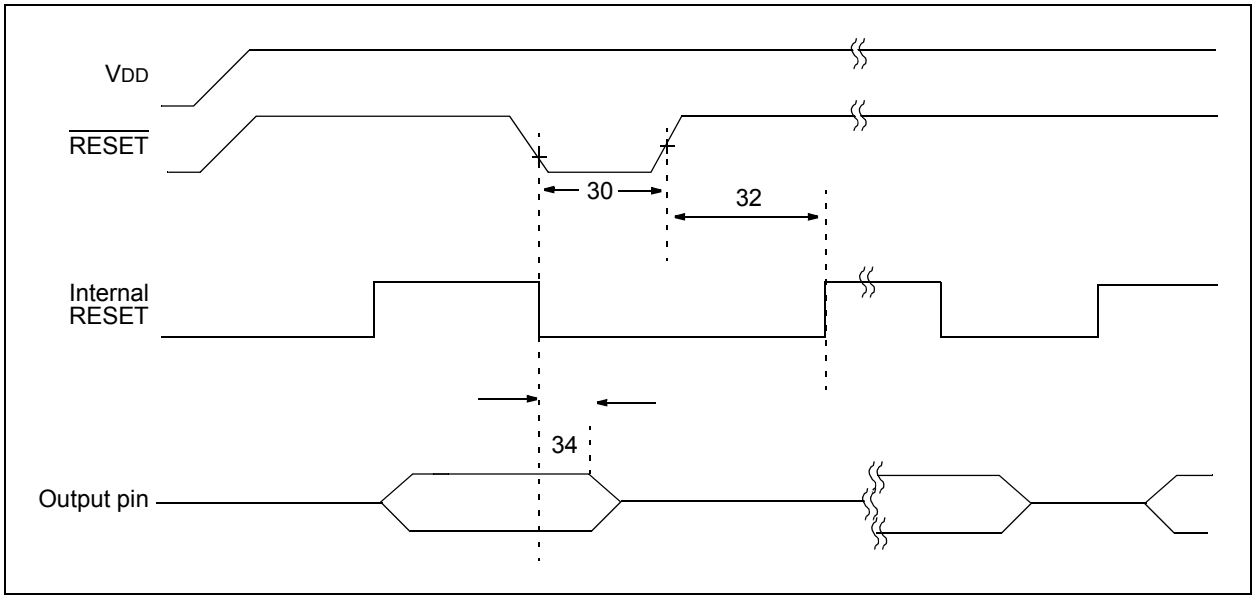


TABLE 2-1: DEVICE RESET SPECIFICATIONS

AC Characteristics		Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) **(Note 1)**					
Param No.	**Characteristic**	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
30	$\overline{\text{RESET}}$ Pulse Width (Low)	TRSTL	1	—	—	µs	
32	Device Active After $\overline{\text{RESET}}$ high	THLD	—	0	—	µs	VDD = 5.0V
34	Output High-Impedance From $\overline{\text{RESET}}$ Low	TIOZ	—	—	1	µs	

Note 1: This parameter is characterized, not 100% tested.

FIGURE 2-3: I²C™ BUS START/STOP BITS TIMING

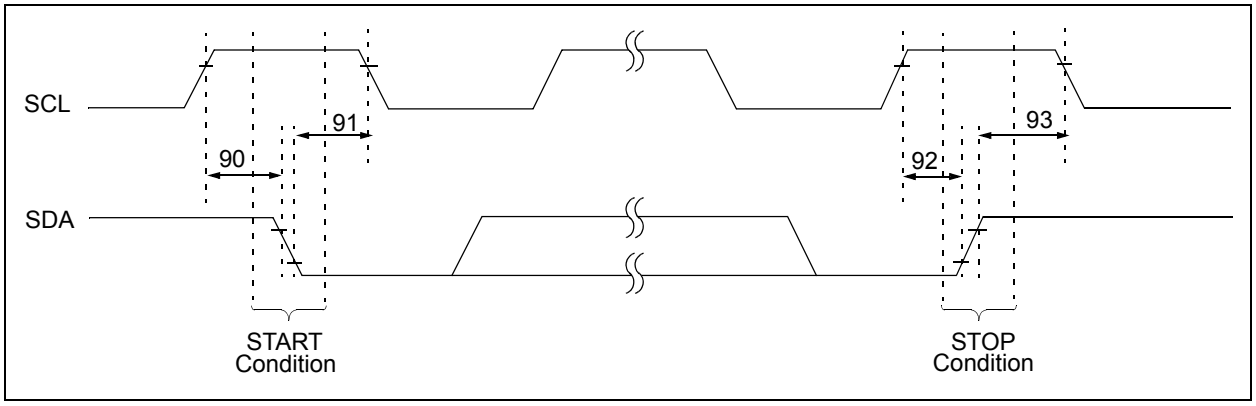


FIGURE 2-4: I²C™ BUS DATA TIMING

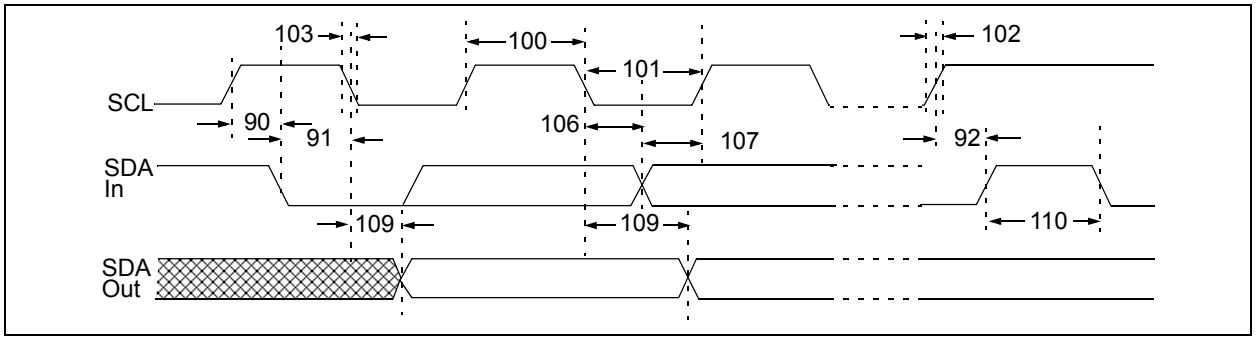


TABLE 2-2: I²C™ BUS DATA REQUIREMENTS

I²C™ AC Characteristics		Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) **(Note 1)** RPU (SCL, SDA) = 1 kΩ, CL (SCL, SDA) = 135 pF					
Param No.	**Characteristic**	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
100	Clock High Time:	THIGH					
	100 kHz mode		4.0	—	—	µs	1.8V – 5.5V (I-Temp)
	400 kHz mode		0.6	—	—	µs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		0.12	—	—	µs	4.5V – 5.5V (E-Temp)
101	Clock Low Time:	TLOW					
	100 kHz mode		4.7	—	—	µs	1.8V – 5.5V (I-Temp)
	400 kHz mode		1.3	—	—	µs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		0.32	—	—	µs	4.5V – 5.5V (E-Temp)
102	SDA and SCL Rise Time:	TR **(Note 1)**					
	100 kHz mode		—	—	1000	ns	1.8V – 5.5V (I-Temp)
	400 kHz mode		20 + 0.1 CB **(2)**	—	300	ns	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		20	—	160	ns	4.5V – 5.5V (E-Temp)
103	SDA and SCL Fall Time:	TF **(Note 1)**					
	100 kHz mode		—	—	300	ns	1.8V – 5.5V (I-Temp)
	400 kHz mode		20 + 0.1 CB **(2)**	—	300	ns	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		20	—	80	ns	4.5V – 5.5V (E-Temp)
90	START Condition Setup Time:	TSU:STA					
	100 kHz mode		4.7	—	—	µs	1.8V – 5.5V (I-Temp)
	400 kHz mode		0.6	—	—	µs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		0.16	—	—	µs	4.5V – 5.5V (E-Temp)
91	START Condition Hold Time:	THD:STA					
	100 kHz mode		4.0	—	—	µs	1.8V – 5.5V (I-Temp)
	400 kHz mode		0.6	—	—	µs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		0.16	—	—	µs	4.5V – 5.5V (E-Temp)
106	Data Input Hold Time:	THD:DAT					
	100 kHz mode		0	—	3.45	µs	1.8V – 5.5V (I-Temp)
	400 kHz mode		0	—	0.9	µs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		0	—	0.15	µs	4.5V – 5.5V (E-Temp)
107	Data Input Setup Time:	TSU:DAT					
	100 kHz mode		250	—	—	ns	1.8V – 5.5V (I-Temp)
	400 kHz mode		100	—	—	ns	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		0.01	—	—	µs	4.5V – 5.5V (E-Temp)
92	STOP Condition Setup Time:	TSU:STO					
	100 kHz mode		4.0	—	—	µs	1.8V – 5.5V (I-Temp)
	400 kHz mode		0.6	—	—	µs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		0.16	—	—	µs	4.5V – 5.5V (E-Temp)

Note 1: This parameter is characterized, not 100% tested.

2: CB is specified to be from 10 to 400 pF.

TABLE 2-2: I²C™ BUS DATA REQUIREMENTS (CONTINUED)

I²C™ AC Characteristics		Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) **(Note 1)** RPU (SCL, SDA) = 1 kΩ, CL (SCL, SDA) = 135 pF					
Param No.	**Characteristic**	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
109	Output Valid From Clock:	TAA					
	100 kHz mode		—	—	3.45	µs	1.8V – 5.5V (I-Temp)
	400 kHz mode		—	—	0.9	µs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		—	—	0.18	µs	4.5V – 5.5V (E-Temp)
110	Bus Free Time:	TBUF					
	100 kHz mode		4.7	—	—	µs	1.8V – 5.5V (I-Temp)
	400 kHz mode		1.3	—	—	µs	2.7V – 5.5V (I-Temp)
	1.7 MHz mode		N/A	—	N/A	µs	4.5V – 5.5V (E-Temp)
	Bus Capacitive Loading:	CB					
	100 kHz and 400 kHz		—	—	400	pF	**(Note 1)**
	1.7 MHz		—	—	100	pF	**(Note 1)**
	Input Filter Spike Suppression: (SDA and SCL)	TSP					
	100 kHz and 400 kHz		—	—	50	ns	
	1.7 MHz		—	—	10	ns	Spike suppression off

Note 1: This parameter is characterized, not 100% tested.

2: CB is specified to be from 10 to 400 pF.

FIGURE 2-5: SPI INPUT TIMING

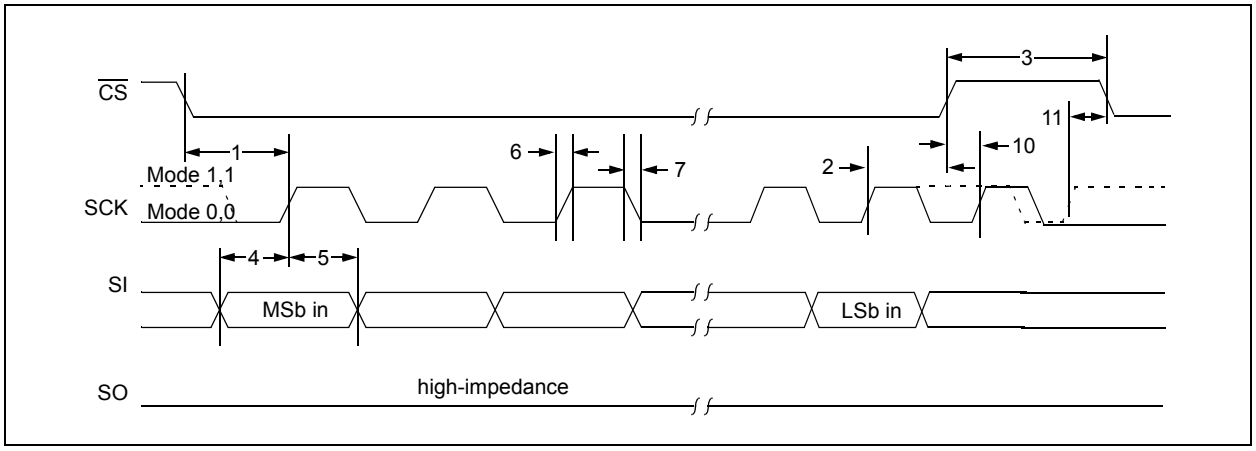


FIGURE 2-6: SPI OUTPUT TIMING

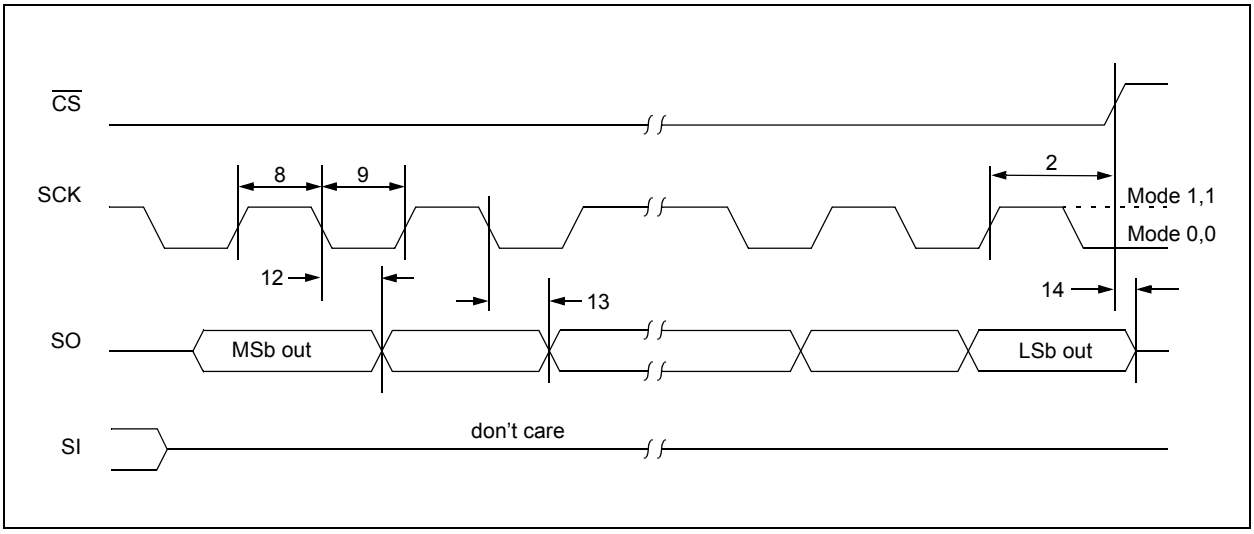


TABLE 2-3: SPI INTERFACE AC CHARACTERISTICS

SPI Interface AC Characteristics		Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) **(Note 1)**					
Param No.	**Characteristic**	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
	Clock Frequency	FCLK	—	—	5	MHz	1.8V – 5.5V (I-Temp)
			—	—	10	MHz	2.7V – 5.5V (I-Temp)
			—	—	10	MHz	4.5V – 5.5V (E-Temp)
1	$\overline{CS}$ Setup Time	TCSS	50	—	—	ns	
2	$\overline{CS}$ Hold Time	TCSH	100	—	—	ns	1.8V – 5.5V (I-Temp)
			50	—	—	ns	2.7V – 5.5V (I-Temp)
			50	—	—	ns	4.5V – 5.5V (E-Temp)
3	$\overline{CS}$ Disable Time	TCSD	100	—	—	ns	1.8V – 5.5V (I-Temp)
			50	—	—	ns	2.7V – 5.5V (I-Temp)
			50	—	—	ns	4.5V – 5.5V (E-Temp)
4	Data Setup Time	TSU	20	—	—	ns	1.8V – 5.5V (I-Temp)
			10	—	—	ns	2.7V – 5.5V (I-Temp)
			10	—	—	ns	4.5V – 5.5V (E-Temp)
5	Data Hold Time	THD	20	—	—	ns	1.8V – 5.5V (I-Temp)
			10	—	—	ns	2.7V – 5.5V (I-Temp)
			10	—	—	ns	4.5V – 5.5V (E-Temp)
6	CLK Rise Time	TR	—	—	2	µs	**Note 1**
7	CLK Fall Time	TF	—	—	2	µs	**Note 1**
8	Clock High Time	THI	90	—	—	ns	1.8V – 5.5V (I-Temp)
			45	—	—	ns	2.7V – 5.5V (I-Temp)
			45	—	—	ns	4.5V – 5.5V (E-Temp)

Note 1: This parameter is characterized, not 100% tested.

2: TV = 90 ns (max) when address pointer rolls over from address 0x0A to 0x00.

TABLE 2-3: SPI INTERFACE AC CHARACTERISTICS (CONTINUED)

SPI Interface AC Characteristics		Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +85°C (I-Temp) 4.5V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C (E-Temp) **(Note 1)**					
Param No.	**Characteristic**	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
9	Clock Low Time	TLO	90	—	—	ns	1.8V – 5.5V (I-Temp)
			45	—	—	ns	2.7V – 5.5V (I-Temp)
			45	—	—	ns	4.5V – 5.5V (E-Temp)
10	Clock Delay Time	TCLD	50	—	—	ns	
11	Clock Enable Time	TCLE	50	—	—	ns	
12(2)	Output Valid from Clock Low	TV	—	—	90	ns	1.8V – 5.5V (I-Temp)
			—	—	45	ns	2.7V – 5.5V (I-Temp)
			—	—	45	ns	4.5V – 5.5V (E-Temp)
13	Output Hold Time	THO	0	—	—	ns	
14	Output Disable Time	TDIS	—	—	100	ns	

Note 1: This parameter is characterized, not 100% tested.

2: TV = 90 ns (max) when address pointer rolls over from address 0x0A to 0x00.

FIGURE 2-7: GPIO AND INT TIMING

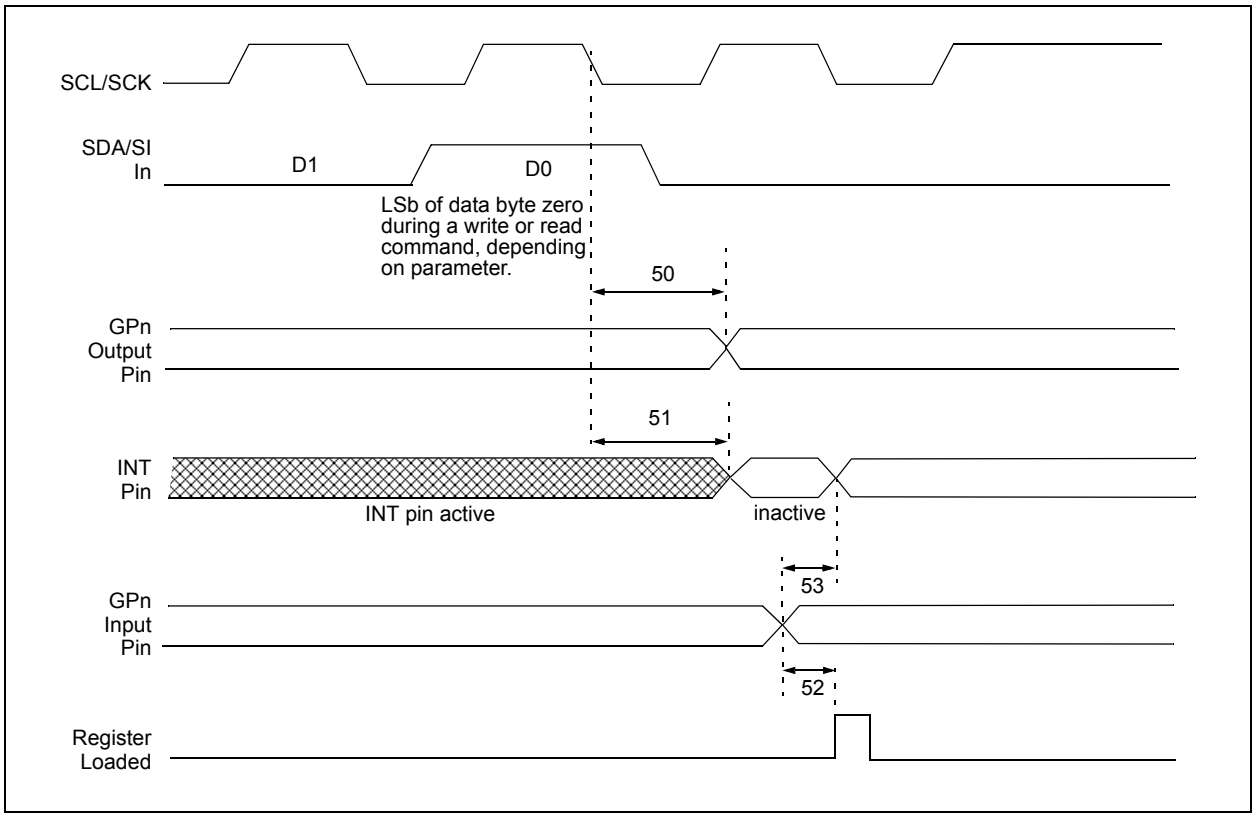


TABLE 2-4: GP AND INT PINS

AC Characteristics		Operating Conditions (unless otherwise indicated): 1.8V ≤ V_{DD} ≤ 5.5V at -40°C ≤ T_A ≤ +85°C (I-Temp) 4.5V ≤ V_{DD} ≤ 5.5V at -40°C ≤ T_A ≤ +125°C (E-Temp) **(Note 1)**					
Param No.	**Characteristic**	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
50	Serial data to output valid	T_{GPOV}	—	—	500	ns	
51	Interrupt pin disable time	T_{INTD}	—	—	600	ns	
52	GP input change to register valid	T_{GPIV}	—	—	450	ns	
53	IOC event to INT active	T_{GPINT}	—	—	600	ns	
	Glitch Filter on GP Pins	T_{GLITCH}	—	—	150	ns	

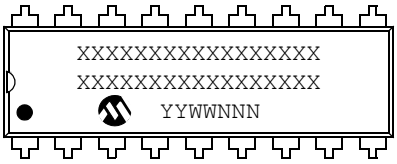
Note 1: This parameter is characterized, not 100% tested

NOTES:

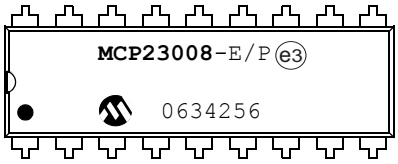
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

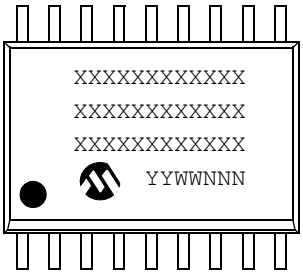
18-Lead PDIP (300 mil)



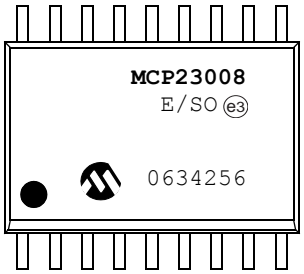
Example:



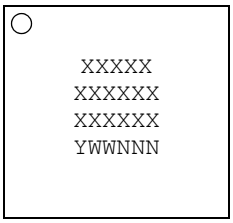
18-Lead SOIC (300 mil)



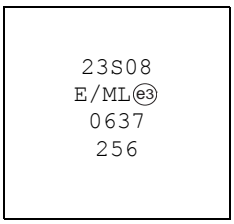
Example:



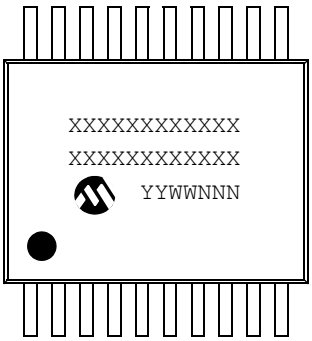
20-Lead QFN



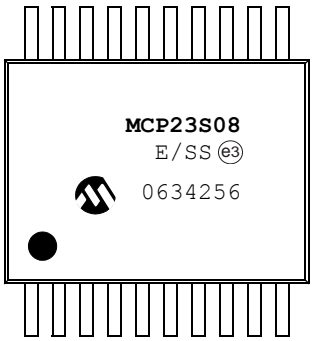
Example



20-Lead SSOP



Example:

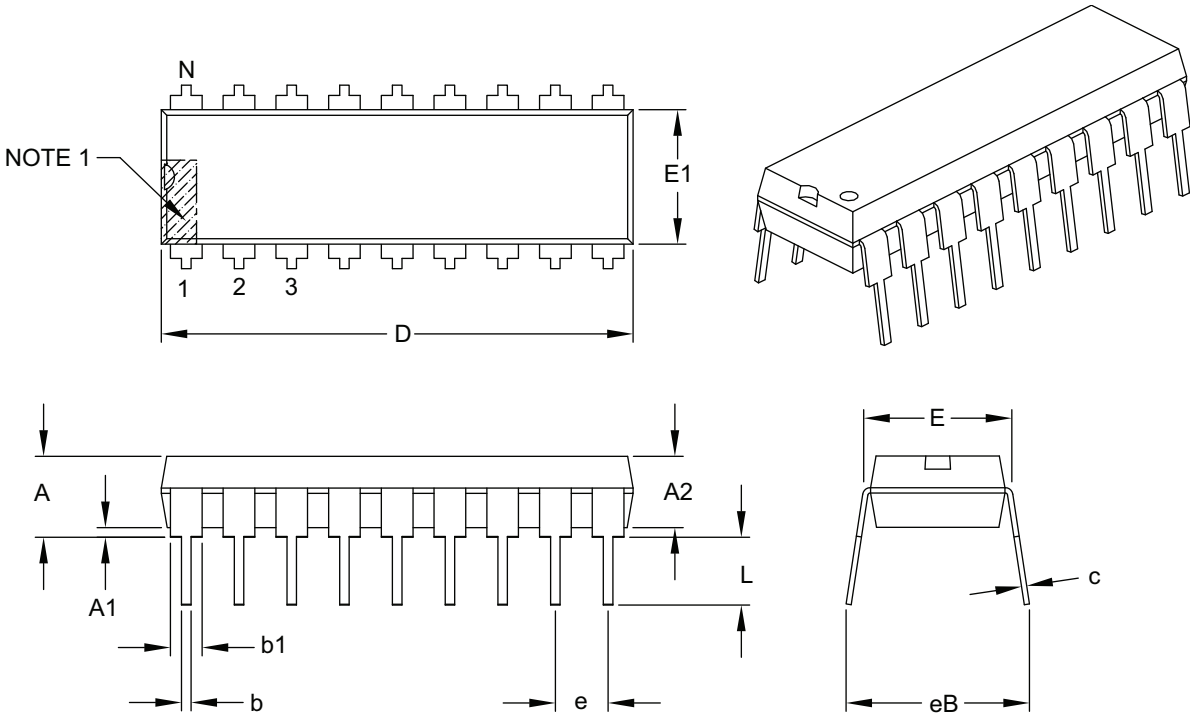


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

18-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		18	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.300	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.880	.900	.920
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.014
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

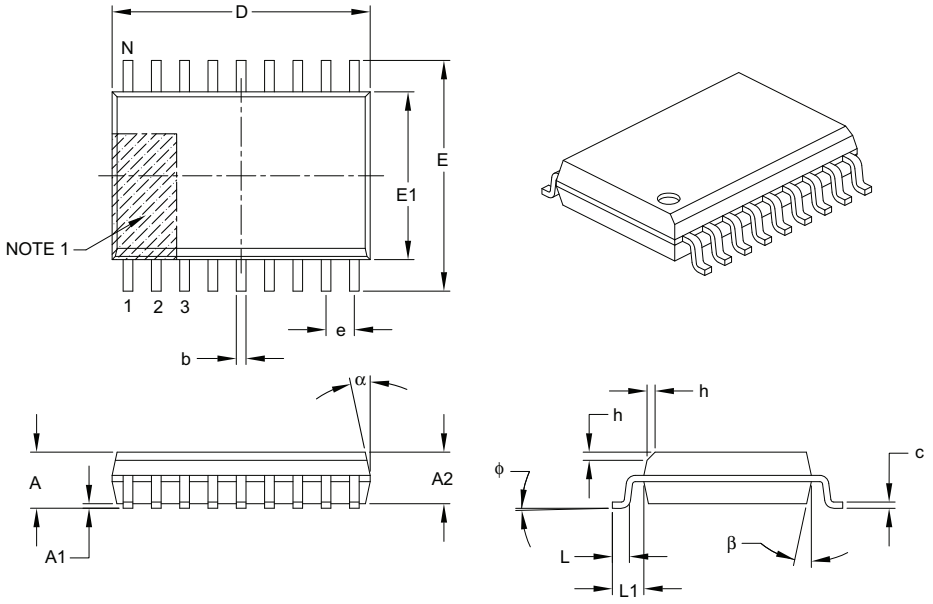
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-007B

18-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		18	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	2.65
Molded Package Thickness	A2	2.05	–	–
Standoff §	A1	0.10	–	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		11.55 BSC	
Chamfer (optional)	h	0.25	–	0.75
Foot Length	L	0.40	–	1.27
Footprint	L1		1.40 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.20	–	0.33
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

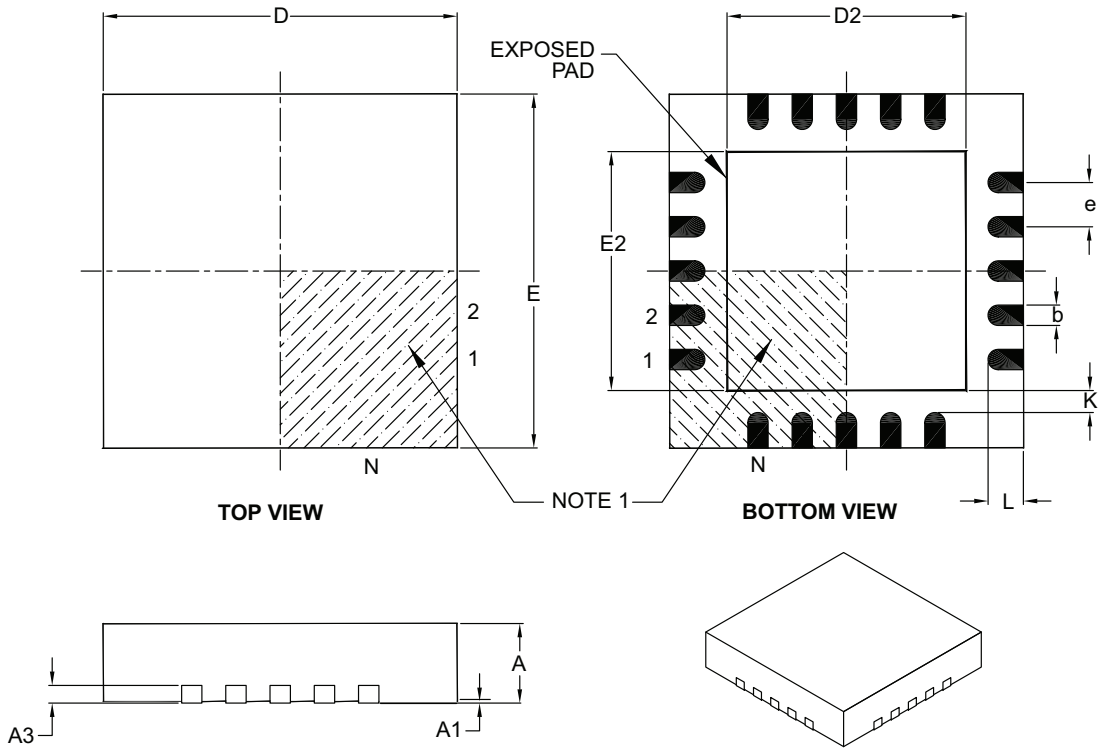
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-051B

20-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

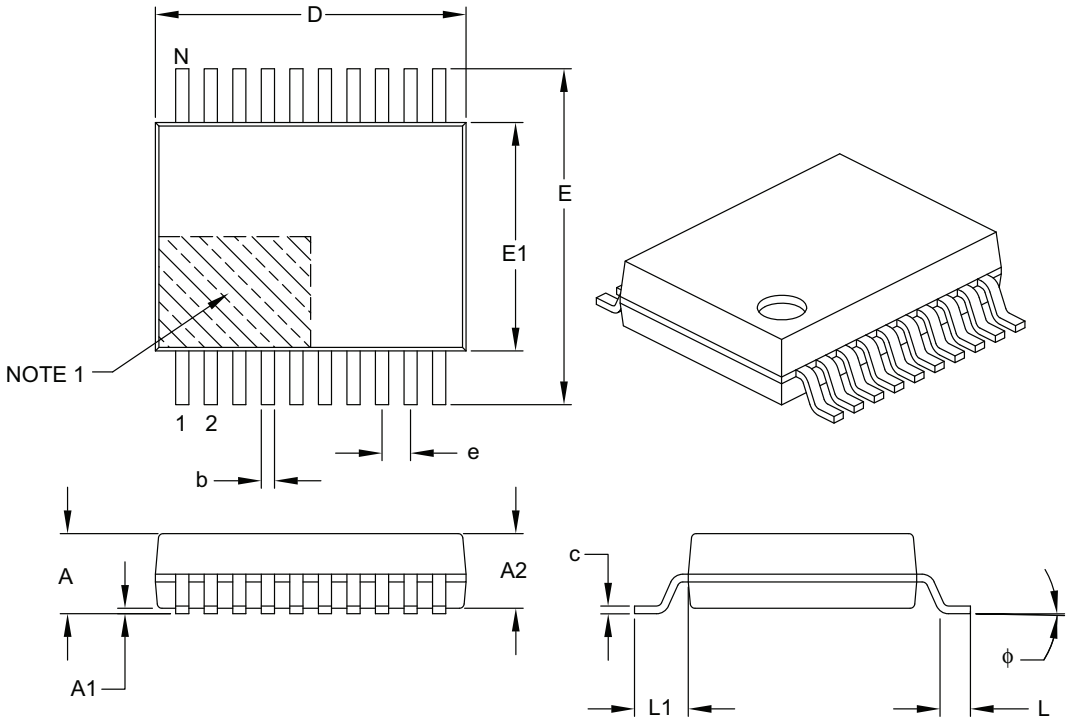
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-126B

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

NOTES:

APPENDIX A: REVISION HISTORY

Revision E (August 2007)

1. **Section 3.0 "Packaging Information"**: Updated package outline drawings.

Revision D (February 2007)

1. Changed Byte and Sequential Read in Figure 1-1 from "R" to "W".
2. Table 2-4, Param No. 51 and 53: Changed from 450 to 600 and 500 to 600, respecively.
3. Added disclaimer to package outline drawings.
4. Updated package outline drawings.

Revision C (October 2006)

1. Added 20-pin QFN package information throughout document.
2. Added disclaimer to package outline drawings.

Revision B (February 2005)

The following is the list of modifications:

1. **Section 1.6 "Configuration and Control Registers"**. Added Hardware Address Enable (HAEN) bit to Table 1-3.
2. **Section 1.6.6 "Configuration (IOCON) Register"**. Added Hardware Address Enable (HAEN) bit to Register 1-6.

Revision A (December 2004)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	−	X	/XX
Device		Temperature Range	Package

Device	MCP23008:	8-Bit I/O Expander w/ I²C™ Interface
	MCP23008T:	8-Bit I/O Expander w/ I²C Interface (Tape and Reel)
	MCP23S08:	8-Bit I/O Expander w/ SPI Interface
	MCP23S08T:	8-Bit I/O Expander w/ SPI Interface (Tape and Reel)
Temperature Range	E =	-40°C to +125°C (Extended) *
	* While these devices are only offered in the "E" temperature range, the device will operate at different voltages and temperatures as identified in the **Section 2.0 "Electrical Characteristics"**.	
Package	ML =	Plastic Quad Flat, No Lead Package 4x4x0.9 mm Body (QFN), 20-Lead
	P =	Plastic DIP (300 mil Body), 18-Lead
	SO =	Plastic SOIC (300 mil Body), 18-Lead
	SS =	SSOP, (209 mil Body, 5.30 mm), 20-Lead

Examples:

a)	MCP23008-E/P:	Extended Temp., 18LD PDIP package.
b)	MCP23008-E/SO:	Extended Temp., 18LD SOIC package.
c)	MCP23008T-E/SO:	Tape and Reel, Extended Temp., 18LD SOIC package.
d)	MCP23008-E/SS:	Extended Temp., 20LD SSOP package.
e)	MCP23008T-E/SS:	Tape and Reel, Extended Temp., 20LD SSOP package.
f)	MCP23008-E/ML:	Extended Temp., 20LD QFN package.
a)	MCP23S08-E/P:	Extended Temp., 18LD PDIP package.
b)	MCP23S08-E/SO:	Extended Temp., 18LD SOIC package.
c)	MCP23S08T-E/SO:	Tape and Reel, Extended Temp., 18LD SOIC package.
d)	MCP23S08-E/SS:	Extended Temp., 20LD SSOP package.
e)	MCP23S08T-E/SS:	Tape and Reel, Extended Temp., 20LD SSOP package.
f)	MCP23S08T-E/MF:	Tape and Reel, Extended Temp., 20LD QFN package.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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06/25/07

35W Single Output Switching Power Supply — PS-35 series

■ Features :

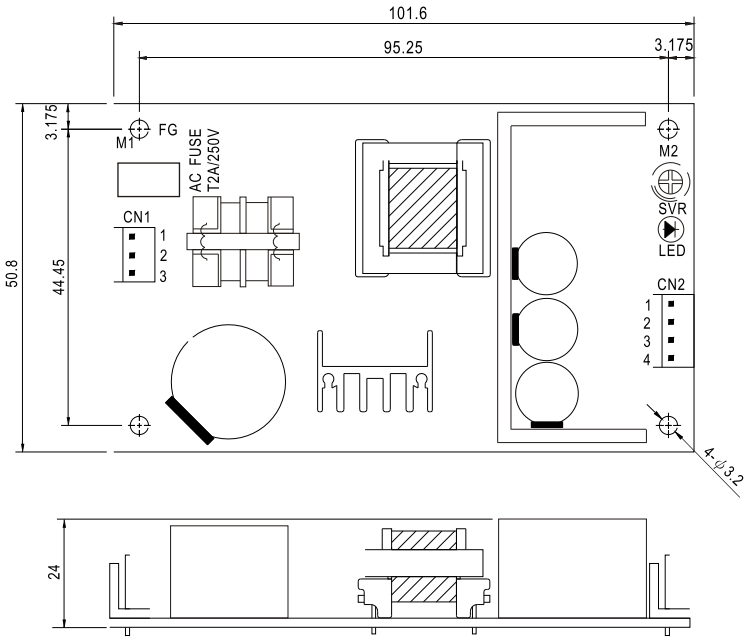
- Universal AC input/Full range
- Protections:Short circuit/Over load/Over voltage
- Cooling by free air convection
- 100% full load burn-in test
- Fixed switching frequency at 60KHz
- 2 years warranty

SPECIFICATION

MODEL		PS-35-3.3	PS-35-5	PS-35-7.5	PS-35-12	PS-35-13.5	PS-35-15	PS-35-24	PS-35-48
OUTPUT	DC VOLTAGE	3.3V	5V	7.5V	12V	13.5V	15V	24V	48V
	RATED CURRENT	6A	6A	4.7A	3A	2.6A	2.4A	1.5A	0.75A
	CURRENT RANGE	0 ~ 6A	0 ~ 6A	0 ~ 4.7A	0 ~ 3A	0 ~ 2.6A	0 ~ 2.4A	0 ~ 1.5A	0 ~ 0.75A
	RATED POWER	19.8W	30W	35.25W	36W	35.1W	36W	36W	36W
	RIPPLE & NOISE (max.) Note.2	80mVp-p	100mVp-p	100mVp-p	120mVp-p	120mVp-p	150mVp-p	200mVp-p	240mVp-p
	VOLTAGE ADJ. RANGE	3.14 ~ 3.63V	4.75 ~ 5.5V	7.13 ~ 8.25V	10.8 ~ 13.2V	12.15 ~ 14.85V	13.5 ~ 16.5V	21.6 ~ 26.4V	43.2 ~ 52.8V
	VOLTAGE TOLERANCE Note.3	±2.0%	±2.0%	±2.0%	±1.0%	±1.0%	±1.0%	±1.0%	±1.0%
	LINE REGULATION	±0.5%	±0.5%	±0.5%	±0.5%	±0.5%	±0.5%	±0.5%	±0.5%
	LOAD REGULATION	±1%	±1%	±1%	±0.5%	±0.5%	±0.5%	±0.5%	±0.5%
	SETUP, RISE TIME	1200ms, 30ms/230VAC,1200ms,30ms/115VAC at full load							
	HOLD TIME (Typ.)	50ms/230VAC,10ms/115VAC at full load							
INPUT	VOLTAGE RANGE	90 ~ 264VAC 127 ~370VDC							
	FREQUENCY RANGE	47 ~ 440Hz							
	EFFICIENCY(Typ.)	70%	78%	80%	81%	81%	81%	85%	84%
	AC CURRENT (Typ.)	0.75A/115VAC 0.5A/230VAC							
	INRUSH CURRENT (Typ.)	COLD START 23A/115VAC 45A/230VAC							
	LEAKAGE CURRENT	<2mA / 240VAC							
PROTECTION	OVER LOAD	105 ~ 150% rated output power (3.3V:105 ~ 160% rated output power)							
		Protection type : Hiccup mode, recovers automatically after fault condition is removed.							
	OVER VOLTAGE	3.8 ~ 4.95V	5.75 ~ 6.75V	8.63 ~ 10.5V	13.8 ~ 16.2V	15.5 ~ 18.2V	17.25 ~ 20.25V	27.6 ~ 32.4V	55.2 ~ 62.4V
		Protection type : shut down O/P voltage,re-power on to recover							
ENVIRONMENT	WORKING TEMP.	-20 ~ +65℃ (Refer to output load derating curve)							
	WORKING HUMIDITY	20 ~ 90% RH non-condensing							
	STORAGE TEMP., HUMIDITY	-20 ~ +85℃, 10 ~ 95% RH							
	TEMP. COEFFICIENT	±0.05%/℃ (0 ~ 50℃)							
	VIBRATION	10 ~ 500Hz, 2G 10min./1cycle, Period for 60min.each along X, Y, Z axes							
SAFETY & EMC (Note 4)	SAFETY STANDARDS	UL60950, TUV EN60950-1 Approved							
	WITHSTAND VOLTAGE	I/P-O/P:3KVAC I/P-FG:1.5KVAC O/P-FG:0.5KVAC							
	ISOLATION RESISTANCE	I/P-O/P, I/P-FG, O/P-FG:100M Ohms/500VDC							
	EMI CONDUCTION & RADIATION	Compliance to EN55022 (CISPR22) Class B							
	HARMONIC CURRENT	Compliance to EN61000-3-2,-3							
	EMS IMMUNITY	Compliance to EN61000-4-2,3,4,5,6,8,11; ENV50204, EN55024, Light industry level, criteria A							
OTHERS	MTBF	588.8Khrs							
	DIMENSION	101.6*50.8*24mm (L*W*H)							
	PACKING	0.124Kg;96PCS/12.9Kg/0.8CUFT							
NOTE	1. All parameters NOT specially mentioned are measured at 230VAC input, rated load and 25℃ of ambient temperature. 2. Ripple & noise are measured at 20MHz of bandwidth by using a 12" twisted pair-wire terminated with a 0.1uf & 47uf parallel capacitor. 3. Tolerance : includes set up tolerance, line regulation and load regulation. 4. The power supply is considered a component which will be installed into a final equipment. The final equipment must be re-confirmed that it still meets EMC directives.								

■ Mechanical Specification

Unit:mm



AC Input Connector (CN1) : JST B3P-VH-B or equivalent

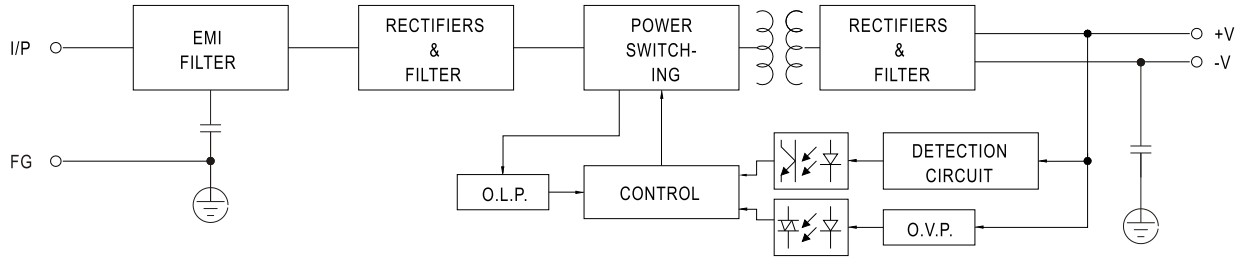
Pin No.	Assignment	Mating Housing	Terminal
1	AC/L	JST VHR or equivalent	JST SVH-21T-P1.1 or equivalent
3	AC/N		
2	NC		

DC Output Connector (CN2) : JST B4P-VH-B or equivalent

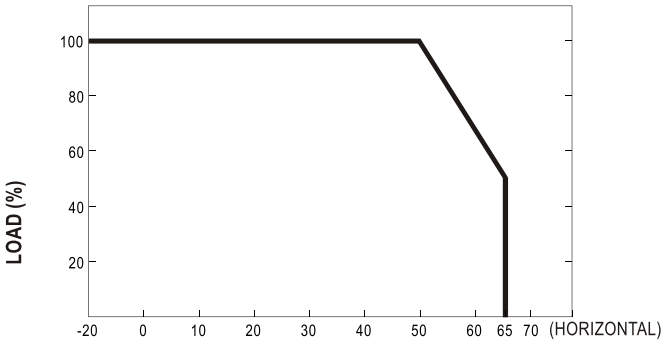
Pin No.	Assignment	Mating Housing	Terminal
1,2	+V	JST VHR or equivalent	JST SVH-21T-P1.1 or equivalent
3,4	-V		

■ Block Diagram

fosc : 60KHz

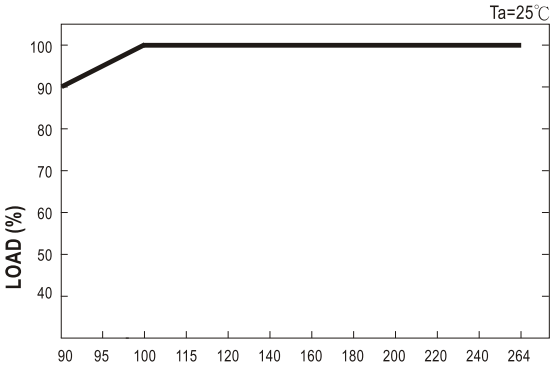


■ Derating Curve



AMBIENT TEMPERATURE (℃)

■ Output Derating VS Input Voltage



INPUT VOLTAGE (VAC) 60Hz

DC/DC Converters

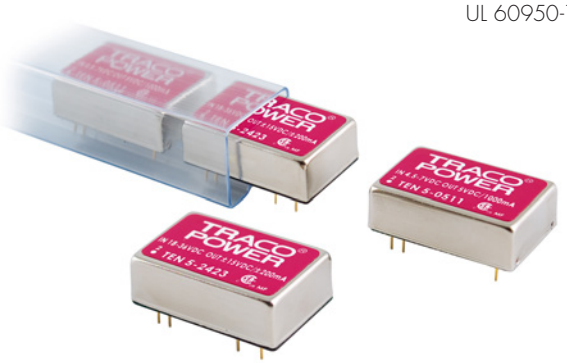
TEN 5 Series, 6 Watt

CB Scheme c SA us

UL 60950-1

Features

- Wide 2:1 input range
- Full SMD-design
- High efficiency up to 86%
- Extended operating temperature range –40°C to 85°C
- I/O isolation 1'500 VDC
- Indefinite short circuit protection
- Input filter to meet EN 55022, class A and FCC, level A without external components
- Shielded metal case with insulated baseplate
- 24-pin DIP with industry standard pinout
- High reliability, MTBF >1 Mio. h
- 3-year product warranty



The TEN 5 Series is a range of DC/DC-converter modules with wide input range of 2:1. State of the art SMD-technology guarantees a product with very high reliability and good cost /performance ratio. I/O-isolation of 1'500 VDC together with conducted noise compliance to EN 55022-A and FCC level A makes these converters ideal for a wide range of applications in communications, mobile battery powered equipments and industrial systems.

Models

Ordercode	Input voltage range	Output voltage	Output current max.	Efficiency typ.
TEN 5-0510	4.5 – 7 VDC (5 VDC nominal)	3.3 VDC	1200 mA	75 %
TEN 5-0511		5 VDC	1000 mA	79 %
TEN 5-0512		12 VDC	500 mA	82 %
TEN 5-0513		15 VDC	400 mA	82 %
TEN 5-0521		±5 VDC	±500 mA	79 %
TEN 5-0522		±12 VDC	±250 mA	82 %
TEN 5-0523		±15 VDC	±200 mA	82 %
TEN 5-1210	9 – 18 VDC (12 VDC nominal)	3.3 VDC	1200 mA	77 %
TEN 5-1211		5 VDC	1000 mA	81 %
TEN 5-1212		12 VDC	500 mA	84 %
TEN 5-1213		15 VDC	400 mA	84 %
TEN 5-1221		±5 VDC	±500 mA	81 %
TEN 5-1222		±12 VDC	±250 mA	84 %
TEN 5-1223		±15 VDC	±200 mA	84 %
TEN 5-2410	18 – 36 VDC (24 VDC nominal)	3.3 VDC	1200 mA	79 %
TEN 5-2411		5 VDC	1000 mA	83 %
TEN 5-2412		12 VDC	500 mA	86 %
TEN 5-2413		15 VDC	400 mA	86 %
TEN 5-2421		±5 VDC	±500 mA	83 %
TEN 5-2422		±12 VDC	±250 mA	86 %
TEN 5-2423		±15 VDC	±200 mA	86 %
TEN 5-4810	36 – 75 VDC (48 VDC nominal)	3.3 VDC	1200 mA	79 %
TEN 5-4811		5 VDC	1000 mA	83 %
TEN 5-4812		12 VDC	500 mA	86 %
TEN 5-4813		15 VDC	400 mA	86 %
TEN 5-4821		±5 VDC	±500 mA	83 %
TEN 5-4822		±12 VDC	±250 mA	86 %
TEN 5-4823		±15 VDC	±200 mA	86 %

Input Specifications

Input current no load	5 Vin models:	80 mA typ.
	12 Vin models:	30 mA typ.
	24 Vin models:	15 mA typ.
	48 Vin models:	8 mA typ.
Start-up voltage / under voltage shut down	5 Vin models:	4.4 VDC / 4.0 VDC (or lower)
	12 Vin models:	8.0 VDC / 8.0 VDC (or lower)
	24 Vin models:	16.0 VDC / 16.0 VDC (or lower)
	48 Vin models:	32.0 VDC / 32.0 VDC (or lower) long term operation at undervoltage will demage the converter!
Surge voltage (1 sec. max.)	5 Vin models:	10 V max.
	12 Vin models:	25 V max.
	24 Vin models:	50 V max.
	48 Vin models:	100 V max.
Reverse voltage protection		1.0 A max.
Conducted noise (input)		EN 55022 class A, FCC part 15, level A

Output Specifications

Voltage set accuracy		1.0 %
Regulation	– Input variation Vin min. to Vin max.	0.3 % max.
	– Load variation 20 – 100 %	
	single output models:	1.0 % max.
	dual output models balanced load:	2.0 % max.
	dual output models unbalanced load:	5.0 % max. (25 % / 100 %)
Minimum load		5 % of rated max current (operation at lower load condition is safe but a higher output ripple will be experienced)
Ripple and noise (20 MHz Bandwidth)		50 mVpk-pk typ., 75 mVpk-pk max.
Temperature coefficient		±0.02 %/K
Output current limitation		>120 % of Iout max., foldback
Short-circuit protection		indefinite (automatic recovery)
Start up time (nominal Vin and constant resistive load)		10 ms typ. (for power on and remote on)
Capacitive load	single output models:	6800 µF max.
	dual output models:	1000 µF max. (each output)

General Specifications

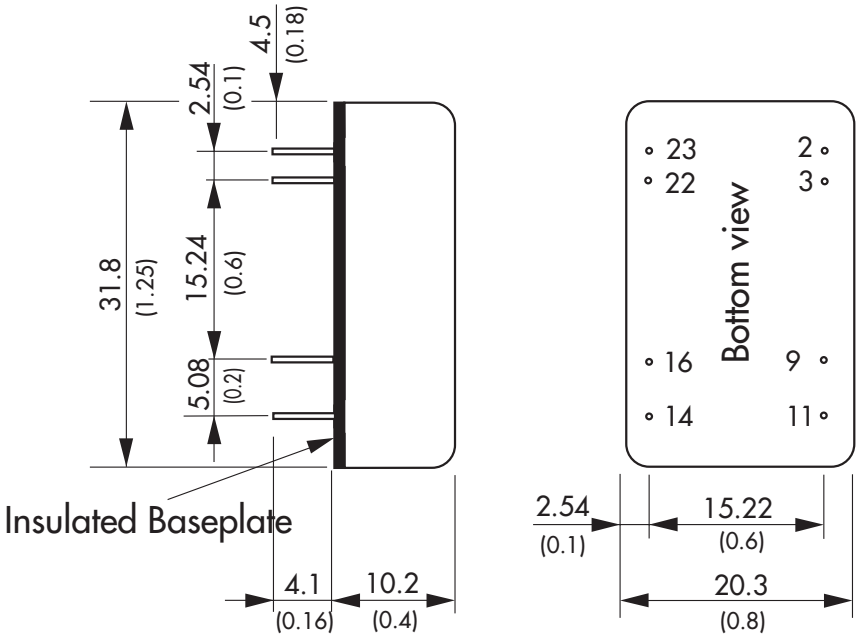
Temperature ranges	– Operating	–40°C to +85°C
	– Case temperature	+90°C max.
	– Storage	–50°C to +125°C
Derating		3.3 %/K above 70°C
Humidity (non condensing)		95 % rel H max.
Reliability, calculated MTBF (MIL-HDBK-217F, at +25°C, ground benign)		>1 Mio. h
Isolation voltage (60 sec.)	– Input/Output	1'500 VDC
Isolation capacitance	– Input/Output	380 pF typ.
Isolation resistance	– Input/Output	>1'000 M Ohm (500 VDC)
Switching frequency		300 kHz typ. (Pulse frequency modulation PFM)
Safety standards		UL 60950-1, IEC/EN 60950-1
Safety approval		CSA File No. 226037 http://directories.csa-international.org
Environmental compliance	– Reach	www.tracopower.com/products/ten5-reach.pdf
	– RoHS	directive 2011/65/EU

All specifications valid at nominal input voltage, full load and +25°C after warm-up time unless otherwise stated.

Physical Specifications

Casing material	steel, metal
Baseplate material	non conductive FR4
Potting material	epoxy (UL 94V-0 rated)
Weight	16.9 g (0.59 oz)
Soldering temperature	max. 260°C / 10 sec.

Outline Dimensions



Pin-Out		
Pin	**Single**	**Dual**
2	–Vin (GND)	–Vin (GND)
3	–Vin (GND)	–Vin (GND)
9	No pin	Common
11	No con.	–Vout
14	+Vout	+Vout
16	–Vout	Common
22	+Vin (Vcc)	+Vin (Vcc)
23	+Vin (Vcc)	+Vin (Vcc)

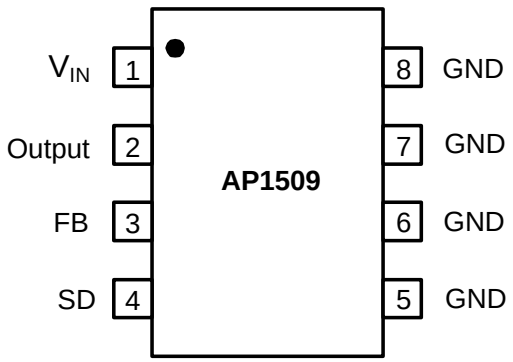
Dimensions in [mm], () = Inch
Pin diameter ø 0.5 ±0.05 (0.02 ±0.002)
Tolerances ±0.25 (±0.01)
Pin pitch tolerances ±0.13 (±0.005)

Description

The AP1509 series are monolithic IC designed for a step-down DC/DC converter, and own the ability of driving a 2A load without additional transistor. It saves board space. The external shutdown function can be controlled by logic level and then come into standby mode. The internal compensation makes feedback control having good line and load regulation without external design. Regarding protected function, thermal shutdown is to prevent over temperature operating from damage, and current limit is against over current operating of the output switch. If current limit function occurs and V_{FB} is down below 0.5V, the switching frequency will be reduced. The AP1509 series operates at a switching frequency of 150KHz thus allow smaller sized filter components than what would be needed with lower frequency switching regulators. Other features include a guaranteed ±4% tolerance on output voltage under specified input voltage and output load conditions, and ±15% on the oscillator frequency. The output version included fixed 3.3V, 5V, 12V, and an adjustable type. The chips are available in a standard 8-lead SOP-8 package.

Pin Assignments

(Top View)



SOP-8L

Features

- Output Voltage: 3.3V, 5V, 12V and Adjustable Output Version
- Adjustable Version Output Voltage Range, 1.23V to 18V+4%
- 150KHz +15% Fixed Switching Frequency
- Voltage Mode Non-Synchronous PWM Control
- Thermal-Shutdown and Current-Limit Protection
- ON/OFF Shutdown Control Input
- Operating Voltage can be up to 22V
- Output Load Current: 2A
- SOP-8L Packages
- Low Power Standby Mode
- Built-in Switching Transistor On Chip
- SOP-8L: Available in “Green” Molding Compound (No Br, Sb)
- Lead Free Finish/ RoHS Compliant (Note 1)

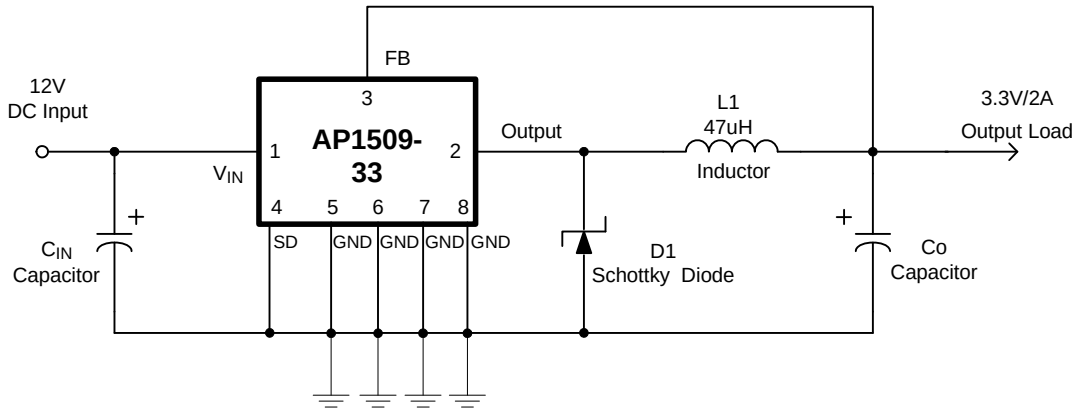
Applications

- Simple High-Efficiency Step-Down Regulator
- On-Card Switching Regulators
- Positive to Negative Converter

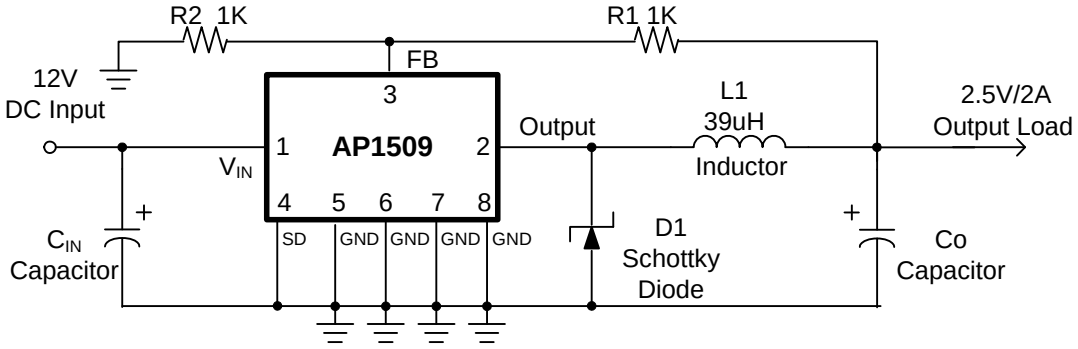
Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at http://www.diodes.com/products/lead_free.html.

Typical Application Circuit

(1) Fixed Type Circuit



(2) Adjustable Type Circuit

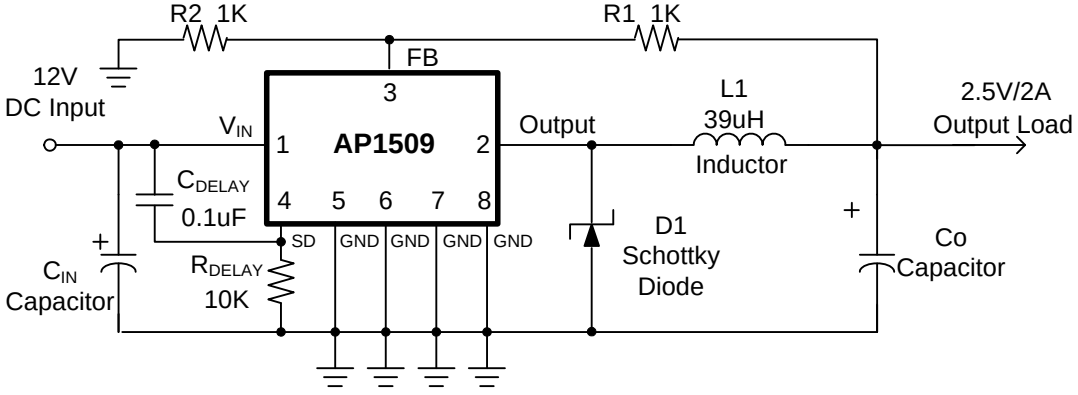


$$V_{OUT} = V_{FB} \times (1 + \frac{R1}{R2})$$

$$V_{FB} = 1.23V$$

$$R2 = 1K \sim 3K$$

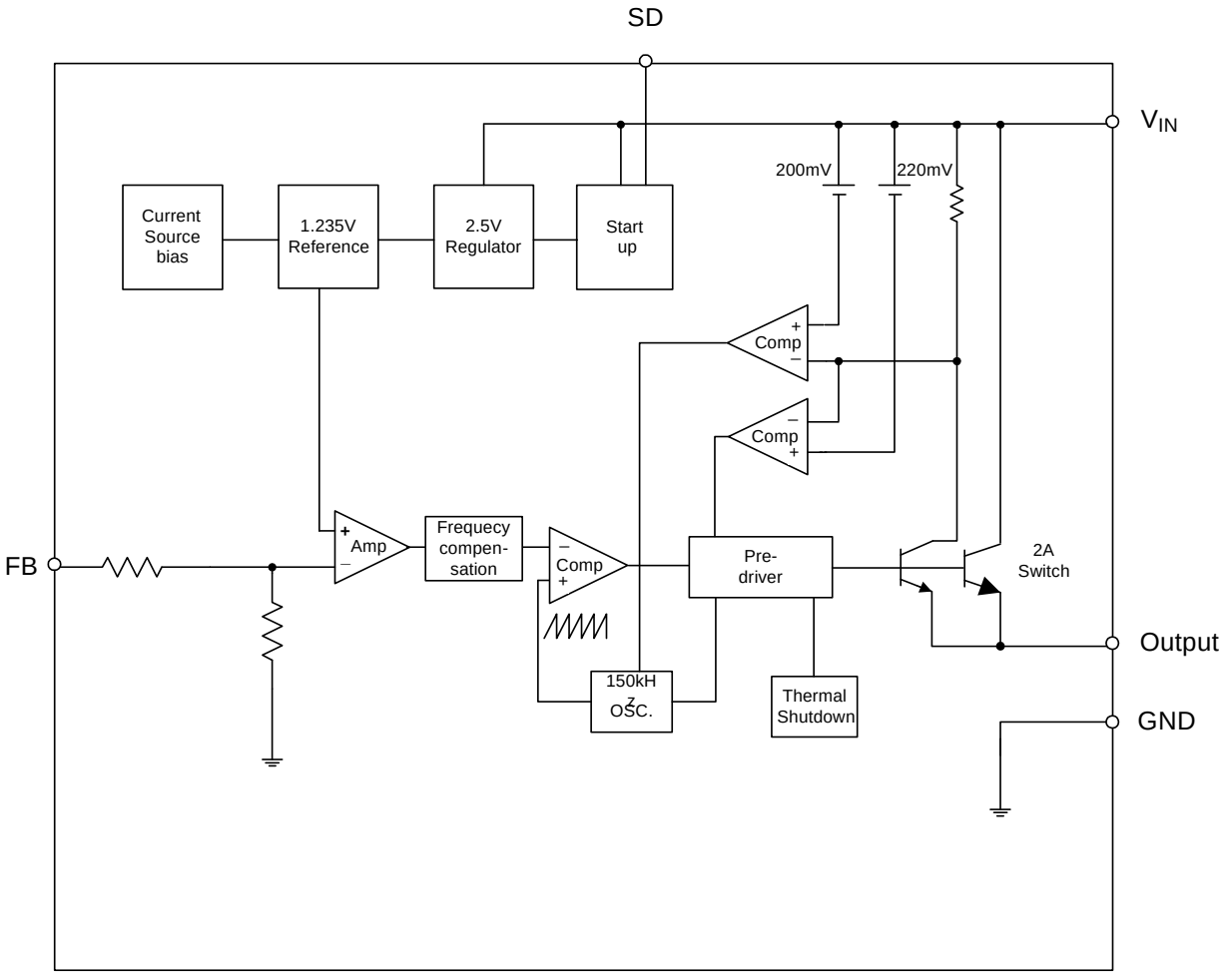
(3) Delay Start Circuit



Pin Descriptions

Pin Name	Description
V_{IN}	Operating voltage input
Output	Switching output
GND	Ground
FB	Output voltage feedback control
SD	ON/OFF Shutdown

Functional Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	KV
ESD MM	Machine Model ESD Protection	200	V
V_{IN}	Supply Voltage	+24	V
V_{SD}	ON/OFF Pin Input Voltage	-0.3 to +18	V
V_{FB}	Feedback Pin Voltage	-0.3 to +18	V
V_{OUT}	Output Voltage to Ground	-1	V
P_D	Power Dissipation	Internally Limited	W
T_{ST}	Storage Temperature	-65 to +150	^oC
T_J	Operating Junction Temperature	-40 to +125	^oC

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
I_{OUT}	Output Current	0	2	A
V_{OP}	Operating Voltage	4.5	22	V
T_A	Operating Ambient Temperature	-20	85	^oC

Electrical Characteristics

Unless otherwise specified, V_{IN} = 12V for 3.3V, 5V, adjustable version and V_{IN} = 18V for the 12V version. I_{LOAD} = 0.5A
Specifications with **boldface type** are for full operating temperature range, the other type are for T_J = 25ºC.

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
I_{FB}	Feedback Bias Current	V_{FB} = 1.3V (Adjustable version only)		-10	-50 **-100**	nA
F_{OSC}	Oscillator Frequency		127 **110**	150	173 **173**	KHz
F_{SCP}	Oscillator Frequency of Short Circuit Protect	When current limit occurred and V_{FB} < 0.5V, T_a = 25 °C	10	30	50	KHz
V_{SAT}	Saturation Voltage	I_{OUT} = 2A No outside circuit V_{FB} = 0V force driver on		1.25	1.4 **1.5**	V
DC	Max. Duty Cycle (ON)	V_{FB} = 0V force driver on		100		%
	Min. Duty Cycle (OFF)	V_{FB} = 12V force driver off		0		
I_{CL}	Current Limit	Peak current No outside circuit V_{FB} = 0V force driver on	3			A
I_L	Output = 0 (Output Leakage Current)	No outside circuit V_{FB} = 12V force driver off			-200	uA
	Output = -1 (Output Leakage Current)	V_{IN} = 22V		-5		mA
I_Q	Quiescent Current	V_{FB} = 12V force driver off		5	10	mA
I_{STBY}	Standby Quiescent Current	ON/OFF pin = 5V V_{IN} = 22V		70	150 **200**	uA
V_{IL}	ON/OFF Pin Logic Input Threshold Voltage	Low (regulator ON)	-	1.3	0.6	V
V_{IH}		High (regulator OFF)	2.0		-	
I_H	ON/OFF Pin Logic Input Current	V_{LOGIC} = 2.5V (OFF)			-0.01	uA
I_L	ON/OFF Pin Input Current	V_{LOGIC} = 0.5V (ON)		-0.1	-1	
θ_{JA}	Thermal Resistance	SOP-8L (Junction to case)		15		°C/W
θ_{JC}	Thermal Resistance with a copper area of approximately 3 in^2	SOP-8L (Junction to ambient)		70		°C/W

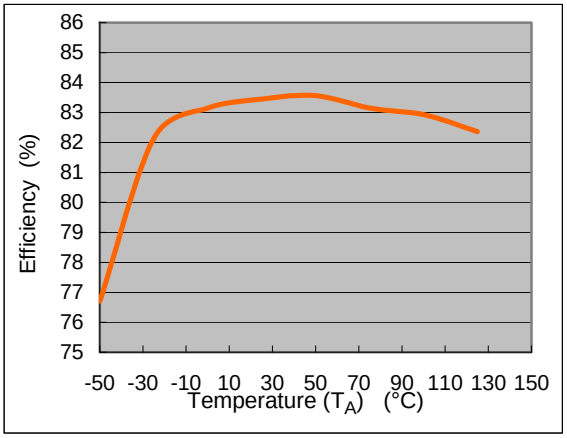
Electrical Characteristics (Continued)

Specifications with **boldface type** are for full operating temperature range, the other type are for T_J = 25ºC.

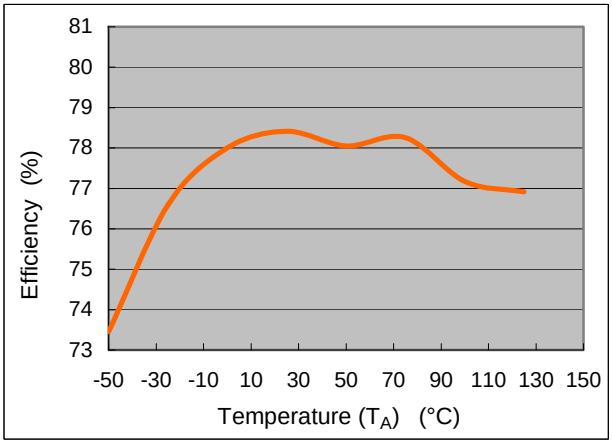
	Symbol	Parameter	Conditions	V_{Min}	Typ.	V_{Max}	Unit
AP1509-ADJ	V_{FB}	Output Feedback	4.5V ≤ V_{IN} ≤ 22V 0.2A ≤ I_{LOAD} ≤ 2A V_{OUT} programmed for 3V	1.193 **1.18**	1.23	1.267 **1.28**	V
	η	Efficiency	V_{IN} = 12V, I_{LOAD}=2A	76	76		%
AP1509-3.3V	V_{OUT}	Output Voltage	4.75V ≤ V_{IN} ≤ 22V 0.2A ≤ I_{LOAD} ≤ 2A	3.168 **3.135**	3.3	3.432 **3.465**	V
	η	Efficiency	V_{IN} = 12V, I_{LOAD} = 2A	78	78		%
AP1509-5V	V_{OUT}	Output Voltage	7V ≤ V_{IN} ≤ 22V 0.2A ≤ I_{LOAD} ≤ 2A	4.8 **4.75**	5	5.2 **5.25**	V
	η	Efficiency	V_{IN} = 12V, I_{LOAD} = 2A	83	83		%
AP1509-12V	V_{OUT}	Output Voltage	15V ≤ V_{IN} ≤ 22V 0.2A ≤ I_{LOAD} ≤ 2A	11.52 **11.4**	12	12.48 **12.6**	V
	η	Efficiency	V_{IN} = 15V, I_{LOAD} = 2A	90	90		%

Typical Performance Characteristics

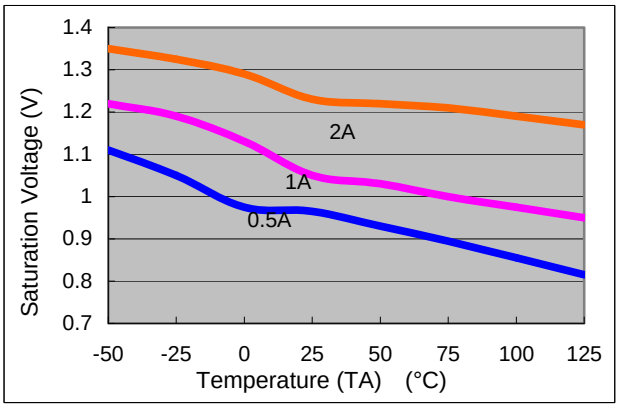
AP1509 Efficiency vs. Temperature
(V_{IN}=12V, V_{OUT}=5V, Io=2A)



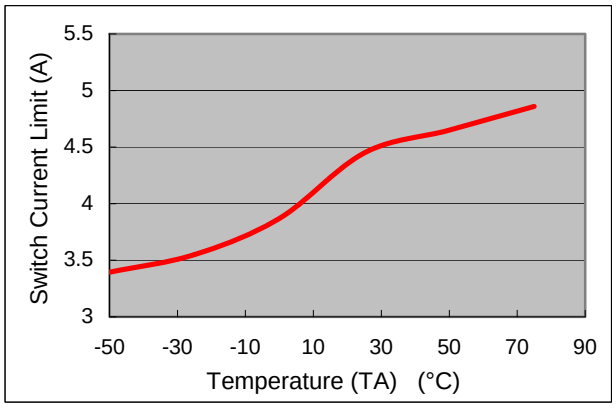
AP1509 Efficiency vs. Temperature
(V_{IN}=12V, V_{OUT}=3.3V, Io=2A)



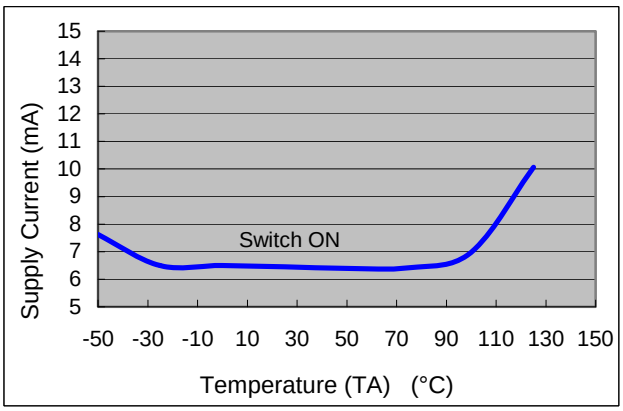
AP1509 Saturation Voltage vs. Temperature
(V_{IN} =12V, V_{FB}=0V, VSD=0)

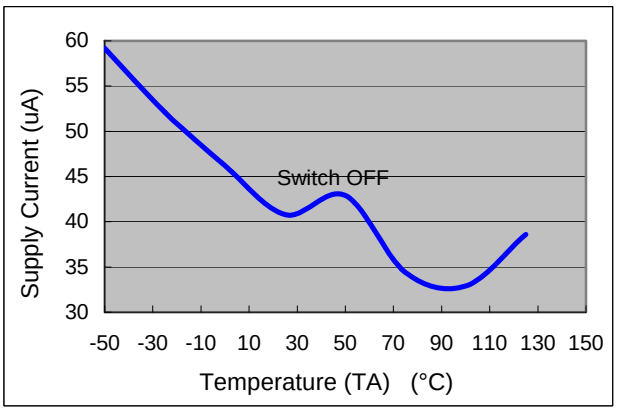


AP1509 Switch Current Limit vs. Temperature
(V_{IN}=12V, V_{FB}=0V)



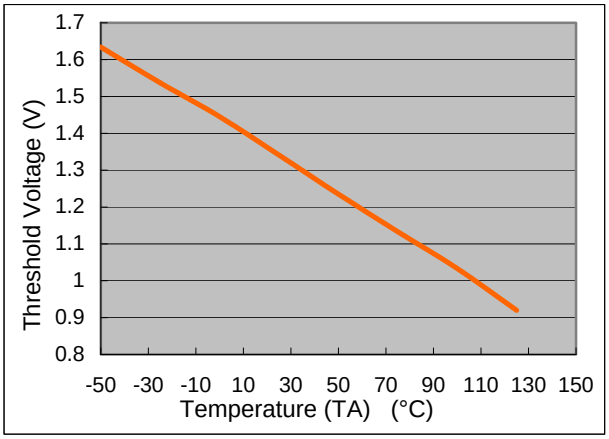
AP1509 Supply Current vs. Temperature
(V_{IN}=12V, No Load, Von/off =0V(Switch ON) ,Von/off =5V(Switch OFF))



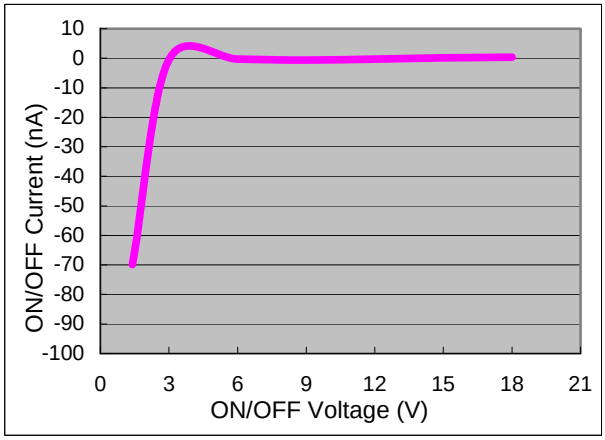


Typical Performance Characteristics (Continued)

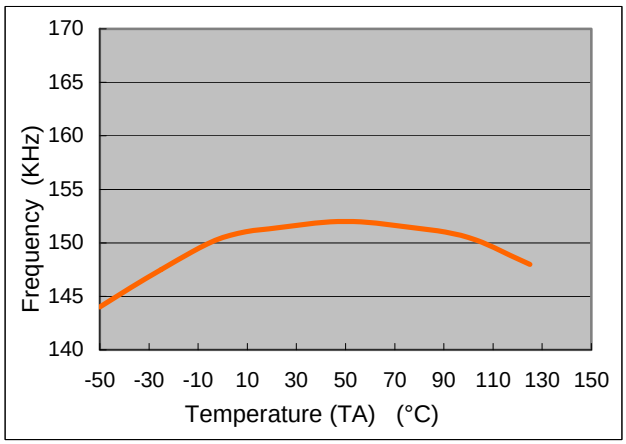
AP1509 Threshold Voltage vs. Temperature
(V_{IN}=12V, Io=100mA)



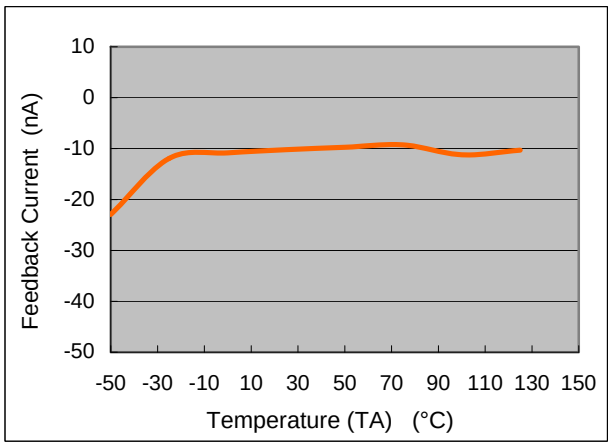
AP1509 ON/OFF Current vs. ON/OFF Voltage
(V_{IN}=12V)



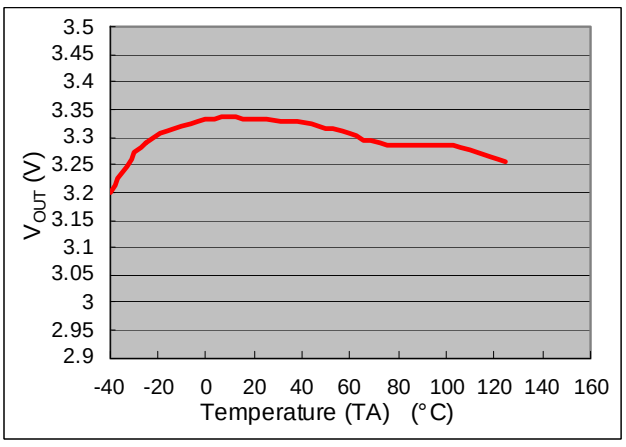
AP1509 Frequency vs. Temperature
(V_{IN}=12V, Io=500mA, V_{OUT}=5V)



AP1509 Feedback Current vs. Temperature
(V_{IN}=12V, V_{OUT}=5V, Vfb=1.3V)

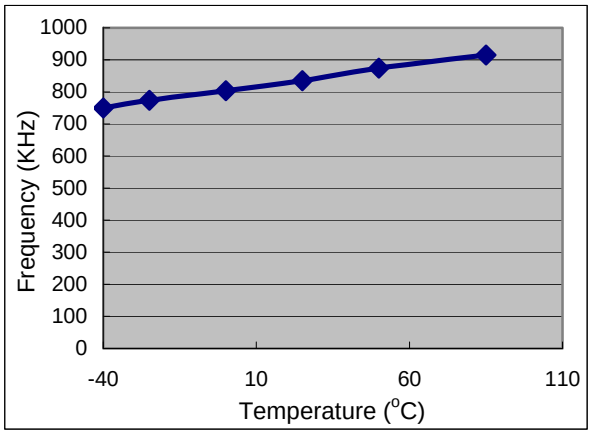


AP1509 Output Voltage vs. Temperature
(V_{IN}=12V, Io=2A)

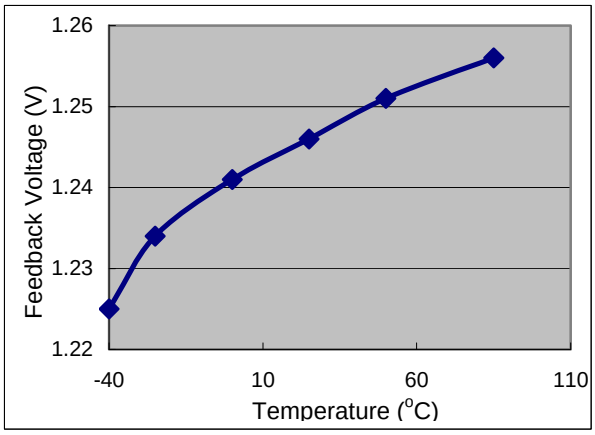


Typical Performance Characteristics (Continued)

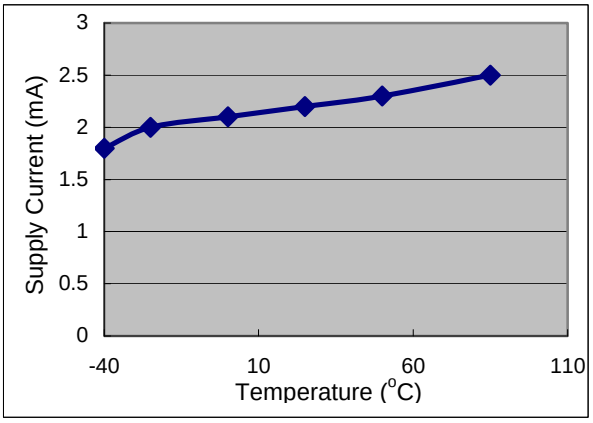
Header Frequency vs. Temperature



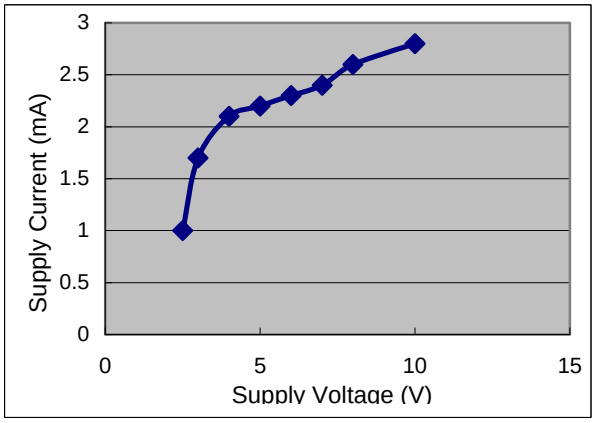
Feedback Voltage vs. Temperature (V_{IN}=15V, V_{OUT}=5V)



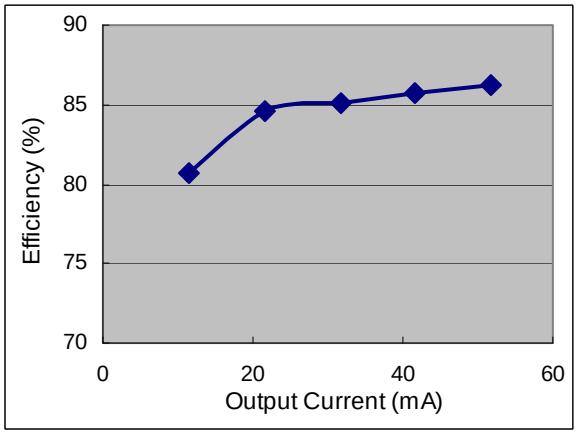
Supply Current vs. Temperature (V_{IN}=15V, V_{OUT}=5V, I_{OUT}=0A)



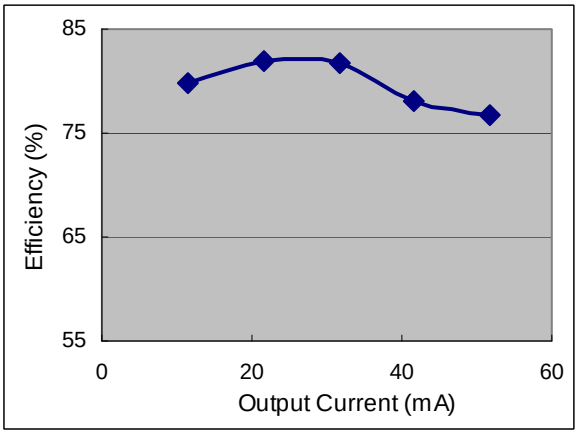
Supply Current vs. Supply Voltage (V_{IN}=15V, V_{OUT}=5V, I_{OUT}=0A)



Efficiency vs. Output Current (V_{IN}=15V, V_{OUT}=5V)



Efficiency vs. Output Current (V_{IN}=15V, V_{OUT}=3.3V)



Functions Description

Pin Functions

$+V_{IN}$

This is the positive input supply for the IC switching regulator. A suitable input bypass capacitor must be presented at this pin to minimize voltage transients and to supply the switching currents needed by the regulator.

Ground

Circuit ground.

Output

Internal switch. The voltage at this pin switches between ($+V_{IN} – V_{SAT}$) and approximately – 0.5V, with a duty cycle of approximately V_{OUT} / V_{IN}. To minimize coupling to sensitive circuitry, the PC board copper area connected to this pin should be minimized.

Feedback

Senses the regulated output voltage to complete the feedback loop.

SD

Allows the switching regulator circuit to be shutdown using logic level signals thus dropping the total input supply current to approximately 150uA. Pulling this pin below a threshold voltage of approximately 1.3V turns the regulator on, and pulling this pin above 1.3V (up to a maximum of 18V) shuts the regulator down. If this shutdown feature is not needed, the SD pin can be wired to the ground pin.

Thermal Considerations

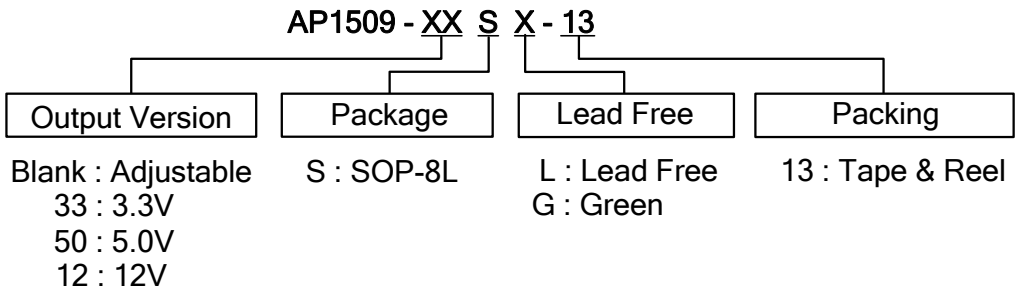
The SOP-8L package needs a heat sink under most conditions. The size of the heat sink depends on the input voltage, the output voltage, the load current and the ambient temperature. The AP1509 junction temperature rises above ambient temperature for a 2A load and different input and output voltages. The data for these curves was taken with the AP1509 (SOP-8L package) operating as a buck-switching regulator in an ambient temperature of 25°C (still air). These temperature increments are all approximate and are affected by many factors. Higher ambient temperatures require more heat sinker.

For the best thermal performance, wide copper traces and generous amounts of printed circuit board copper should be used in the board layout (One exception is the output (switch) pin, which should not have large areas of copper). Large areas of copper provide the best transfer of heat (lower thermal resistance) to the surrounding air, and moving air lowers the thermal resistance even further.

Package thermal resistance and junction temperature increments are all approximate. The increments are affected by a lot of factors. Some of these factors include board size, shape, thickness, position, location, and even board temperature. Other factors are, trace width, total printed circuit copper area, copper thickness, single or double-sided, multi-layer board and the amount of solder on the board.

The effectiveness of the PC board to dissipate heat also depends on the size, quantity and spacing of other components on the board, as well as whether the surrounding air is still or moving. Furthermore, some of these components such as the catch diode will add heat to the PC board and the heat can vary as the input voltage changes. For the inductor, depending on the physical size, type of core material and the DC resistance, it could either act as a heat sink taking heat away from the board, or it could add heat to the board.

Ordering Information

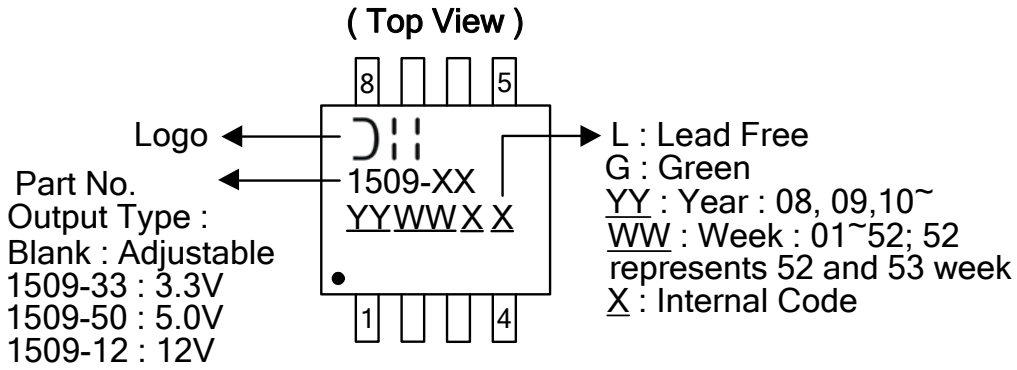


Device	Package Code	Packaging (Note 2)	13" Tape and Reel	
			Quantity	Part Number Suffix
AP1509-XXSL-13	S	SOP-8L	2500/Tape & Reel	-13
AP1509-XXSG-13	S	SOP-8L	2500/Tape & Reel	-13

Notes: 2. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.

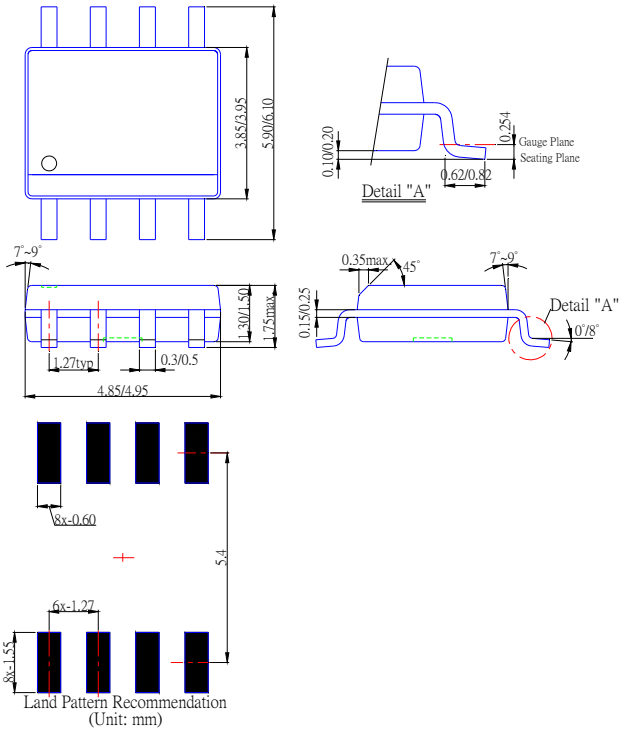
Marking Information

(1) SOP-8L



Package Outline Dimensions (All Dimensions in mm)

(1) Package Type: SOP-8L



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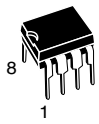
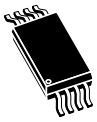
M24C64-W M24C64-R M24C64-F M24C64-DF

64-Kbit serial I²C bus EEPROM

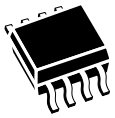
Datasheet - production data



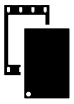
PDIP8 (BN)



TSSOP8 (DW)
169 mil width



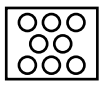
SO8 (MN)
150 mil width



UFDFPN8
(MC)

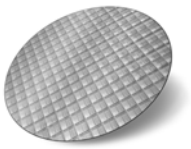
UFDFPN5
(MH)

WLCSP (CS)



Thin WLCSP (CT)

WLCSP
(CU)



Unsawn wafer

Features

- Compatible with all I²C bus modes:
  - 1 MHz
  - 400 kHz
  - 100 kHz
- Memory array:
  - 64 Kbit (8 Kbyte) of EEPROM
  - Page size: 32 byte
  - Additional Write lockable page (M24C64-D order codes)
- Single supply voltage:
  - 1.7 V to 5.5 V over –40 °C / +85 °C
  - 1.6 V to 5.5 V over 0 °C / +85 °C
- Write:
  - Byte Write within 5 ms
  - Page Write within 5 ms
- Random and sequential Read modes
- Write protect of the whole memory array
- Enhanced ESD/Latch-Up protection
- More than 4 million Write cycles
- More than 200-years data retention

Packages

- PDIP8 ECOPACK1®
- SO8 ECOPACK2®
- TSSOP8 ECOPACK2®
- UFDFPN ECOPACK2®
- WLCSP ECOPACK2®
- Unsawn wafer (each die is tested)

This is information on a product in full production. www.st.com

Contents

List of tables

List of figures

1 Description

The M24C64 is a 64-Kbit I^2C-compatible EEPROM (Electrically Erasable PROgrammable Memory) organized as 8 K × 8 bits.

Over an ambient temperature range of -40 °C / +85 °C, the M24C64-W can operate with a supply voltage from 2.5 V to 5.5 V, the M24C64-R can operate with a supply voltage from 1.8 V to 5.5 V, and the M24C64-F and M24C64-DF can operate with a supply voltage from 1.7 V to 5.5 V (the M24C64-F can also operate down to 1.6 V, under some restricting conditions).

The M24C64-D offers an additional page, named the Identification Page (32 byte). The Identification Page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.

Figure 1. Logic diagram

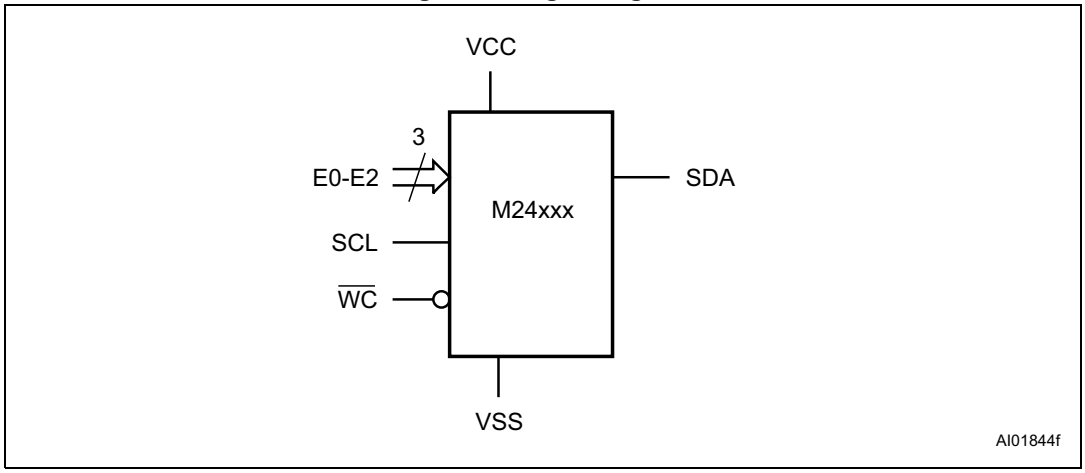
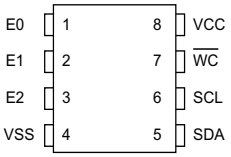


Table 1. Signal names

Signal name	Function	Direction
E2, E1, E0	Chip Enable	Input
SDA	Serial Data	I/O
SCL	Serial Clock	Input
$\overline{WC}$	Write Control	Input
V_{CC}	Supply voltage	-
V_{SS}	Ground	-

Figure 2. 8-pin package connections, top view



AI01845f

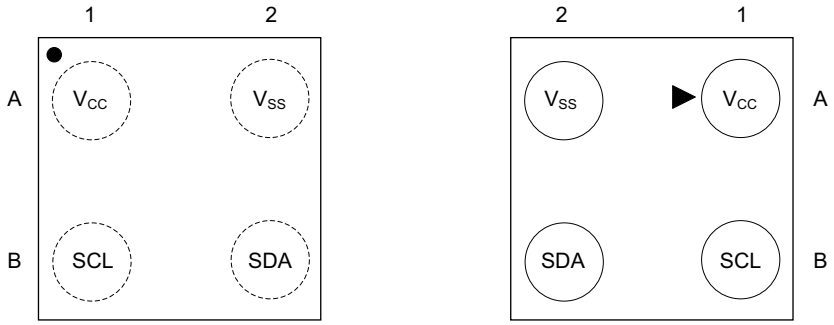
1. See *Section 9: Package mechanical data* for package dimensions, and how to identify pin 1

Figure 3. UFDFPN5 package connections

MS32117V1

Note: Inputs E2, E1, E0 are not connected, therefore read as (000). Please refer to Section 2.3 for further explanations.

Figure 4. WLCSP 4 bump Ultra thin package connections



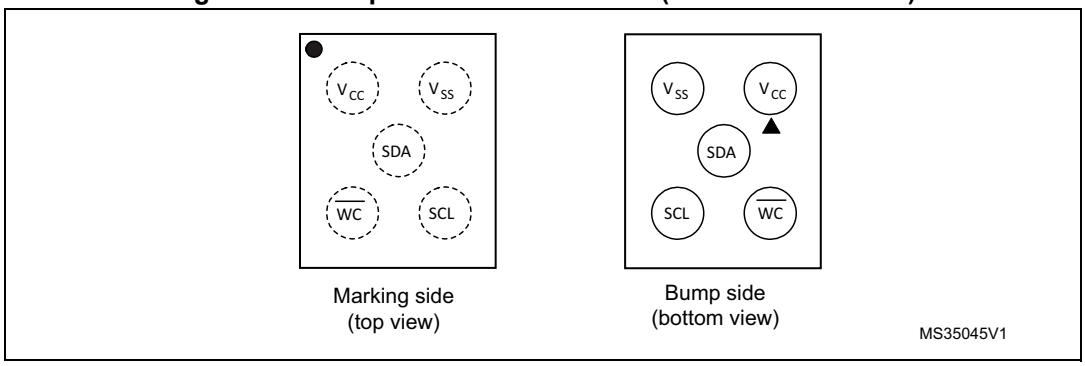
MSv38426V2

1. Inputs E2, E1, E0 are read as (000). Please refer to *Section 2.3* for further explanations.

Table 2. Signals vs. bump position

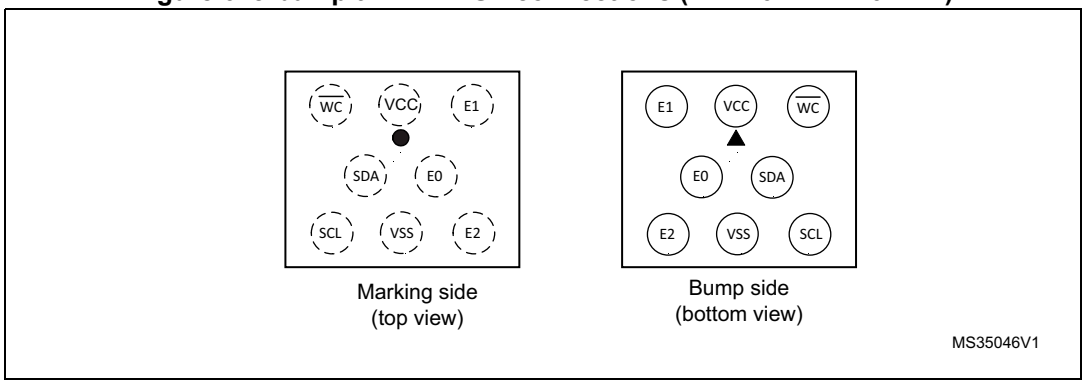
Position	A	B
1	V_{CC}	SCL
2	V_{SS}	SDA

Figure 5. 5-bump WLCSP connections (M24C64-FCS6TP/K)



1. Inputs E2, E1, E0 are internally connected to (001). Please refer to *Section 2.3* for further explanations.

Figure 6. 8-bump thin WLCSP connections (M24C64-DFCT6TP/K)



2 Signal description

2.1 Serial Clock (SCL)

The signal applied on the SCL input is used to strobe the data available on SDA(in) and to output the data on SDA(out).

2.2 Serial Data (SDA)

SDA is an input/output used to transfer data in or data out of the device. SDA(out) is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull-up resistor must be connected from Serial Data (SDA) to V_{CC} (*Figure 15* indicates how to calculate the value of the pull-up resistor).

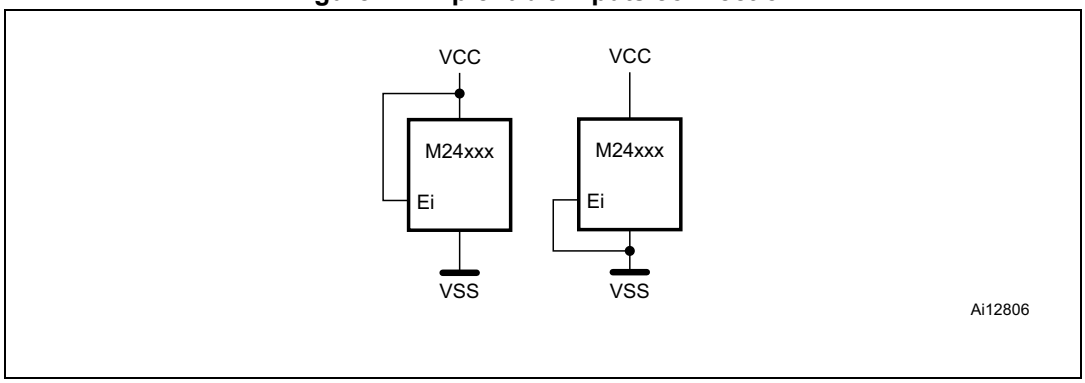
2.3 Chip Enable (E2, E1, E0)

(E2,E1,E0) input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit device select code (see *Table 3*). These inputs must be tied to V_{CC} or V_{SS}, as shown in *Figure 7*. When not connected (left floating), these inputs are read as low (0).

For the 4-balls WLCSP package (see *Figure 4*), the (E2,E1,E0) inputs are internally connected to (0, 0, 0).

For the 5-balls WLCSP package (see *Figure 5*), the (E2,E1,E0) inputs are internally connected to (0,0,1).

Figure 7. Chip enable inputs connection



2.4 Write Control ($\overline{WC}$)

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ($\overline{WC}$) is driven high. Write operations are enabled when Write Control ($\overline{WC}$) is either driven low or left floating.

When Write Control ($\overline{WC}$) is driven high, device select and address bytes are acknowledged, Data bytes are not acknowledged.

2.5 V_{SS} (ground)

V_{SS} is the reference for the V_{CC} supply voltage.

2.6 Supply voltage (V_{CC})

2.6.1 Operating supply voltage (V_{CC})

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see Operating conditions in *Section 8: DC and AC parameters)*. In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_W).

2.6.2 Power-up conditions

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage (see Operating conditions in *Section 8: DC and AC parameters)*.

2.6.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} has reached the internal reset threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see Operating conditions in *Section 8: DC and AC parameters*). When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode; however, the device must not be accessed until V_{CC} reaches a valid and stable DC voltage within the specified [V_{CC}(min), V_{CC}(max)] range (see Operating conditions in *Section 8: DC and AC parameters*).

In a similar way, during power-down (continuous decrease in V_{CC}), the device must not be accessed when V_{CC} drops below V_{CC}(min). When V_{CC} drops below the power-on-reset threshold voltage, the device stops responding to any instruction sent to it.

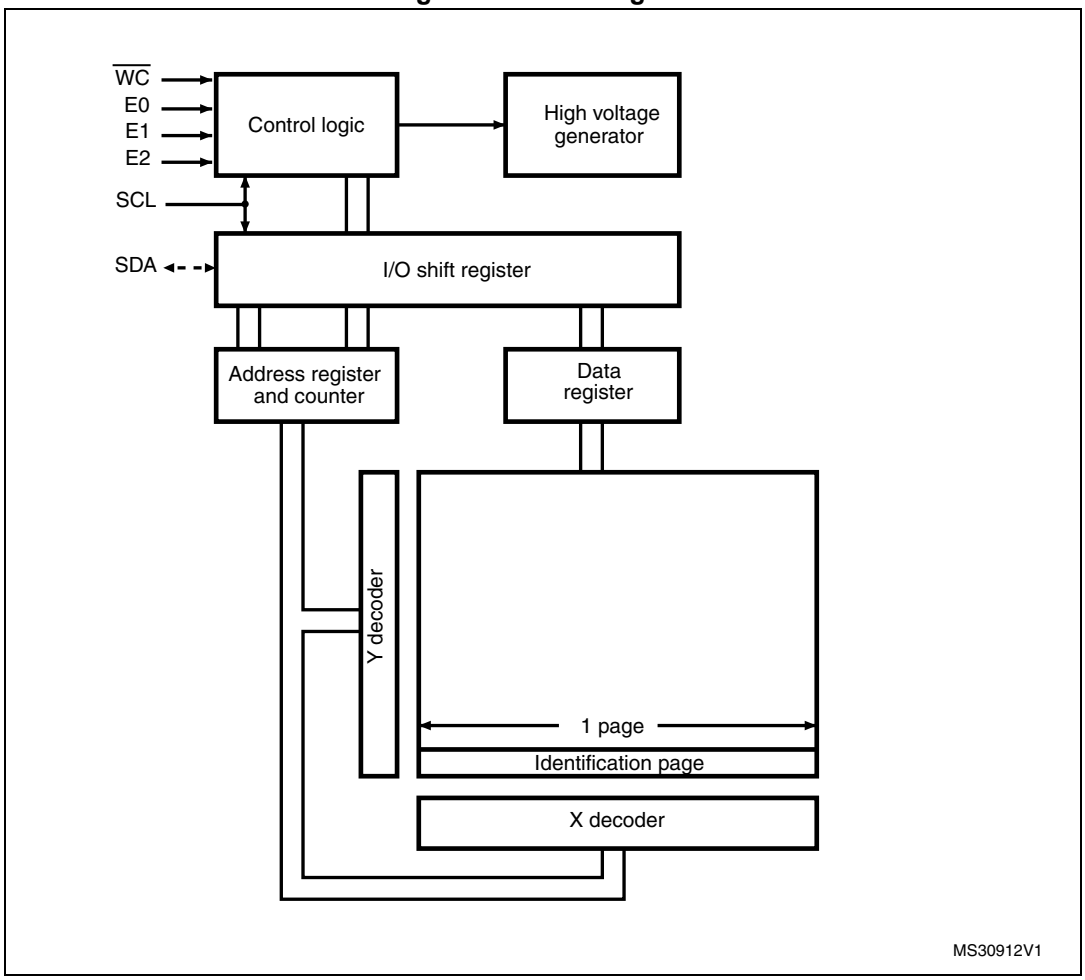
2.6.4 Power-down conditions

During power-down (continuous decrease in V_{CC}), the device must be in the Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

3 Memory organization

The memory is organized as shown below.

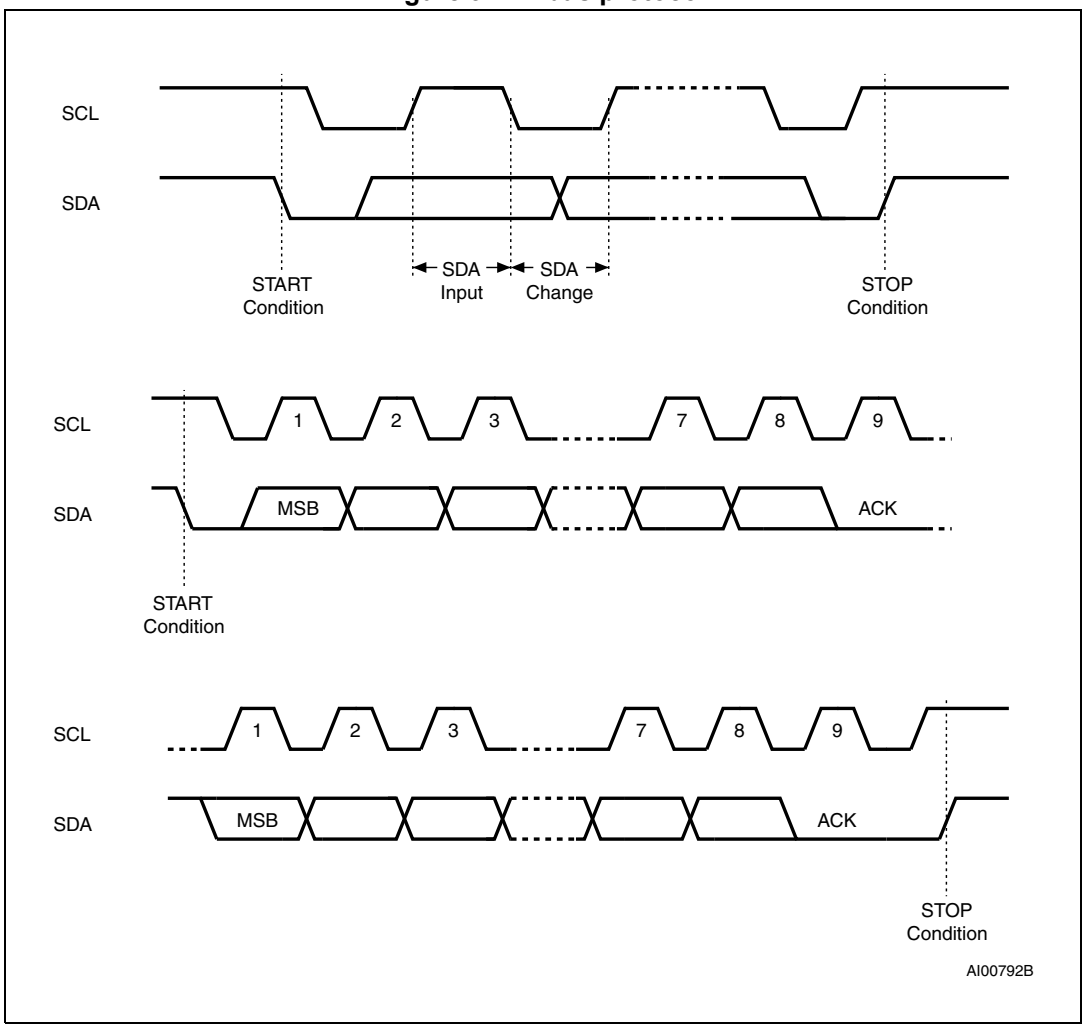
Figure 8. Block diagram



4 Device operation

The device supports the I^2C protocol. This is summarized in *Figure 9*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always a slave in all communications.

Figure 9. I^2C bus protocol



4.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer instruction. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition.

4.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read instruction that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode.

A Stop condition at the end of a Write instruction triggers the internal Write cycle.

4.3 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven low.

4.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9^{th} clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

4.5 Device addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in *Table 3* (most significant bit first).

Table 3. Device select code

	Device type identifier(1)				Chip Enable address(2)			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Device select code when addressing the memory array	1	0	1	0	E2	E1	E0	RW
Device select code when accessing the Identification page	1	0	1	1	E2	E1	E0	RW

1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared with the value read on input pins E0, E1 and E2.

When the device select code is received, the device only responds if the Chip Enable address is the same as the value on its Chip Enable E2,E1,E0 inputs.

The 8th bit is the Read/Write bit (RW). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the device select code, the device deselects itself from the bus, and goes into Standby mode.

5 Instructions

5.1 Write operations

Following a Start condition the bus master sends a device select code with the R/$\overline{W}$ bit (R$\overline{W}$) reset to 0. The device acknowledges this, as shown in *Figure 10*, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data byte.

Table 4. Most significant address byte

A15	A14	A13	A12	A11	A10	A9	A8

Table 5. Least significant address byte

A7	A6	A5	A4	A3	A2	A1	A0

When the bus master generates a Stop condition immediately after a data byte Ack bit (in the “10^{th} bit” time slot), either at the end of a Byte Write or a Page Write, the internal Write cycle t_W is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

After the Stop condition and the successful completion of an internal Write cycle (t_W), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

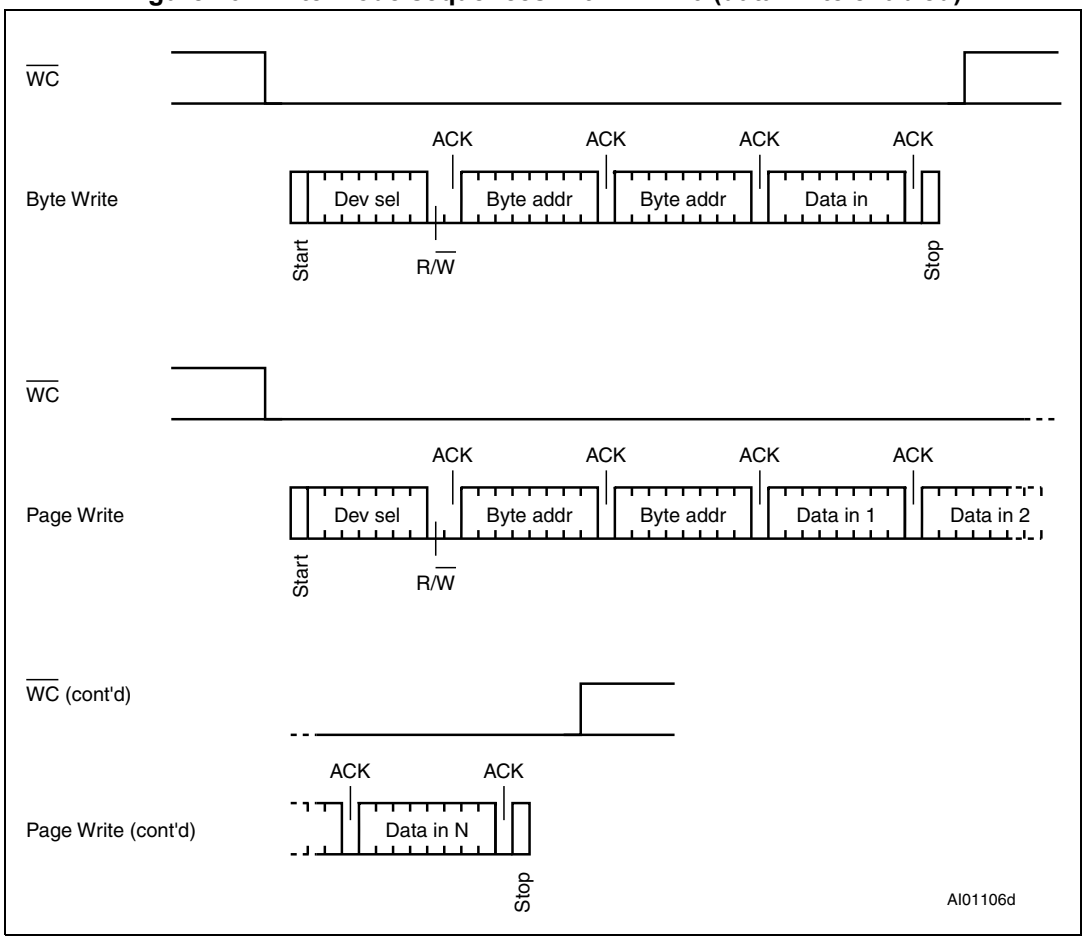
During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

If the Write Control input (WC) is driven High, the Write instruction is not executed and the accompanying data bytes are *not* acknowledged, as shown in *Figure 11*.

5.1.1 Byte Write

After the device select code and the address bytes, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ($\overline{WC}$) being driven high, the device replies with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 10*.

Figure 10. Write mode sequences with $\overline{WC}$ = 0 (data write enabled)



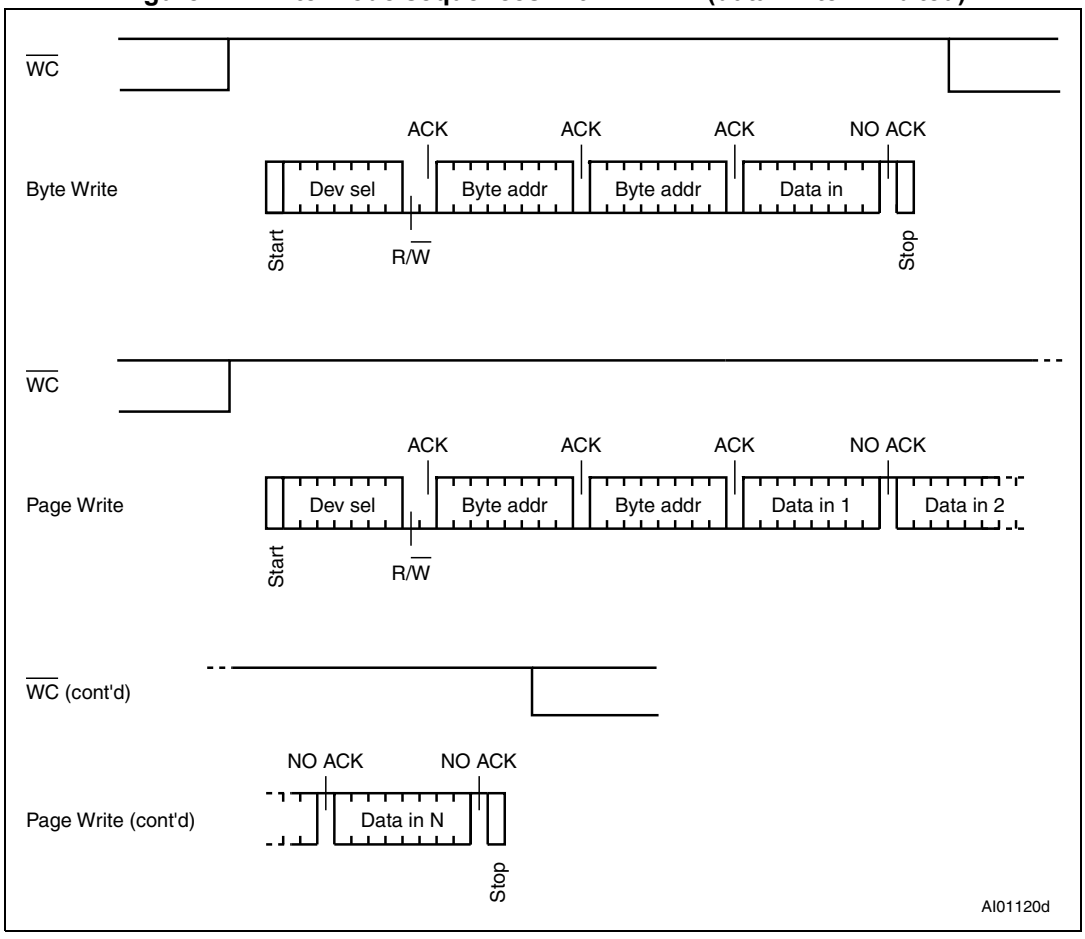
5.1.2 Page Write

The Page Write mode allows up to 32 byte to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits, A15/A5, are the same. If more bytes are sent than will fit up to the end of the page, a “roll-over” occurs, i.e. the bytes exceeding the page end are written on the same page, from location 0.

The bus master sends from 1 to 32 byte of data, each of which is acknowledged by the device if Write Control ($\overline{WC}$) is low. If Write Control ($\overline{WC}$) is high, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck, as shown in *Figure 11*. After each transferred byte, the internal page address counter is incremented.

The transfer is terminated by the bus master generating a Stop condition.

Figure 11. Write mode sequences with $\overline{WC}$ = 1 (data write inhibited)



5.1.3 Write Identification Page (M24C64-D only)

The Identification Page (32 byte) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by issuing the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device type identifier = 1011b
- MSB address bits A15/A5 are don't care except for address bit A10 which must be ‘0’. LSB address bits A4/A0 define the byte address inside the Identification page.

If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoAck).

5.1.4 Lock Identification Page (M24C64-D only)

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

- Device type identifier = 1011b
- Address bit A10 must be ‘1’; all other address bits are don't care
- The data byte must be equal to the binary value xxxx xx1x, where x is don't care

5.1.5 ECC (Error Correction Code) and Write cycling

The ECC is offered only in devices identified with process letter K, all other devices (identified with a different process letter) do not embed the ECC logic.

The Error Correction Code (ECC) is an internal logic function which is transparent for the I^2C communication protocol.

The ECC logic is implemented on each group of four EEPROM bytes(1). Inside a group, if a single bit out of the four bytes happens to be erroneous during a Read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

Even if the ECC function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other bytes located in the same group(1). As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the 4 bytes of the group: the sum of the cycles seen by byte0, byte1, byte2 and byte3 of the same group must remain below the maximum value defined *Table 12: Cycling performance*.

1. A group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer.

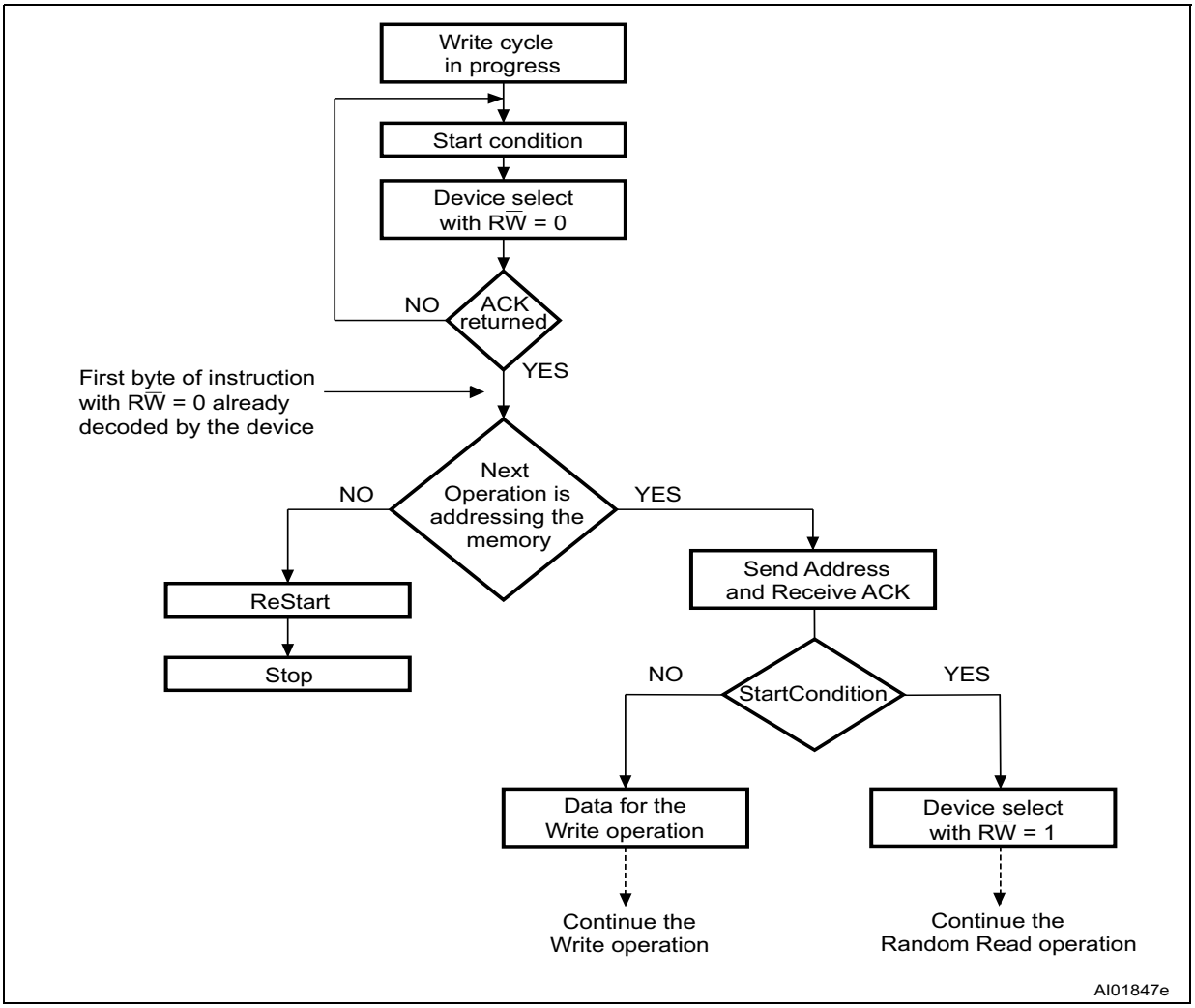
5.1.6 Minimizing Write delays by polling on ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_w) is shown in AC characteristics tables in *Section 8: DC and AC parameters*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 12*, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 12. Write cycle polling flowchart using ACK



1. The seven most significant bits of the Device Select code of a Random Read (bottom right box in the figure) must be identical to the seven most significant bits of the Device Select code of the Write (polling instruction in the figure).

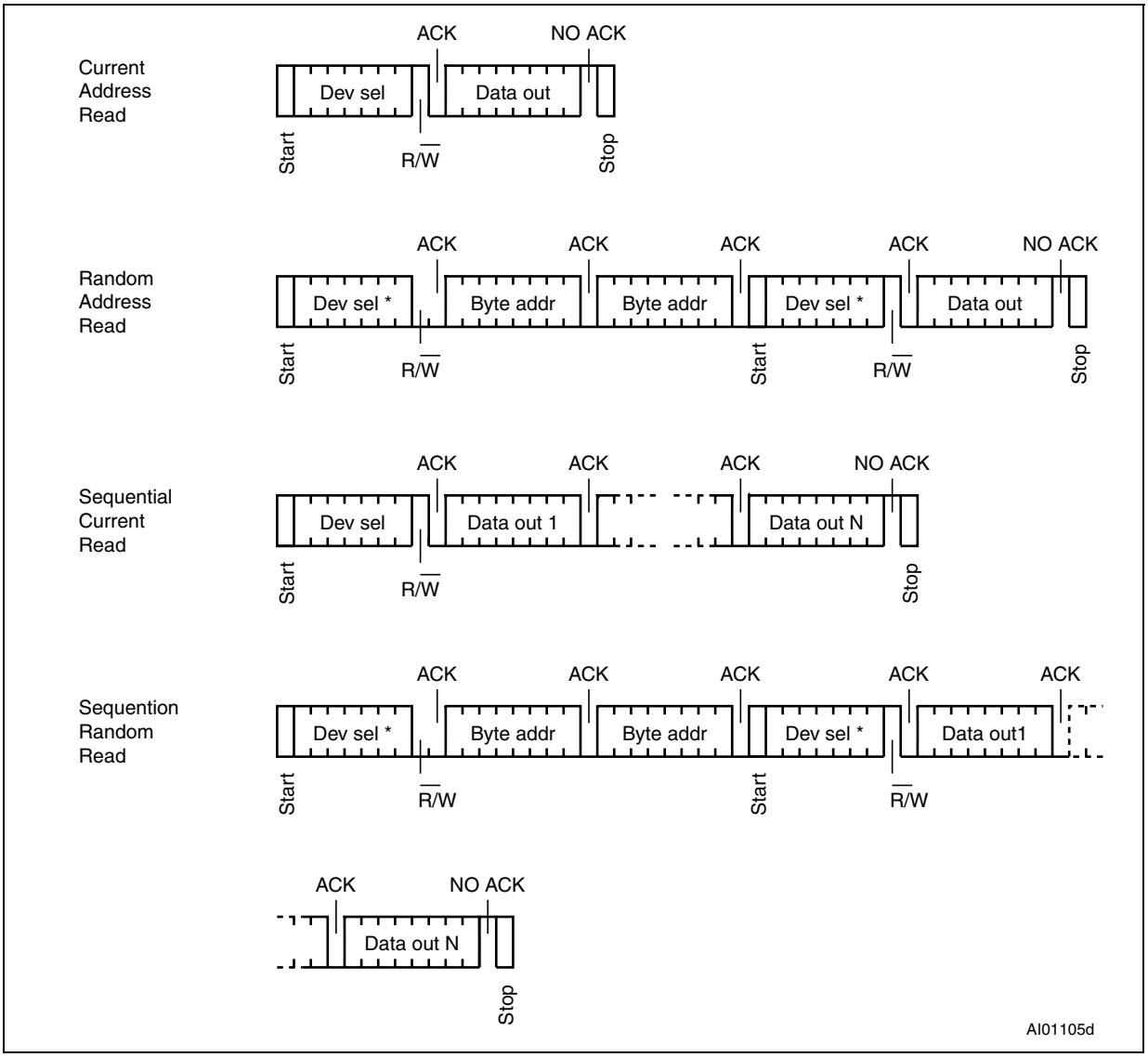
5.2 Read operations

Read operations are performed independently of the state of the Write Control ($\overline{WC}$) signal.

After the successful completion of a Read operation, the device internal address counter is incremented by one, to point to the next byte address.

For the Read instructions, after each byte read (data out), the device waits for an acknowledgment (data in) during the 9th bit time. If the bus master does not acknowledge during this 9th time, the device terminates the data transfer and switches to its Standby mode.

Figure 13. Read mode sequences



5.2.1 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in *Figure 13*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the RW bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

5.2.2 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the R/W bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 13*, *without* acknowledging the byte.

Note that the address counter value is defined by instructions accessing either the memory or the Identification page. When accessing the Identification page, the address counter value is loaded with the byte location in the Identification page, therefore the next Current Address Read in the memory uses this new address counter value. When accessing the memory, it is safer to always use the Random Address Read instruction (this instruction loads the address counter with the byte location to read in the memory, see *Section 5.2.1*) instead of the Current Address Read instruction.

5.2.3 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 13*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter “rolls-over”, and the device continues to output data from memory address 00h.

5.3 Read Identification Page (M24C64-D only)

The Identification Page (32 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

The Identification Page can be read by issuing an Read Identification Page instruction. This instruction uses the same protocol and format as the Random Address Read (from memory array) with device type identifier defined as 1011b. The MSB address bits A15/A5 are don't care, the LSB address bits A4/A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g.: when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 22, as the ID page boundary is 32 bytes).

5.4 Read the lock status (M24C64-D only)

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a NoAck bit if the Identification page is locked.

Right after this, it is recommended to transmit to the device a Start condition followed by a Stop condition, so that:

- Start: the truncated command is not executed because the Start condition resets the device internal logic,
- Stop: the device is then set back into Standby mode by the Stop condition.

6 Initial delivery state

The device is delivered with all the memory array bits and Identification page bits set to 1 (each byte contains FFh).

When delivered in unsawn wafer, all memory bits are set to 1 (each memory byte contains FFh) except the last byte located at address 1FFFh which is written with the value 22h.

7 Maximum rating

Stressing the device outside the ratings listed in *Table 6* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	see note(1)		°C
	PDIP-specific lead temperature during soldering	-	260(2)	°C
I_{OL}	DC output current (SDA = 0)	-	5	mA
V_{IO}	Input or output range	–0.50	6.5	V
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic pulse (Human Body model)(3)	-	3000(4)	V

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb-free assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions of Hazardous Substances (RoHS directive 2011/65/EU of July 2011).
2. T_{LEAD} max must not be applied for more than 10 s.
3. Positive and negative pulses applied on different combinations of pin connections, according to AEC-Q100-002 (compliant with ANSI/ESDA/JEDEC JS-001-2012 standard, C1=100 pF, R1=1500 Ω).
4. 4000 V for devices identified with process letter K and P.

8 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

Table 7. Operating conditions (voltage range W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature	–40	85	°C
f_C	Operating clock frequency	-	1(1)	MHz

1. 400 kHz for devices identified by process letter P.

Table 8. Operating conditions (voltage range R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	85	°C
f_C	Operating clock frequency	-	1(1)	MHz

1. 400 kHz for devices identified by process letter P.

Table 9. Operating conditions (voltage range F)

Symbol	Parameter	Min.		Max.	Unit
V_{CC}	Supply voltage	1.6(1)	1.7	5.5	V
T_A	Ambient operating temperature: READ	-40	-40	85	°C
	Ambient operating temperature: WRITE	0	-40	85	
f_C	Operating clock frequency, $V_{CC} \geq 1.6$ V(1)	-		400	kHz
	Operating clock frequency, $V_{CC} \geq 1.7$ V	-		1000	

1. Only for devices identified with process letter T

Table 10. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_{bus}	Load capacitance	100		pF
-	SCL input rise/fall time, SDA input fall time	-	50	ns
-	Input levels	0.2 V_{CC} to 0.8 V_{CC}		V
-	Input and output timing reference levels	0.3 V_{CC} to 0.7 V_{CC}		V

Figure 14. AC measurement I/O waveform

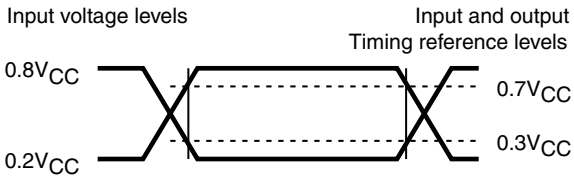


Table 11. Input parameters

Symbol	Parameter(1)	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)	-	-	8	pF
C_{IN}	Input capacitance (other pins)	-	-	6	pF
Z_L	Input impedance (E2, E1, E0, $\overline{WC}$)(2)	$V_{IN} < 0.3\ V_{CC}$	30	-	kΩ
Z_H		$V_{IN} > 0.7\ V_{CC}$	500	-	kΩ

1. Characterized only, not tested in production.
2. input impedance when the memory is selected (after a Start condition).

Table 12. Cycling performance

Symbol	Parameter	Test condition	Max.(1)	Unit
Ncycle	Write cycle endurance(2)	$T_A \leq 25$ °C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	4,000,000	Write cycle(3)
		$T_A = 85$ °C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	1,200,000	

1. Cycling performance for products identified by process letter K or T (previous products were specified with 1 million cycles at 25 °C)
2. The Write cycle endurance is defined by characterization and qualification. For devices embedding the ECC functionality (see *Chapter 5.1.5*), the write cycle endurance is defined for group of four bytes located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3] where N is an integer.
3. A Write cycle is executed when either a Page Write, a Byte write, a Write Identification Page or a Lock Identification Page instruction is decoded. When using the Byte Write, the Page Write or the Write Identification Page, refer also to *Section 5.1.5: ECC (Error Correction Code) and Write cycling*

Table 13. Memory cell data retention

Parameter	Test condition	Min.	Unit
Data retention(1)	$T_A = 55$ °C	200(2)	Year

1. The data retention behavior is checked in production, while the data retention limit defined in this table is extracted from characterization and qualification results.
2. For products identified by process letter K or T (previous products were specified with a data retention of 40 years at 55°C).

Table 14. DC characteristics (M24C64-W, device grade 6)

Symbol	Parameter	Test conditions (in addition to those in *Table 7*)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA, E2, E1, E0)	$V_{IN} = V_{SS}$ or V_{CC}, device in Standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)	2.5 V < V_{CC} < 5.5 V, f_c = 400 kHz (rise/fall time < 50 ns)	-	2	mA
		2.5 V < V_{CC} < 5.5 V, f_c = 1 MHz(1) (rise/fall time < 50 ns)	-	2.5	mA
I_{CC0}	Supply current (Write)	During t_W, 2.5 V ≤ V_{CC} ≤ 5.5 V	-	2.5(2)	mA
I_{CC1}	Standby supply current	Device not selected(3), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5 V	-	2	µA
		Device not selected(3), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5.5 V	-	3(4)	µA
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$, E2, E1, E0)(5)	-	–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	-	0.7 V_{CC}	6.5	V
	Input high voltage ($\overline{WC}$, E2, E1, E0)(6)	-	0.7 V_{CC}	V_{CC}+0.6	V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V or I_{OL} = 3 mA, V_{CC} = 5.5 V	-	0.4	V

1. For devices identified with process letter K or T.
2. Characterized value, not tested in production.
3. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).
4. Previous products (identified with process letter P) offer ICC1(max) = 5 µA
5. E_i inputs should be tied to V_{ss} (see *Section 2.3*).
6. E_i inputs should be tied to V_{cc} (see *Section 2.3*).

Table 15. DC characteristics (M24C64-R device grade 6)

Symbol	Parameter	Test conditions[1] (in addition to those in *Table 8*)	Min.	Max.	Unit
I_{LI}	Input leakage current (E0, E1, E2, SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC}, device in Standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.8 V, f_c= 400 kHz	-	0.8	mA
		f_c= 1 MHz[2]	-	2.5	mA
I_{CC0}	Supply current (Write)[3]	During t_W, 1.8 V ≤ V_{CC} 2.5 V	-	1.5[4]	mA
I_{CC1}	Standby supply current	Device not selected[5], $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8 V	-	1	µA
V_{IL}	Input low voltage (SCL, SDA)[6]	1.8 V ≤ V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	1.8 V ≤ V_{CC} < 2.5 V	0.75 V_{CC}	6.5	V
	Input high voltage ($\overline{WC}$)[7]	1.8 V ≤ V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC}+ 0.6	V
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} = 1.8 V[8]	-	0.2	V

1. If the application uses the voltage range R device with 2.5 V < V_{cc} < 5.5 V and -40 °C < T_A < +85 °C, please refer to *Table 14* instead of this table.
2. Only for devices operating at f_C max = 1 MHz (see note (1) in *Table 18*).
3. For devices identified with process letter K or T
4. Characterized value, not tested in production.
5. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).
6. E_i inputs should be tied to V_{ss} (see *Section 2.3*).
7. E_i inputs should be tied to V_{cc} (see *Section 2.3*).
8. I_{OL} = 0.7 mA for devices identified by process letter P.

Table 16. DC characteristics (M24C64-F, M24C64-DF, device grade 6)

Symbol	Parameter	Test conditions(1) (in addition to those in *Table 9*)	Min.	Max.	Unit
I_{LI}	Input leakage current (E1, E2, SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)	VCC = 1.6 V or 1.7 V, f_C = 400 kHz	-	0.8	mA
		f_C = 1 MHz(2)	-	2.5	
I_{CC0}	Supply current (Write)	During t_W VCC < 2.5 V	-	1.5(3)	mA
I_{CC1}	Standby supply current	Device not selected(4), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.6 V or 1.7 V	-	1	µA
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$, E_i)(5)	V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	V_{CC} < 2.5 V	0.75 V_{CC}	6.5	V
	Input high voltage ($\overline{WC}$, E2, E1, E0)(6)	V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC}+ 0.6	
V_{OL}	Output low voltage	I_{OL} =1mA, V_{CC} = 1.6 V or 1.7 V	-	0.2	V

1. If the application uses the voltage range F device with 2.5 V < V_{CC} < 5.5 V and -40 °C < T_A < +85 °C, please refer to *Table 14* instead of this table.
2. Only for devices identified by process letter K or T (see *Table 18*).
3. Characterized value, not tested in production.
4. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).
5. E_i inputs should be tied to V_{SS}(see *Section 2.3*).
6. E_i inputs should be tied to V_{CC} (see *Section 2.3*).

Table 17. 400 kHz AC characteristics

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	-	400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300	-	ns
t_{QL1QL2}(1)	t_F	SDA (out) fall time	20(2)	300	ns
t_{XH1XH2}	t_R	Input signal rise time	(3)	(3)	ns
t_{XL1XL2}	t_F	Input signal fall time	(3)	(3)	ns
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	100	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX}(4)	t_{DH}	Data out hold time	50(5)	-	ns
t_{CLQV}(6)	t_{AA}	Clock low to next data valid (access time)	-	900	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300	-	ns
t_{WLDL}(7)(1)	$t_{SU:WC}$	$\overline{WC}$ set up time (before the Start condition)	0	-	µs
t_{DHWH}(8)(1)	$t_{HD:WC}$	$\overline{WC}$ hold time (after the Stop condition)	1	-	µs
t_W	t_{WR}	Internal Write cycle duration	-	5	ms
t_{NS}(1)	-	Pulse width ignored (input filter on SCL and SDA) - single glitch	-	50(9)	ns

1. Characterized only, not tested in production.
2. With C_L = 10 pF.
3. There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when f_C < 400 kHz.
4. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
5. The previous products were specified with t_{CLQX} longer than 50 ns. it should be noted that any t_{CLQX} value longer than 50ns offers a safe margin when compared to the I2C-bus specification recommendations.
6. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either $0.3V_{CC}$ or $0.7V_{CC}$, assuming that $R_{bus} \times C_{bus}$ time constant is within the values specified in *Figure 15*.
7. $\overline{WC}$=0 set up time condition to enable the execution of a WRITE command.
8. $\overline{WC}$=0 hold time condition to enable the execution of a WRITE command.
9. The previous products were specified with t_{NS} longer than 50ns. it should be noted that the t_{NS} (max) = 50ns is the value defined by the I2C-bus specification.

Table 18. 1 MHz AC characteristics

Symbol	Alt.	Parameter[1]	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	0	1	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	260	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	500	-	ns
t_{XH1XH2}	t_R	Input signal rise time	(2)	(2)	ns
t_{XL1XL2}	t_F	Input signal fall time	(2)	(2)	ns
t_{QL1QL2}[3]	t_F	SDA (out) fall time	20[4]	120	ns
t_{DXCH}	$t_{SU:DAT}$	Data in setup time	50	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX}[5]	t_{DH}	Data out hold time	50[6]	-	ns
t_{CLQV}[7]	t_{AA}	Clock low to next data valid (access time)	-	450	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	250	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	250	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition setup time	250	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	500	-	ns
t_{WLDL}[8][3]	$t_{SU:WC}$	$\overline{WC}$ set up time (before the Start condition)	0	-	µs
t_{DHWH}[9][3]	$t_{HD:WC}$	$\overline{WC}$ hold time (after the Stop condition)	1	-	µs
t_W	t_{WR}	Write time	-	5	ms
t_{NS}[3]	-	Pulse width ignored (input filter on SCL and SDA)	-	50[10]	ns

1. Only for devices identified by the process letter K or T (devices qualified at 1 MHz).
2. There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be less than 120 ns when f_C < 1 MHz.
3. Characterized only, not tested in production.
4. With C_L = 10 pF.
5. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
6. The previous products were specified with t_{CLQX} longer than 50 ns. it should be noted that any t_{CLQX} value longer than 50ns offers a safe margin when compared to the I2C-bus specification recommendations.
7. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 V_{CC} or 0.7 V_{CC}, assuming that the Rbus × Cbus time constant is within the values specified in *Figure 16*.
8. $\overline{WC}$=0 set up time condition to enable the execution of a WRITE command.
9. $\overline{WC}$=0 hold time condition to enable the execution of a WRITE command.
10. The previous products were specified with t_{NS} longer than 50 ns. it should be noted that the I2C-bus specification recommends a t_{NS} value longer than 50ns.

Figure 15. Maximum R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I2C bus at maximum frequency f_C = 400 kHz

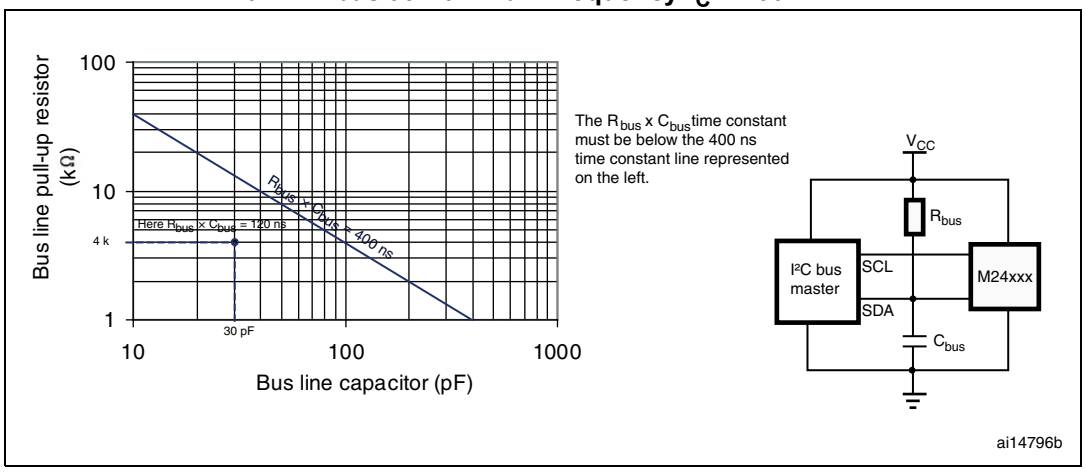


Figure 16. Maximum R_{bus} value versus bus parasitic capacitance C_{bus}) for an I2C bus at maximum frequency f_C = 1MHz

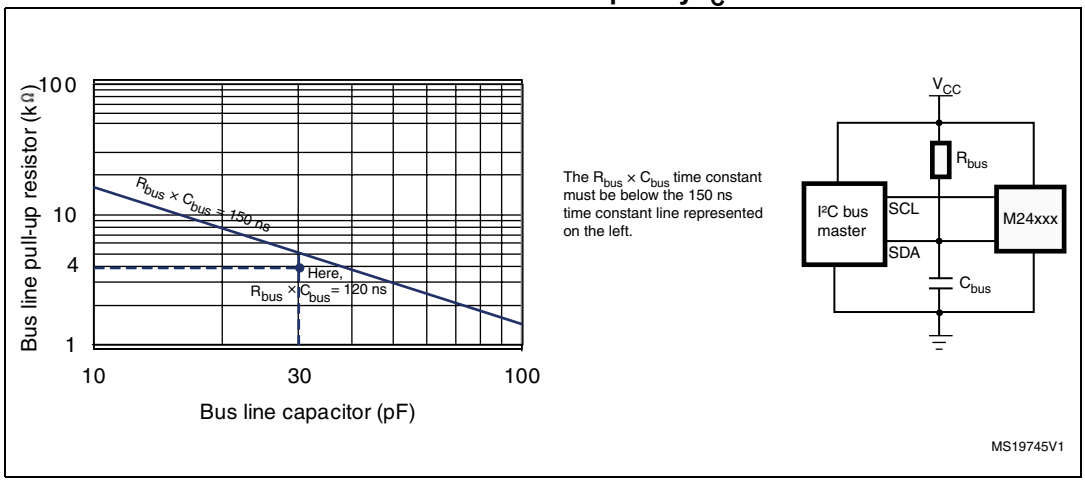
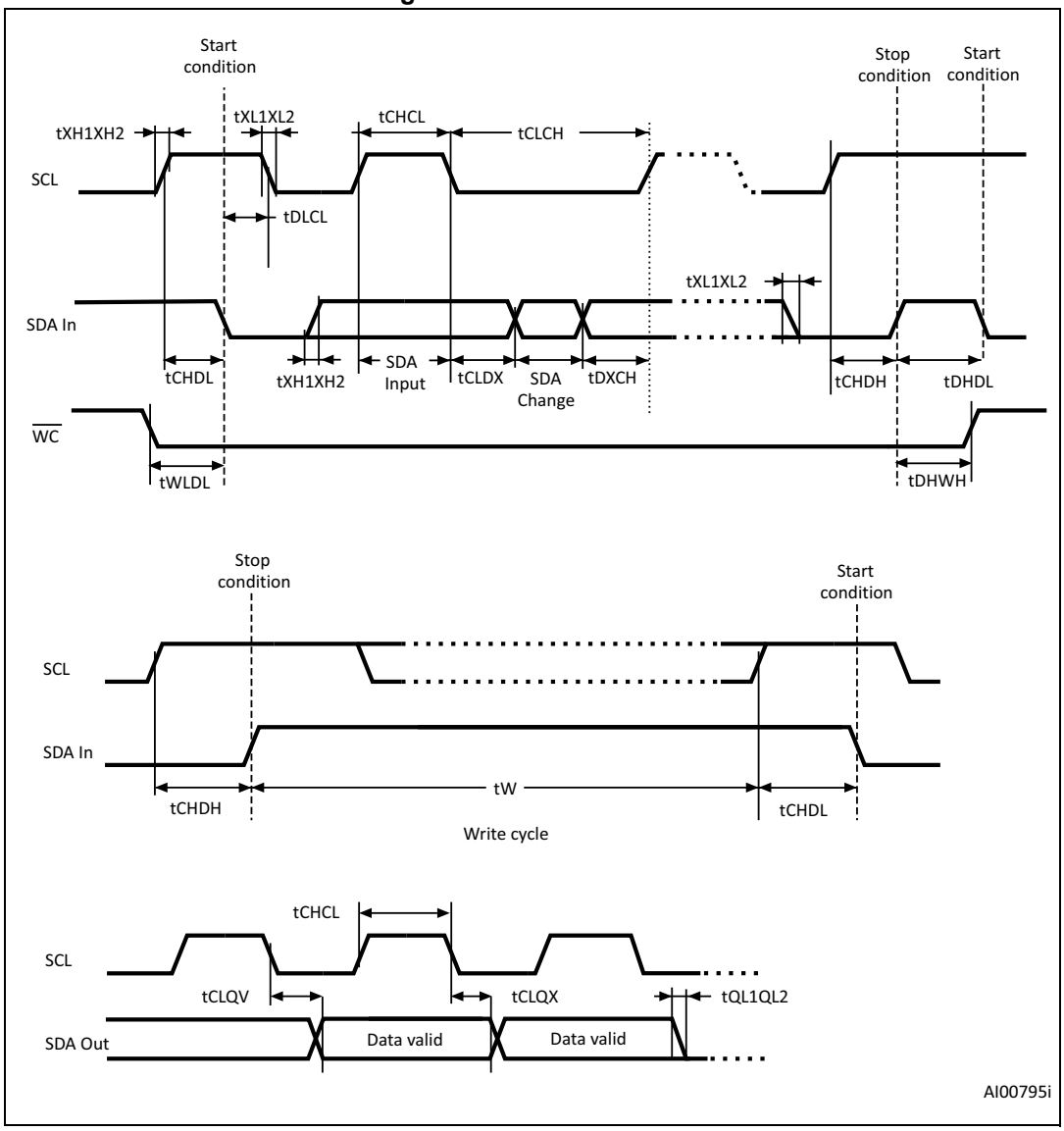


Figure 17. AC waveforms



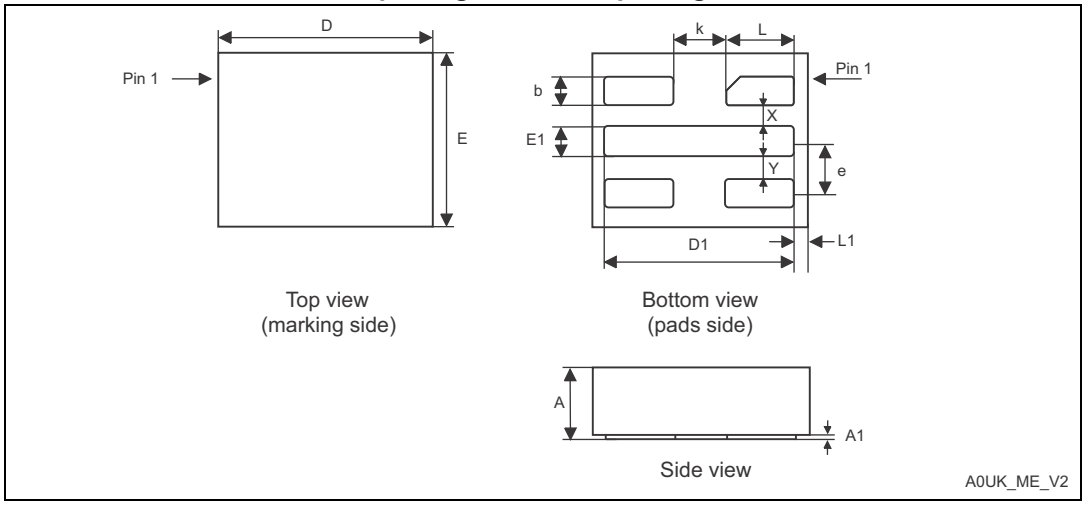
9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

For die information concerning the M24C64 delivered in unsawn wafer, please contact your nearest ST Sales Office.

9.1 UFDFPN5 package information

Figure 18. UFDFPN5 – 1.7x1.4 mm, 0.55 mm thickness, ultra thin fine pitch dual flat package, no lead - package outline



1. On the bottom side, pin 1 is identified by the specific pad shape and, on the top side, pin 1 is defined from the orientation of the marking: when reading the marking, pin 1 is below the upper left package corner.

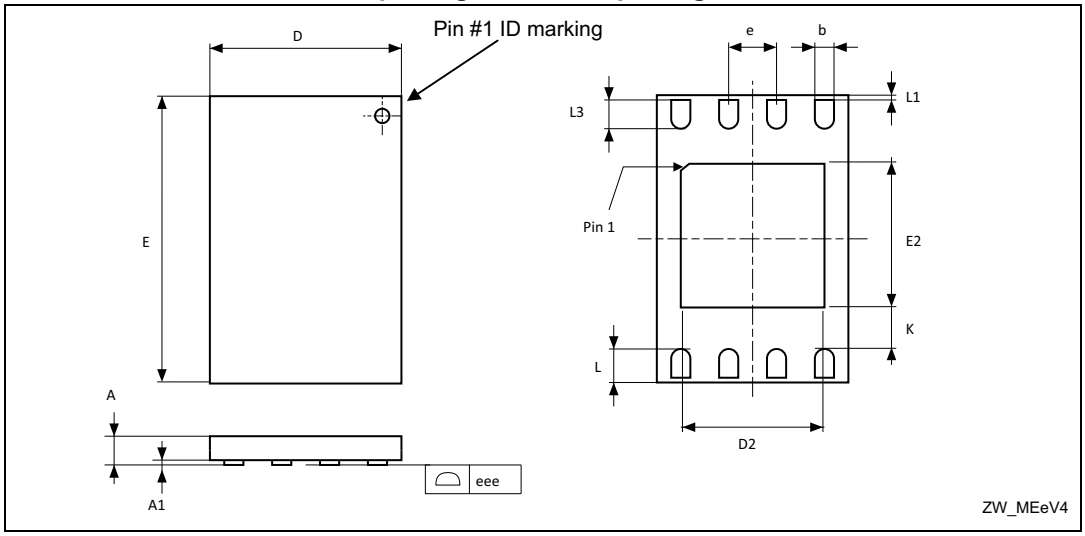
Table 19. UFDFPN5 - 1.7 × 1.4 mm, 0.55 mm thickness, ultra thin fine pitch dual flat package, no lead - package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	-	0.050	0.0000	-	0.0020
b[2]	0.175	0.200	0.225	0.0069	0.0079	0.0089
D	1.600	1.700	1.800	0.0630	0.0669	0.0709
D1	1.400	1.500	1.600	0.0551	0.0591	0.0630
E	1.300	1.400	1.500	0.0512	0.0551	0.0591
E1	0.175	0.200	0.225	0.0069	0.0079	0.0089
X	-	0.200	-	-	0.0079	-
Y	-	0.200	-	-	0.0079	-
e	-	0.400	-	-	0.0157	-
L	0.500	0.550	0.600	0.0197	0.0217	0.0236
L1	-	0.100	-	-	0.0039	-
k	-	0.400	-	-	0.0157	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension b applies to plated terminal and is measured between 0.15 and 0.30mm from the terminal tip.

9.2 UFDFPN8 package information

Figure 19. UFDFPN8 – 2x3 mm, 0.55 thickness, ultra thin fine pitch dual flat package, no lead - package outline



1. Drawing is not to scale.
2. The central pad (the area E2 by D2 in the above illustration) must be either connected to V_{SS} or left floating (not connected) in the end application.

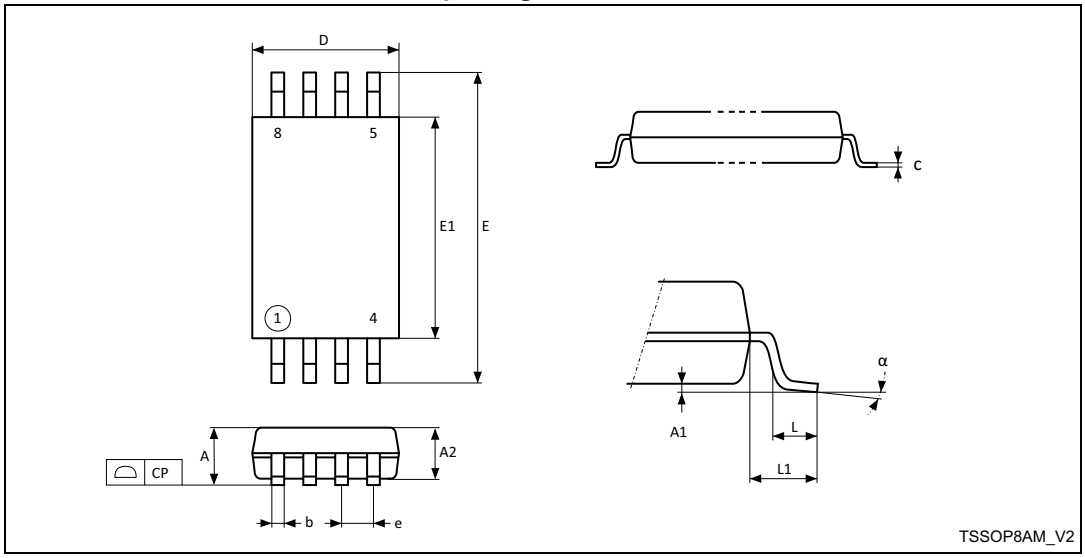
Table 20. UFDFPN8 – 2x3 mm, 0.55 thickness, ultra thin fine pitch dual flat package, no lead - package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.450	0.550	0.600	0.0177	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
D	1.900	2.000	2.100	0.0748	0.0787	0.0827
D2	1.200	–	1.600	0.0472	–	0.0630
E	2.900	3.000	3.100	0.1142	0.1181	0.1220
E2	1.200	–	1.600	0.0472	–	0.0630
e	–	0.500	–	–	0.0197	–
K	0.300	–	–	0.0118	–	–
L	0.300	–	0.500	0.0118	–	0.0197
L1	–	–	0.150	–	–	0.0059
L3	0.300	–	–	0.0118	–	–
eee(2)	0.080	–	–	0.0031	–	–

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

9.3 TSSOP8 package information

Figure 20.TSSOP8 – 3x4.4 mm, 0.65 mm pitch, 8-lead thin shrink small outline, package outline



1. Drawing is not to scale.

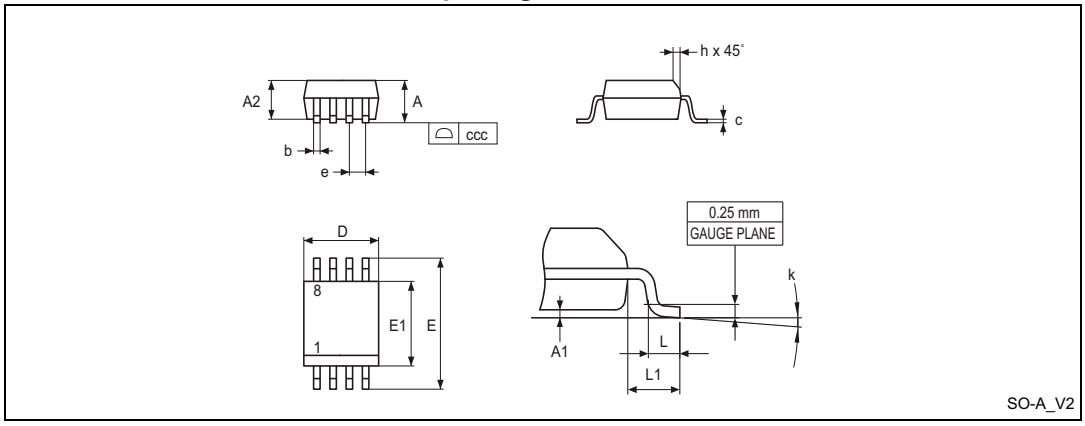
Table 21. TSSOP8 – 3 x 4.4 mm, 0.65 mm pitch, 8-lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
CP	-	-	0.100	-	-	0.0039
D	2.900	3.000	3.100	0.1142	0.1181	0.1220
e	-	0.650	-	-	0.0256	-
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1	4.300	4.400	4.500	0.1693	0.1732	0.1772
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
α	0°	-	8°	0°	-	8°

1. Values in inches are converted from mm and rounded to four decimal digits.

9.4 SO8N package information

Figure 21. SO8N – 3.9x4.9 mm, 8-lead plastic small outline, 150 mils body width, package outline



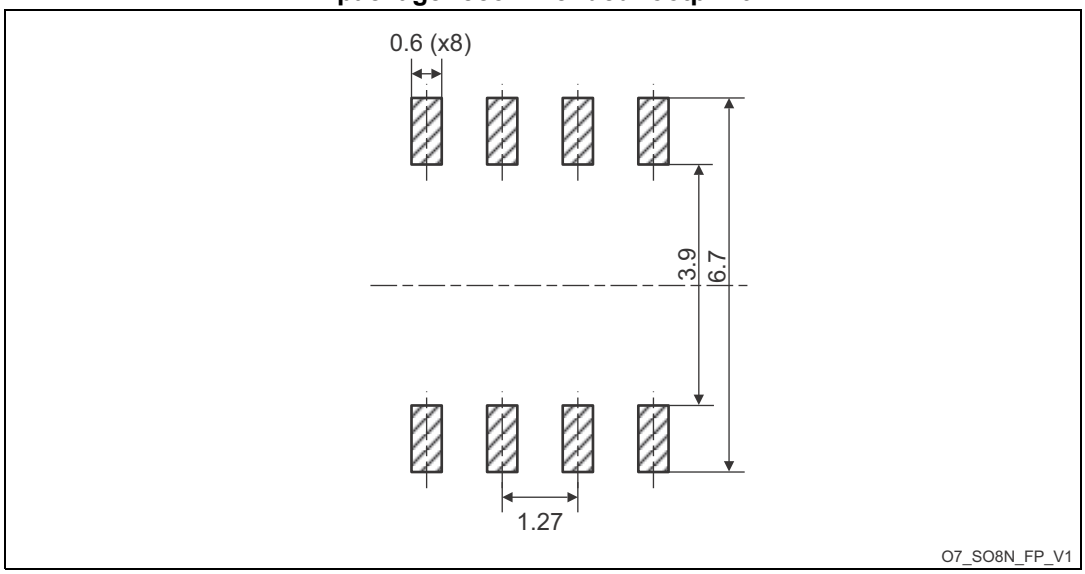
1. Drawing is not to scale.

Table 22. SO8N – 3.9x4.9 mm, 8-lead plastic small outline, 150 mils body width, package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.750	-	-	0.0689
A1	0.100	-	0.250	0.0039	-	0.0098
A2	1.250	-	-	0.0492	-	-
b	0.280	-	0.480	0.0110	-	0.0189
c	0.170	-	0.230	0.0067	-	0.0091
D	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1	3.800	3.900	4.000	0.1496	0.1535	0.1575
e	-	1.270	-	-	0.0500	-
h	0.250	-	0.500	0.0098	-	0.0197
k	0°	-	8°	0°	-	8°
L	0.400	-	1.270	0.0157	-	0.0500
L1	-	1.040	-	-	0.0409	-
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.

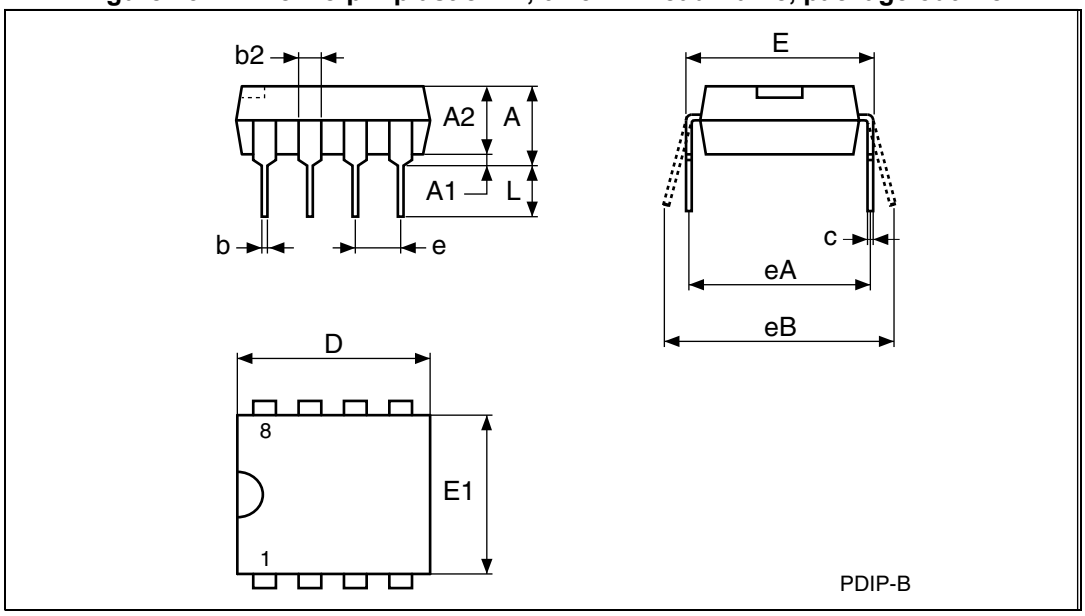
Figure 22. SO8N – 3.9x4.9 mm, 8-lead plastic small outline, 150 mils body width, package recommended footprint



1. Dimensions are expressed in millimeters.

9.5 PDIP8 package information

Figure 23. PDIP8 – 8-pin plastic DIP, 0.25 mm lead frame, package outline



1. Drawing is not to scale.
2. Not recommended for new designs.

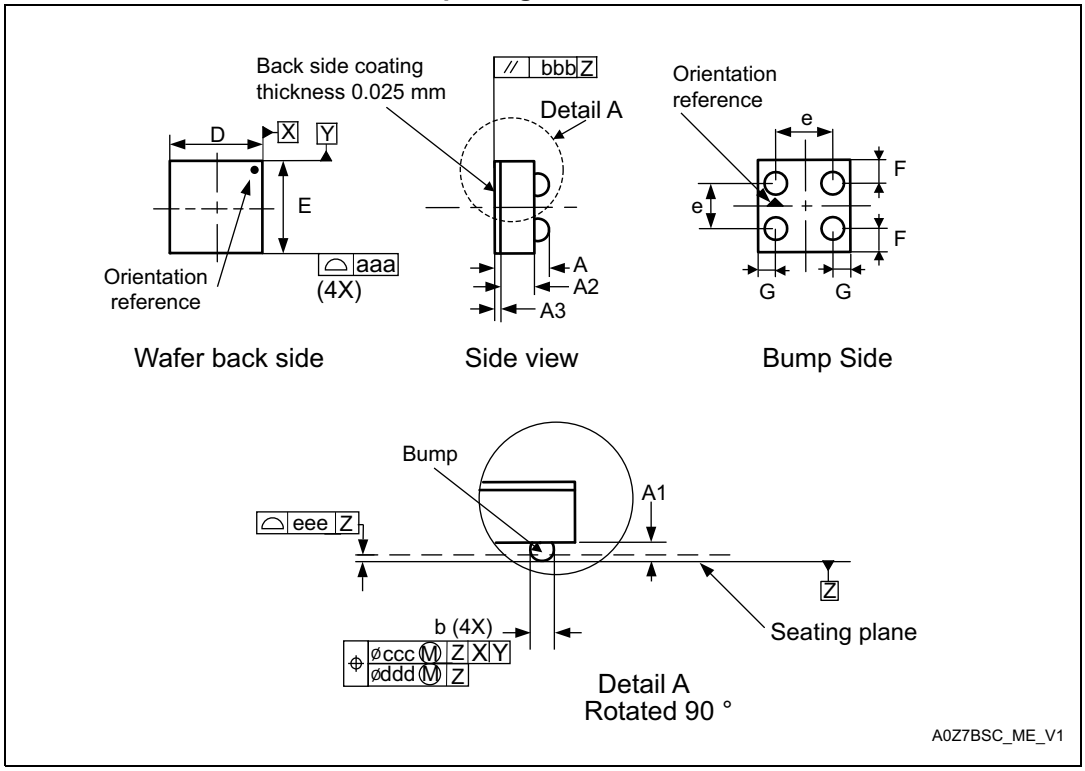
Table 23. PDIP8 – 8-pin plastic DIP, 0.25 mm lead frame, package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	5.33	-	-	0.2098
A1	0.38	-	-	0.0150	-	-
A2	2.92	3.30	4.95	0.1150	0.1299	0.1949
b	0.36	0.46	0.56	0.0142	0.0181	0.0220
b2	1.14	1.52	1.78	0.0449	0.0598	0.0701
c	0.20	0.25	0.36	0.0079	0.0098	0.0142
D	9.02	9.27	10.16	0.3551	0.3650	0.4000
E	7.62	7.87	8.26	0.3000	0.3098	0.3252
E1	6.10	6.35	7.11	0.2402	0.2500	0.2799
e	-	2.54	-	-	0.1000	-
eA	-	7.62	-	-	0.3000	-
eB	-	-	10.92	-	-	0.4299
L	2.92	3.30	3.81	0.1150	0.1299	0.1500

1. Values in inches are converted from mm and rounded to four decimal digits.

9.6 Ultra Thin WLCSP package information

Figure 24. Ultra Thin WLCSP- 4-bump, 0.795 x 0.674 mm, wafer level chip scale package outline



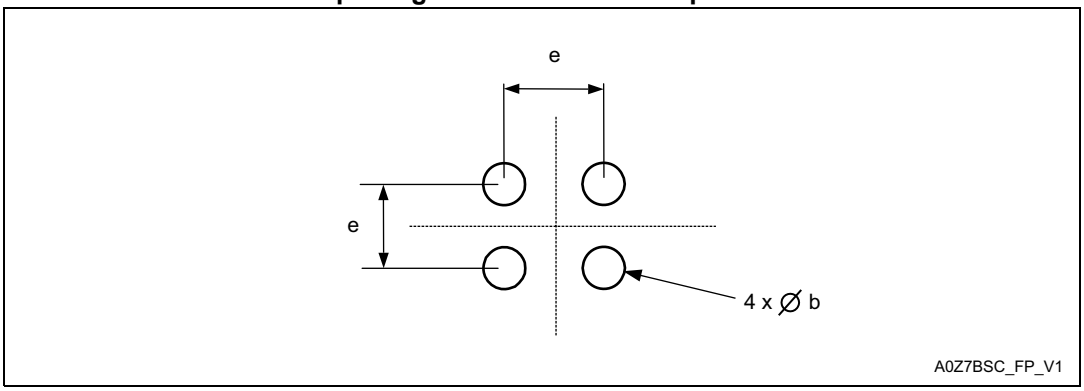
1. Drawing is not to scale.
2. Primary datum Z and seating plane are defined by the spherical crowns of the bump.

Table 24. Ultra Thin WLCSP- 4-bump, 0.795 x 0.674 mm, wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.285	0.315	0.345	0.0112	0.0124	0.0136
A1	-	0.115	-	-	0.0045	-
A2	-	0.175	-	-	0.0069	-
A3 (BSC)	-	0.025	-	-	0.0010	-
b[2] [3]	-	0.160	-	-	0.0063	-
D	-	0.795	0.815	-	0.0313	0.0321
E	-	0.674	0.694	-	0.0265	0.0273
e	-	0.400	-	-	0.0157	-
F	-	0.137	-	-	0.0054	-
G	-	0.198	-	-	0.0078	-
aaa	-	-	0.110	-	-	0.0043
bbb	-	-	0.110	-	-	0.0043
ccc	-	-	0.110	-	-	0.0043
ddd	-	-	0.060	-	-	0.0024
eee	-	-	0.060	-	-	0.0024

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.

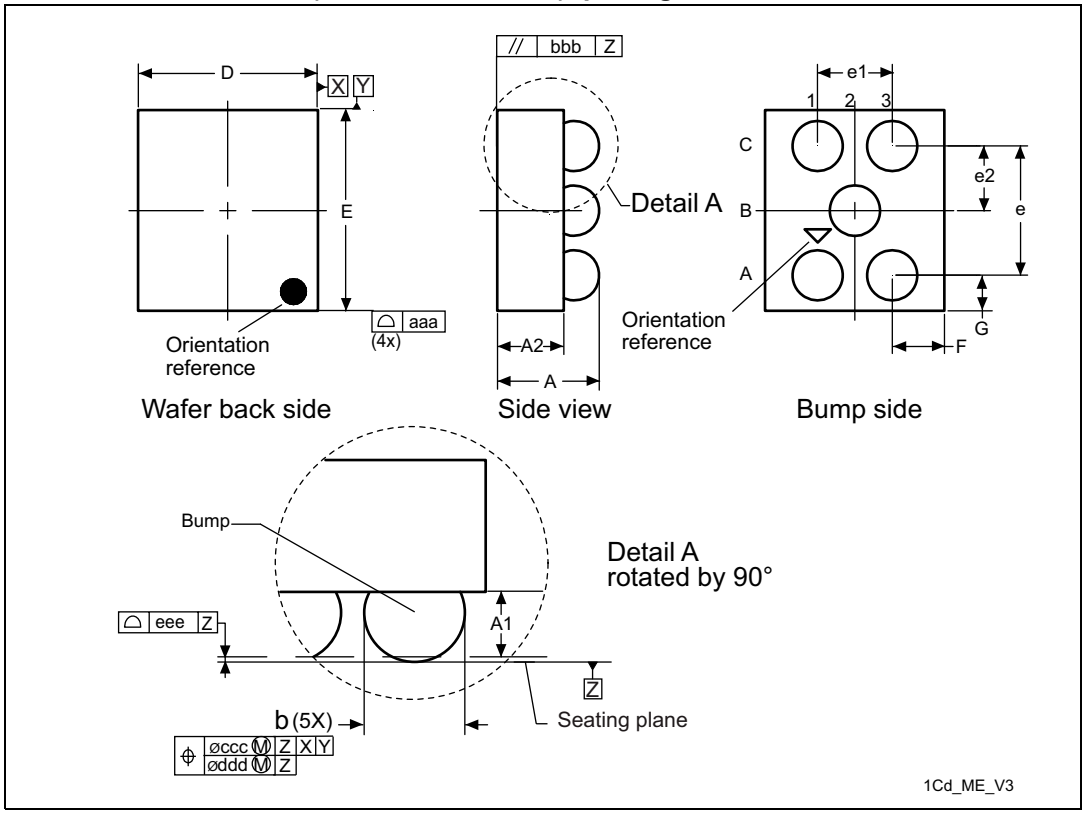
Figure 25. Thin WLCSP- 4-bump, 0.795 x 0.674 mm, wafer level chip scale package recommended footprint



1. Dimensions are expressed in millimeters.

9.7 WLCSP5 package information

Figure 26. WLCSP 5-bump, 0.959 x 1.073 mm, 0.4 mm pitch wafer level chip scale (M24C64-FCS6TP/K)- package outline



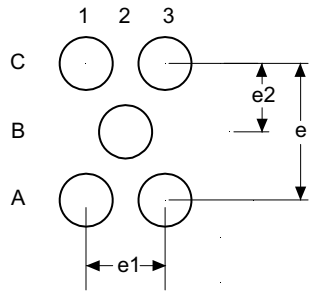
1. Drawing is not to scale.
2. The index on the wafer back side (circle) is above the index of the bump side (triangle/arrow).

Table 25. WLCSP- 5-bump, 0.959 x 1.073 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.455	0.545	0.645	0.0179	0.0215	0.0254
A1	-	0.190	-	-	0.0075	-
A2	-	0.355	-	-	0.0140	-
b[2]	-	0.270	-	-	0.0106	-
D	-	0.959	1.074	-	0.0378	0.0423
E	-	1.073	1.168	-	0.0422	0.0460
e	-	0.693	-	-	0.0273	-
e1	-	0.400	-	-	0.0157	-
e2	-	0.3465	-	-	0.0136	-
F	-	0.280	-	-	0.0110	-
G	-	0.190	-	-	0.0075	-
aaa	-	-	0.110	-	-	0.0043
bbb	-	-	0.110	-	-	0.0043

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

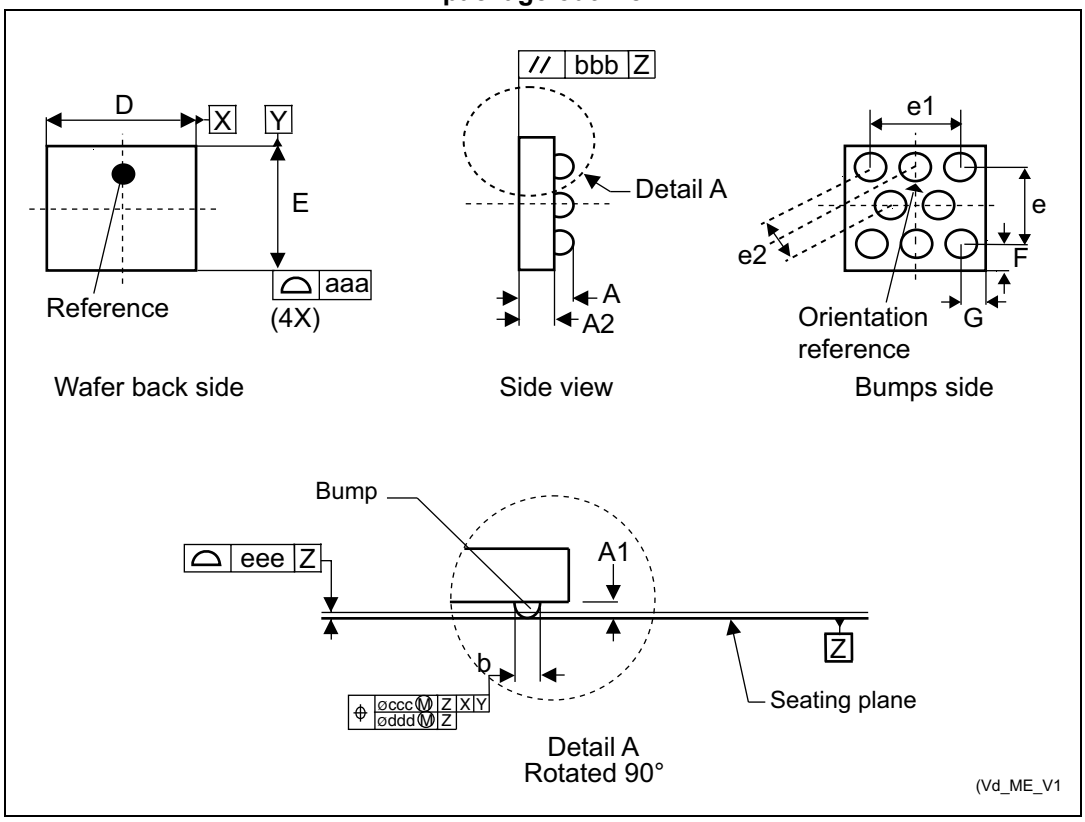
Figure 27. WLCSP - 5-bump, 0.959 x 1.073 mm, 0.4 mm pitch wafer level chip scale recommended footprint



1. Dimensions are expressed in millimeters.

9.8 Thin WLCSP8 package information

Figure 28. Thin WLCSP- 8-bump, 1.073 x 0.959 mm, wafer level chip scale package outline



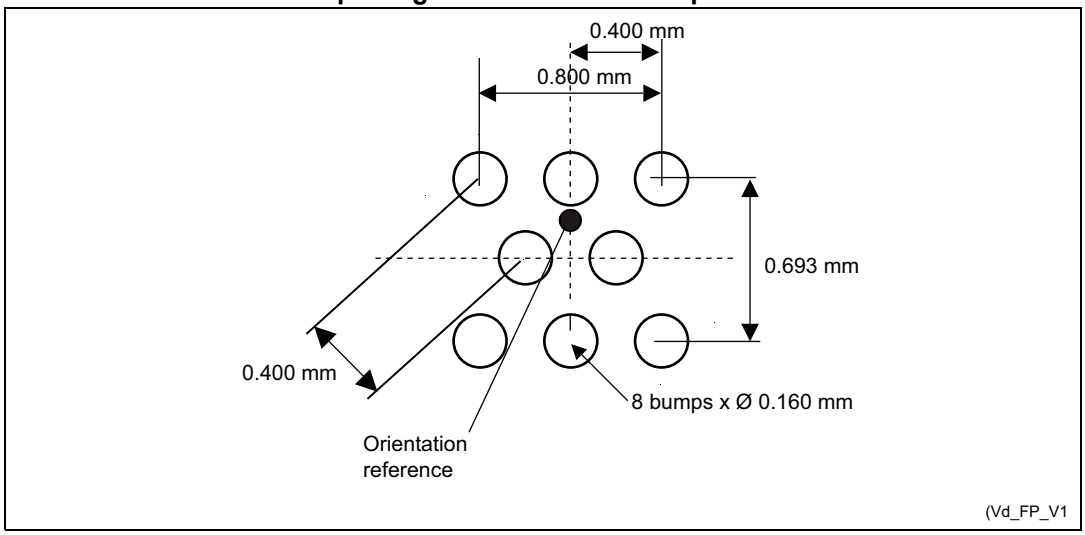
1. Drawing is not to scale.
2. Primary datum Z and seating plane are defined by the spherical crowns of the bump.

Table 26. Thin WLCSP- 8-bump, 1.073 x 0.959 mm, wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.300	0.315	0.330	0.0118	0.0124	0.0130
A1	-	0.115	-	-	0.0045	-
A2	-	0.200	-	-	0.0079	-
b[2]	-	0.160	-	-	0.0063	-
D	-	1.073	0.093	-	0.0422	0.0037
E	-	0.959	0.979	-	0.0378	0.0385
e	-	0.693	-	-	0.0273	-
e1	-	0.800	-	-	0.0315	-
e2	-	0.400	-	-	0.0157	-
F	-	0.133	-	-	0.0052	-
G	-	0.137	-	-	0.0054	-
aaa	-	-	0.110	-	-	0.0043
bbb	-	-	0.110	-	-	0.0043
ccc	-	-	0.110	-	-	0.0043
ddd	-	-	0.060	-	-	0.0024
eee	-	-	0.060	-	-	0.0024

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 29. Thin WLCSP- 8-bump, 1.073 x 0.959 mm, wafer level chip scale package recommended footprint



1. Dimensions are expressed in millimeters.

10 Part numbering

Table 27. Ordering information scheme

Example: M24C64 -D W MC 6 T P /P F

Device type

M24 = I^2C serial access EEPROM

Device function

C64 = 64 Kbit (8192 x 8 bit)

Device family

Blank = Without Identification page

D = With Identification page

Operating voltage

W = VCC = 2.5 V to 5.5 V

R = VCC = 1.8 V to 5.5 V

F = VCC = 1.7 V to 5.5 V

Package

BN = PDIP8(1)

MN = SO8 (150 mil width)(2)

DW = TSSOP8 (169 mil width)(2)

MC = UFDFPN8 (MLP8)(2)

MH = UFDFPN5 (MLP5)(2)

CS = 5-bump WLCSP(2)

CT = 8-bump WLCSP(2)

CU = 4-bump WLCSP

Device grade

6 = Industrial: device tested with standard test flow over –40 to 85 °C

Option

T = Tape and reel packing

blank = tube packing

Plating technology

P or G = ECOPACK2®

Process(3)

/P or /K or /T = Manufacturing technology code

Option

Blank = No Back Side Coating

F = Back Side Coating (WLCSP height = 0.345mm)

1. RoHS-compliant (ECOPACK1®)
2. ECOPACK2® ((RoHS compliant and free of brominated, chlorinated and antimony oxide flame retardants))
3. The process letter is used only when ordering WLCSP packages, the process letter is not specified when ordering any other package. These process letters appear on the device package (marking) and on the shipment box. Please contact your nearest ST Sales Office for further information.

Table 28. Ordering information scheme (unsawn wafer)(1) (2)

Example: M24C64 - F T W 20 I /90

Device type

M24 = I^2C serial access EEPROM

Device function

C64 = 64 Kbit (8192 x 8 bit)

Operating voltage

F = V_{CC} = 1.7 V to 5.5 V

Process

T = F8H+

Delivery form

W = Wafer (bare die)

Wafer thickness

20 = Non-backlapped wafer

Wafer testing

I = Inkless test

Device grade

90 = -40°C to 85°C

1. For all information concerning the M24C64 delivered in unsawn wafer, please contact your nearest ST Sales Office.
2. Unsawn wafer in preview.

Engineering samples

Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

11 Revision history

Table 29. Document revision history

Date	Revision	Changes
14-Mar-2011	22	Updated information concerning E2, E1, E0 for the WLCSP package: – note under *Figure 3: UFDFPN5 package connections* – comment under *Figure 7: Chip enable inputs connection* – note 3 under *Table 2: Device select code*
07-Apr-2011	23	Updated MLP8 package data and *Section 10: Part numbering*Added footnote (a) in *Section 4.5: Memory addressing*.
18-May-2011	24	Updated: – *Figure 3: UFDFPN5 package connections* – *Table 6: Absolute maximum ratings* – *Small text changes* Added: – *Figure 12: Memory cell characteristics*
08-Sep-2011	25	Updated: – *Table 22: UFDFPN8 (MLP8) – 8-lead ultra thin fine pitch dual flat no lead, 2 x 3 mm, data* – *Figure 16: Maximum Rbus value versus bus parasitic capacitance Cbus) for an I2C bus at maximum frequency fC = 1MHz* – *Figure 6: I2C Fast mode Plus (fC = 1 MHz): maximum Rbus value versus bus parasitic capacitance (Cbus)*. Added t_{WLDL} and t_{DHWH} in: – *Table 17: 400 kHz AC characteristics* – *Table 18: 1 MHz AC characteristics* – *Figure :* Minor text changes.
16-Dec-2011	26	Updated A dimension in *Table 25: WLCSP- 5-bump, 0.959 x 1.073 mm, 0.4 mm pitch wafer level chip scale package mechanical data*.

Table 29. Document revision history (continued)

Date	Revision	Changes
28-Aug-2012	27	Datasheet split into: – M24C64-DF, M24C64-W, M24C64-R,M24C64-F (this datasheet) for standard products (range 6), – M24C64-125 datasheet for automotive products (range 3). Added 8-bump thin WLCSP. Updated single supply voltage and number of Write cycles on cover page. Updated *Section 2.1: Serial Clock (SCL)* and *Section 2.2: Serial Data (SDA)*. Updated *Figure 8: Block diagram*. Added *Section 4.5: Device addressing*. *Section 5.1: Write operations* move to *Section 5: Instructions* and updated. Moved *Figure 10: Write mode sequences with WC = 0 (data write enabled)* to *Section 5.1.1: Byte Write*. *Section 5.1.2: Page Write*: changed address bits to A15/A5 and updated *Figure 11*. Case of locked Write identification Page removed from *Section 5.1.4: Lock Identification Page (M24C64-D only)*. Updated *Section 5.1.5: ECC (Error Correction Code) and Write cycling* and move *Figure 12: Write cycle polling flowchart using ACK* to *Section 5.1.6: Minimizing Write delays by polling on ACK*. Added note 1 in *Table 7: Operating conditions (voltage range W)* and *Table 8: Operating conditions (voltage range R)*. Added *Table 12* and updated *Table 13: Memory cell data retention*. Removed note 2 in *Table 17: 400 kHz AC characteristics* for t_{QL1QL2}, t_{WLDL}, t_{DHWH}, and t_{NS}. *Table 27: Ordering information scheme*: removed ambient operating temperature for device grade 5 and added Note *3.* to MLP8 and WLCSP packages.
18-Nov-2013	28	Added text in *Chapter 5.2.2: Current Address Read* Updated note (1) under *Table 6: Absolute maximum ratings*. Removed note (3) in *Table 3: Device select code*. Updated notes below *Table 14: DC characteristics (M24C64-W, device grade 6)* and *Table 15: DC characteristics (M24C64-R device grade 6)* Renamed *Figure 19* and *Table 25*. Updated captions above *Figure 26* and *Figure 24*.

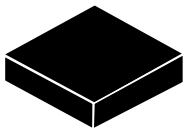
Table 29. Document revision history (continued)

Date	Revision	Changes
21-Jul-2014	29	Updated *Figure 3*, *Figure 6*, *Table 15*, *Table 9*, *Table 17*, *Table 18* and *Table 27*. Updated ECOPACK info on front page. Updated notes: – (1) on *Table 7*, *Table 8*, *Table 14*, *Table 18* – (2) merged with (3) on *Table 15* – (8) on *Table 15* – (2) on *Table 16* – (3) on *Table 27* Added: – note (1) on *Table 9* Added: – supply voltage level specification on Cover page. – package UFDFPN5 on Cover page – *Table 18* and *Figure 18* related to UFDFPN5 package. – Note (1) on *Section 5.1.5*
12-Nov-2014	30	Added: – note 2 on *Table 14* – note 2 on DW, MC and CS package on *Table 27* – note 1on BN package on *Table 27* – *Figure 3* Updated: – *Section 1: Description* – *Chapter 5.1.5* – note 3 on *Table 6* – note 1 on *Table 9* – note 1 on *Table 12* – note 1 on *Table 13* – I_{CC0} max value and note 5 on *Table 14* – I_{CC0} max value on *Table 15* – I_{CC0} max value on *Table 16* – note 2 on *Table 27*
30-Jul-2015	31	Added WLCSP package. Updated *Table 27*.
18-Feb-2016	32	Updated *Figure 4*, *Figure 18*,*Table 19* and added *Table 2*
22-June-2016	33	Added Reference to unsawn wafer inside cover page and added *Table 28: Ordering information scheme (unsawn wafer)*

LSM9DS0

iNEMO inertial module: 3D accelerometer, 3D gyroscope, 3D magnetometer

Datasheet - production data



LGA-24 (4x4x1.0 mm)

Applications

- Indoor navigation
- Smart user interfaces
- Advanced gesture recognition
- Gaming and virtual reality input devices
- Display/map orientation and browsing

Features

- 3 acceleration channels, 3 angular rate channels, 3 magnetic field channels
- ±2/±4/±6/±8/±16 *g* linear acceleration full scale
- ±2/±4/±8/±12 gauss magnetic full scale
- ±245/±500/±2000 dps angular rate full scale
- 16-bit data output
- SPI / I^2C serial interfaces
- Analog supply voltage 2.4 V to 3.6 V
- Power-down mode / low-power mode
- Programmable interrupt generators
- Embedded self-test
- Embedded temperature sensor
- Embedded FIFO
- Position and motion detection functions
- Click/double-click recognition
- Intelligent power saving for handheld devices
- ECOPACK®, RoHS and “Green” compliant

Description

The LSM9DS0 is a system-in-package featuring a 3D digital linear acceleration sensor, a 3D digital angular rate sensor, and a 3D digital magnetic sensor.

The LSM9DS0 has a linear acceleration full scale of ±2*g*/±4*g*/±6g/±8*g*/±16*g,* a magnetic field full scale of ±2/±4/±8/±12 gauss and an angular rate of ±245/±500/±2000 dps.

The LSM9DS0 includes an I^2C serial bus interface supporting standard and fast mode (100 kHz and 400 kHz) and an SPI serial standard interface.

The system can be configured to generate interrupt signals on dedicated pins and is capable of motion and magnetic field detection. Thresholds and timing of interrupt generators are programmable by the end user.

Magnetic, accelerometer and gyroscope sensing can be enabled or set in power-down mode separately for smart power management.

The LSM9DS0 is available in a plastic land grid array package (LGA) and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

Part number	Temperature range [°C]	Package	Packing
LSM9DS0	-40 to +85	LGA-24	Tray
LSM9DS0TR	-40 to +85	LGA-24	Tape and reel

Contents

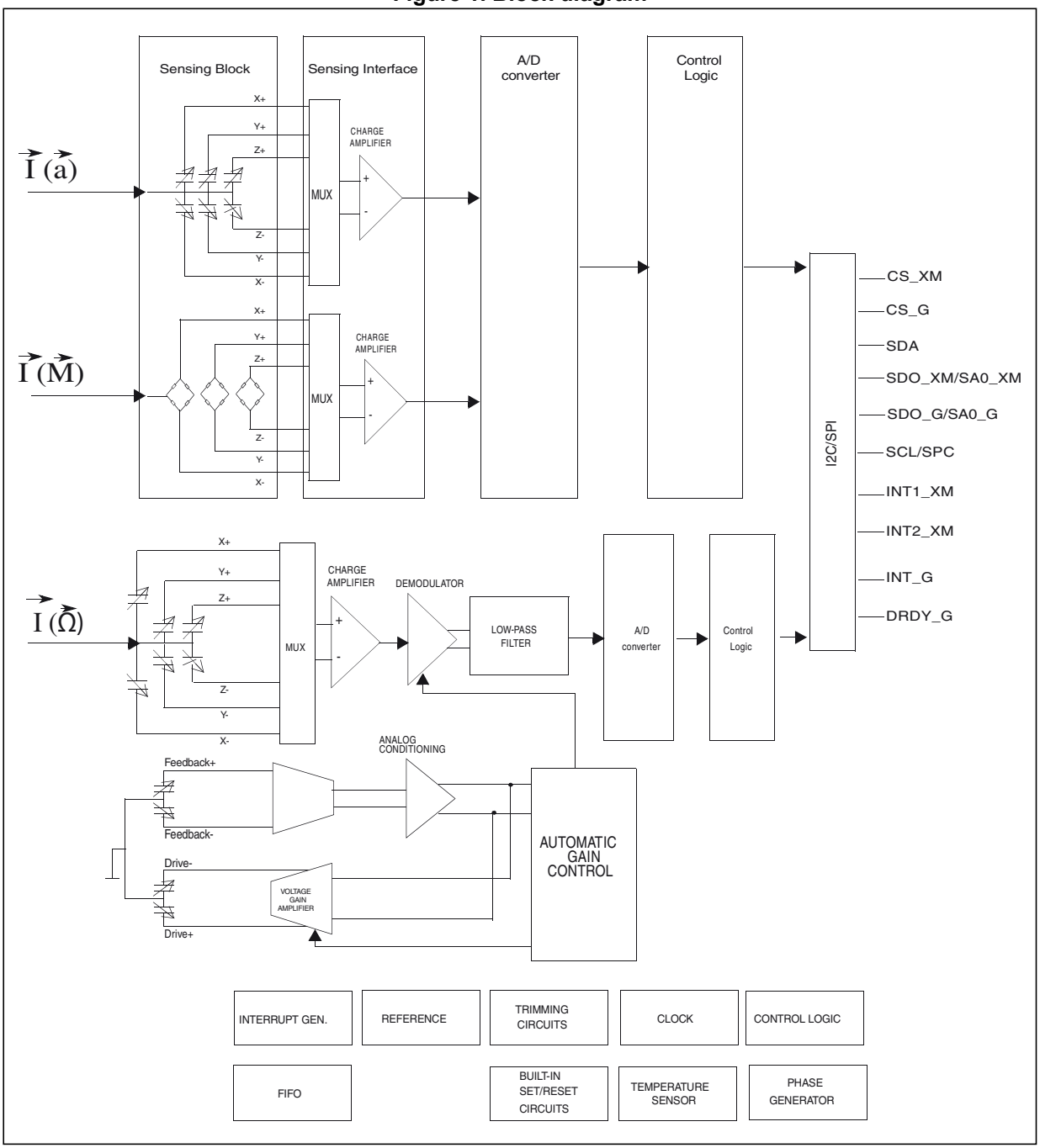
List of tables

List of figures

1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections

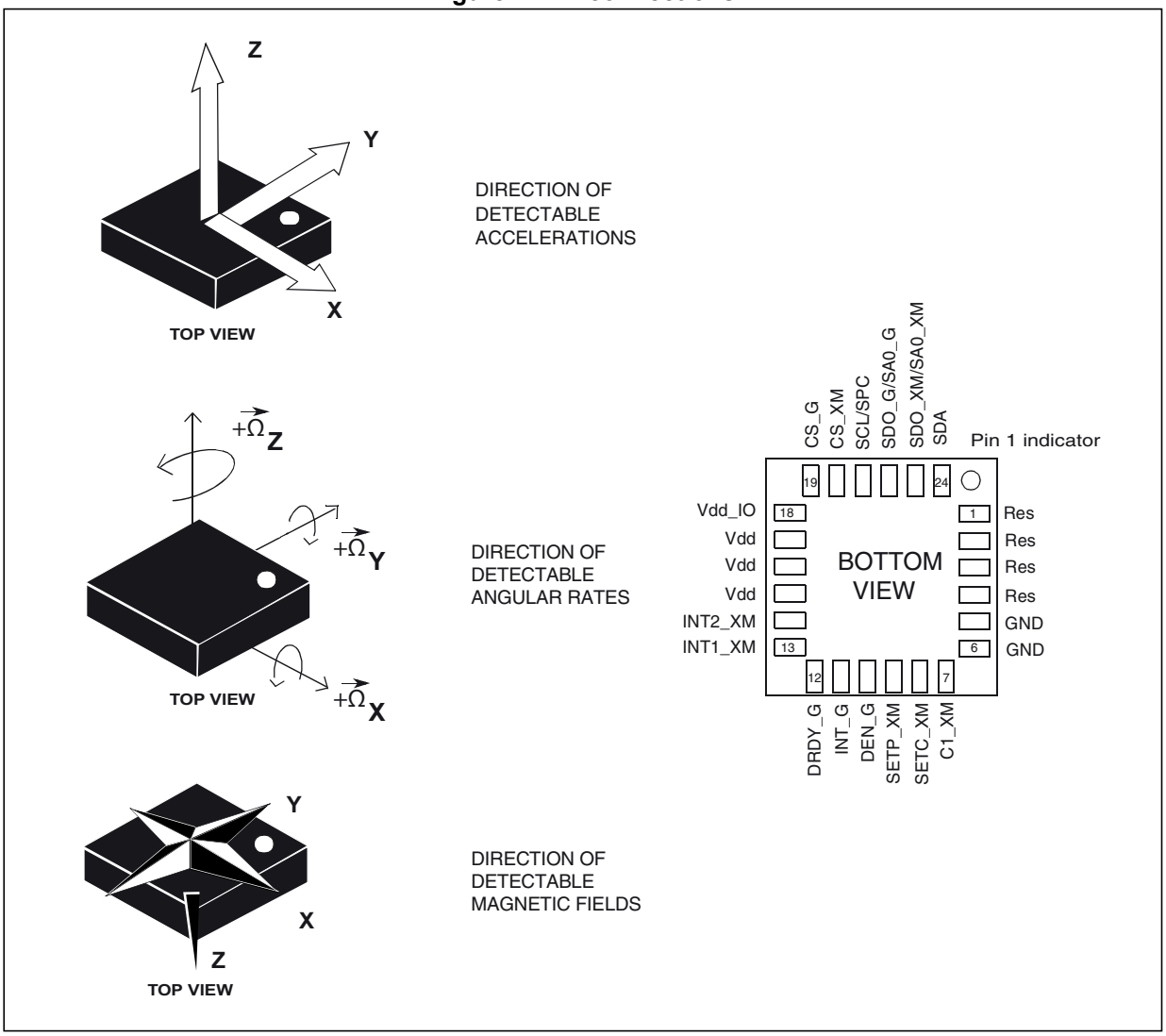


Table 2. Pin description

Pin#	Name	Function
1	Reserved	Leave unconnected
2	Reserved	Connect to GND
3	Reserved	Connect to GND
4	Reserved	Connect to GND
5	GND	0 V supply
6	GND	0 V supply
7	C1_XM	Capacitor connection (C1)
8	SETC_XM	S/R capacitor connection (C2)
9	SETP_XM	S/R capacitor connection (C2)
10	DEN_G	Gyroscope data enable
11	INT_G	Gyroscope programmable interrupt
12	DRDY_G	Gyroscope data ready
13	INT1_XM	Accelerometer and magnetic sensor interrupt 1
14	INT2_XM	Accelerometer and magnetic sensor interrupt 2
15	Vdd	Power supply
16	Vdd	Power supply
17	Vdd	Power supply
18	Vdd_IO	Power supply for I/O pins
19	CS_G	Gyroscope I^2C/SPI mode selection 1: SPI idle mode / I^2C communication enabled 0: SPI communication mode / I^2C disabled
20	CS_XM	Accelerometer and magnetic sensor SPI enabled I^2C/SPI mode selection 1: SPI idle mode / I^2C communication enabled 0: SPI communication mode / I^2C disabled
21	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
22	SDO_G SA0_G	Gyroscope serial data output (SDO) Angular rate sensor I^2C less significant bit of the device address (SA0)
23	SDO_XM SA0_XM	Accelerometer and magnetic sensor SPI serial data output (SDO) Accelerometer and magnetic sensor I^2C less significant bit of the device address (SA0)
24	SDA	I^2C serial data (SDA)

2 Module specifications

2.1 Sensor characteristics

@ Vdd = 3.0 V, T = 25 °C unless otherwise noted[a]

Table 3. Sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
LA_FS	Linear acceleration measurement range[2]			±2		g
				±4		
				±6		
				±8		
				±16		
M_FS	Magnetic measurement range			±2		gauss
				±4		
				±8		
				±12		
G_FS	Angular rate measurement range			±245		dps
				±500		
				±2000		
LA_So	Linear acceleration sensitivity	Linear acceleration FS = ±2 *g*		0.061		mg/LSB
		Linear acceleration FS = ±4 *g*		0.122		
		Linear acceleration FS = ±6 *g*		0.183		
		Linear acceleration FS = ±8 *g*		0.244		
		Linear acceleration FS = ±16 *g*		0.732		
M_GN	Magnetic sensitivity	Magnetic FS = ±2 gauss		0.08		mgauss/ LSB
		Magnetic FS = ±4 gauss		0.16		
		Magnetic FS = ±8 gauss		0.32		
		Magnetic FS = ±12 gauss		0.48		
G_So	Angular rate sensitivity	Angular rate FS = ±245 dps		8.75		mdps/ digit
		Angular rate FS = ±500 dps		17.50		
		Angular rate FS = ±2000 dps		70		
LA_TCSo	Linear acceleration sensitivity change vs. temperature	From -40 °C to +85 °C		±1.5		%
M_TCSo	Magnetic sensitivity change vs. temperature	From -40 °C to +85 °C		±3		%

a. The product is factory calibrated at 3.0 V. The operational power supply range is from 2.4 V to 3.6 V.

Table 3. Sensor characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
G_SoDr	Angular rate sensitivity change vs. temperature	From -40 °C to +85 °C		±2		%
LA_TyOff	Linear acceleration typical zero-g level offset accuracy(3)(4)			±60		mg
G_TyOff	Angular rate typical zero-rate level	FS = 245 dps		±10		dps
		FS = 500 dps		±15		
		FS = 2000 dps		±25		
LA_TCOff	Linear acceleration zero-g level change vs. temperature	Max delta from 25 °C		±0.5		mg/°C
G_TCOff	Zero-rate level change vs. temperature			±0.05		dps/°C
M_EF	Maximum exposed field	No perming effect on zero reading			10000	gauss
M_DF	Magnetic disturbing field	Sensitivity starts to degrade. Automatic S/R pulse restores the sensitivity(5)			20	gauss
LA_ST	Linear acceleration self-test positive difference (6)(7)	±2 *g* range, X, Y, Z-axis AST1:0 = 01 see *Table 74*	60		1700	mg
G_ST	Angular rate self-test output change (8)(9)	FS = 245 dps	20		250	dps
		FS = 500 dps	70		400	
		FS = 2000 dps	150		1000	
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed
2. Verified by wafer level test and measurement of initial offset and sensitivity
3. Typical zero-*g* level offset value after MSL3 preconditioning
4. Offset can be eliminated by enabling the built-in high-pass filter
5. Set / Reset Pulse is automatically applied at each conversion cycle
6. “Self-test output change” is defined as: OUTPUT[mg]$_{(}$*CTRL_REG2_XM (21h)* $_{\text{AST1:0 enabled)}}$ - OUTPUT[mg]$_{(}$*CTRL_REG2_XM (21h)* $_{\text{AST1:0 disabled)}}$
7. For polarity refer to *Table 77: Self-test mode configuration*
8. “Self-test output change” is defined as: OUTPUT[mg]$_{(}$*CTRL_REG4_G (23h)* $_{\text{ST1:0 enabled)}}$ - OUTPUT[mg]$_{(}$*CTRL_REG4_G (23h)* ST1:0 disabled)
9. For polarity refer to *Table 31: Self-test mode configuration*

2.2 Temperature sensor characteristics

The electrical characteristics concerning the temperature sensor are given in the table below.

@ Vdd = 3.0 V, T=25 °C unless otherwise noted.

Table 4. Temperature sensor electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
TSDr	Temperature sensor output change vs. temperature	-		8		LSB/°C
TODR	Temperature refresh rate			M_ODR [2:0](2)		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Refer to *Table 84: Magnetic data rate configuration*.

2.3 Electrical characteristics

@ Vdd = 3.0V, T = 25 °C unless otherwise noted[b]

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		2.4		3.6	V
Vdd_IO	Module power supply for I/O		1.71	1.8	Vdd+0.1	
Idd_XM	Current consumption of the accelerometer and magnetic sensor in normal mode (2)		HR setting CTRL_REG5_XM (M_RES [1,0]) = 11b, see *CTRL_REG5_XM (24h)*	350		µA
Idd_G	Gyroscope current consumption in normal mode(3)			6.1		mA
Idd_G_LP	Gyroscope supply current in sleep mode(4)			2		mA
Idd_Pdn	Current consumption in power-down mode(5)			6		µA
VIH	Digital high-level input voltage		0.8*Vdd_IO			V
VIL	Digital low-level input voltage				0.2*Vdd_IO	V
VOH	High-level output voltage		0.9*Vdd_IO			V
VOL	Low-level output voltage				0.1*Vdd_IO	V
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed
2. Magnetic sensor setting ODR =6.25 Hz, Accelerometer sensor ODR =50 Hz, gyroscope in power-down mode
3. Accelerometer and magnetic sensor in power-down mode
4. Sleep mode introduces a faster turn-on time compared to power-down mode. Accelerometer and magnetic sensor in power-down mode.
5. Linear accelerometer, magnetic sensor and gyroscope in power-down mode

b. LSM9DS0 is factory calibrated at 3.0 V

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

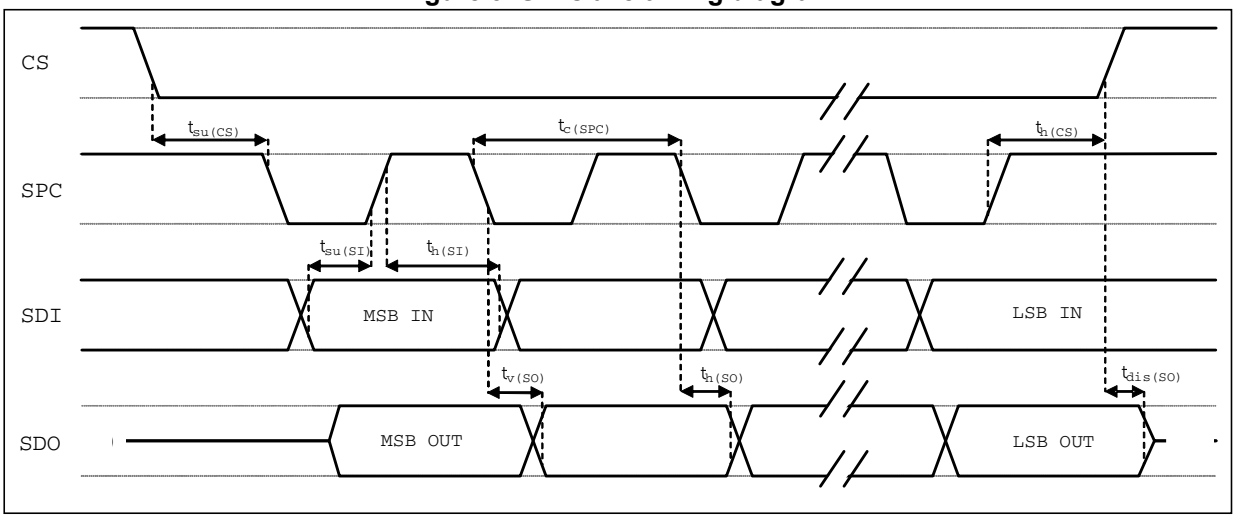
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	5		ns
$t_{h(CS)}$	CS hold time	20		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	5		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 Sensor I²C - inter-IC control interface

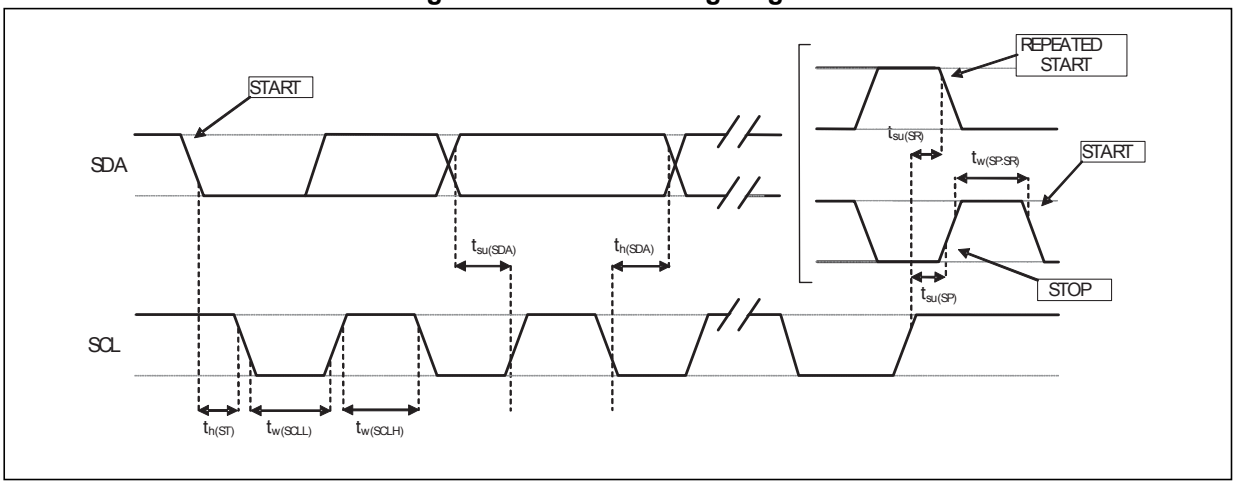
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (SCL/SPC, SDA, SDO_XM/SA0_XM, SDO_G/SA0_G, CS_G, CS_XM, DEN_G)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 2.5 V)	3,000 for 0.5 ms	g
		10,000 for 0.1 ms	g
A_{UNP}	Acceleration (any axis, unpowered)	3,000 for 0.5 ms	g
		10,000 for 0.1 ms	g
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This is an electrostatic-sensitive device (ESD), improper handling can cause permanent damage to the part.

3 Terminology

3.1 Set / reset pulse

The set / reset pulse is an automatic operation performed before each magnetic acquisition cycle to degauss the sensor and to ensure alignment of the magnetic dipoles and thus the linearity of the sensor itself.

3.2 Sensitivity

The methods to determine sensitivity and offset are given below in the following paragraphs.

3.2.1 Linear acceleration sensor sensitivity

Sensitivity describes the gain of the sensor and can be determined by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

3.2.2 Magnetic sensor sensitivity

Sensitivity describes the gain of the sensor and can be determined by applying a magnetic field of 1 *gauss* to it.

3.2.3 Angular rate sensitivity

An angular rate gyroscope is a device that produces a positive-going digital output for counter-clockwise rotation around the sensitive axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

3.2.4 Zero-*g* level

The zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* for the X-axis and 0 *g* for the Y-axis whereas the Z-axis will measure 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called Zero-*g* offset. Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-*g* level change vs. temperature" (LA_TCOff in *Table 3*). The Zero-*g* level tolerance (TyOff) describes the standard deviation of the range of Zero-*g* levels of a population of sensors.

3.2.5 Zero-*gauss* level

The zero-*g*auss level offset describes the deviation of an actual output signal from the ideal output if no magnetic field is present. Thanks to the Set/Reset Pulse and to the magnetic sensor readout chain, the offset is dynamically cancelled. The Zero-*g*auss level does not show any dependency on temperature or power supply.

3.2.6 Zero-rate level

The zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of highly accurate MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

4 Functionality

The LSM9DS0 is a system-in-package featuring a 3D digital accelerometer, a 3D digital magnetometer, and a 3D digital gyroscope.

The device includes specific sensing elements and two IC interfaces capable of measuring both the acceleration/magnetometer and angular rate applied to the module and to provide a signal to external applications through an SPI/I^2C serial interface.

The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using a CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LSM9DS0 may also be configured to generate an inertial *wake-up* and *free-fall* interrupt signal according to a programmed acceleration event along the enabled axes.

4.1 Self-test

4.1.1 Accelerometer

The self-test allows the linear acceleration sensor functionality to be tested without moving it. The self-test function is off when the self-test bit (ST) is programmed to ‘0’. When the self-test bit is programmed to ‘1’ an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified inside *Section 2.1: Sensor characteristics*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

4.1.2 Gyroscope

The self-test allows to test the mechanical and electric part of the sensor, allowing the seismic mass to be moved by means of an electrostatic test-force. When the ST is activated by the IC, an actuation force is applied to the sensor, emulating a definite Coriolis force. In this case the sensor output will exhibit an output change.
When the ST is active, the device output is given by the algebraic sum of the signals produced by the velocity acting on the sensor and by the electrostatic test-force.

For polarity please refer to *Table 31: Self-test mode configuration*.

4.2 Linear acceleration main digital blocks

4.2.1 FIFO

The LSM9DS0 embeds 32 slots of data FIFO for each of the three output channels: X, Y and Z. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed

and burst the significant data out from the FIFO. This buffer can work accordingly in four different modes: Bypass mode, FIFO mode, Stream mode and Stream-to-FIFO mode. Each mode is selected by the FIFO_MODE bits in *FIFO_SRC_REG (2Fh)*. Programmable watermark level, FIFO_Empty or FIFO_Full events can be enabled to generate dedicated interrupts on the INT1_XM/INT2_XM pin (configured through *FIFO_SRC_REG (2Fh)*).

4.2.2 Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. For each channel only the first address is used. The remaining FIFO slots are empty.

4.2.3 FIFO mode

In FIFO mode, data from the X, Y and Z channels are stored in the FIFO. A watermark interrupt can be enabled (FIFO_WTMK_EN bit in *FIFO_CTRL_REG (2Eh)*) in order to be raised when the FIFO is filled to the level specified in the FIFO_WTMK_LEVEL bits of *FIFO_CTRL_REG (2Eh)*. The FIFO continues filling until it is full (32 slots of data for X, Y and Z). When full, the FIFO stops collecting data from the input channels.

4.2.4 Stream mode

In Stream mode, data from the X, Y and Z measurements are stored in the FIFO. A watermark interrupt can be enabled and set as in FIFO mode. The FIFO continues filling until it is full (32 slots of data for X, Y and Z). When full, the FIFO discards the older data as the new data arrives.

4.2.5 Stream-to-FIFO mode

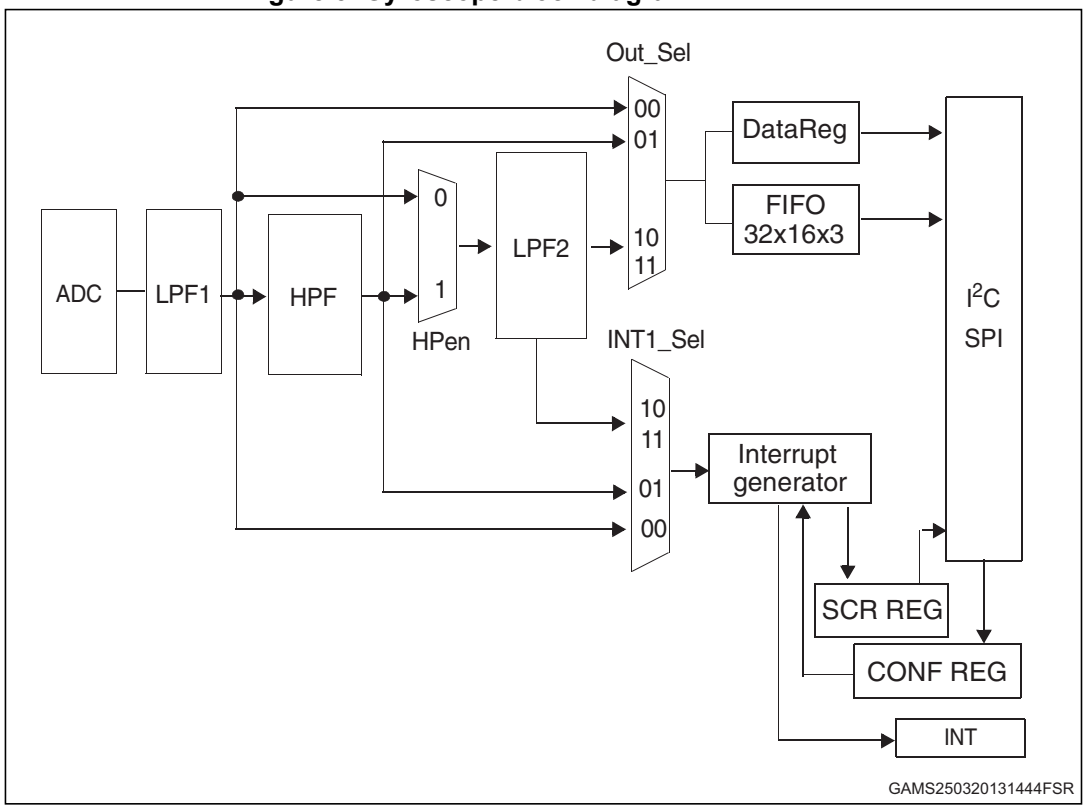
In Stream-to-FIFO mode, data from the X, Y and Z measurements is stored in the FIFO. A watermark interrupt can be enabled (FIFO_WTMK_EN bit in *FIFO_CTRL_REG (2Eh)*) in order to be raised when the FIFO is filled to the level specified in the FIFO_WTMK_LEVEL bits of *FIFO_CTRL_REG (2Eh)*. The FIFO continues filling until it is full (32 slots of 8-bit data for X, Y and Z). When full, the FIFO discards the older data as the data new arrives. Once a trigger event occurs, the FIFO starts operating in FIFO mode.

4.2.6 Retrieving data from FIFO

A read operation to the *OUT_X_L_A (28h), OUT_X_H_A (29h)*, *OUT_Y_L_A (2Ah), OUT_Y_H_A (2Bh)* or *OUT_Z_L_A (2Ch), OUT_Z_H_A (2Dh)* registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest X, Y and Z data are placed in the *OUT_X_L_A (28h), OUT_X_H_A (29h)*, *OUT_Y_L_A (2Ah), OUT_Y_H_A (2Bh)* and *OUT_Z_L_A (2Ch), OUT_Z_H_A (2Dh)* registers and both single read and read_burst operations can be used.

4.3 Gyroscope digital main blocks

Figure 5. Gyroscope block diagram



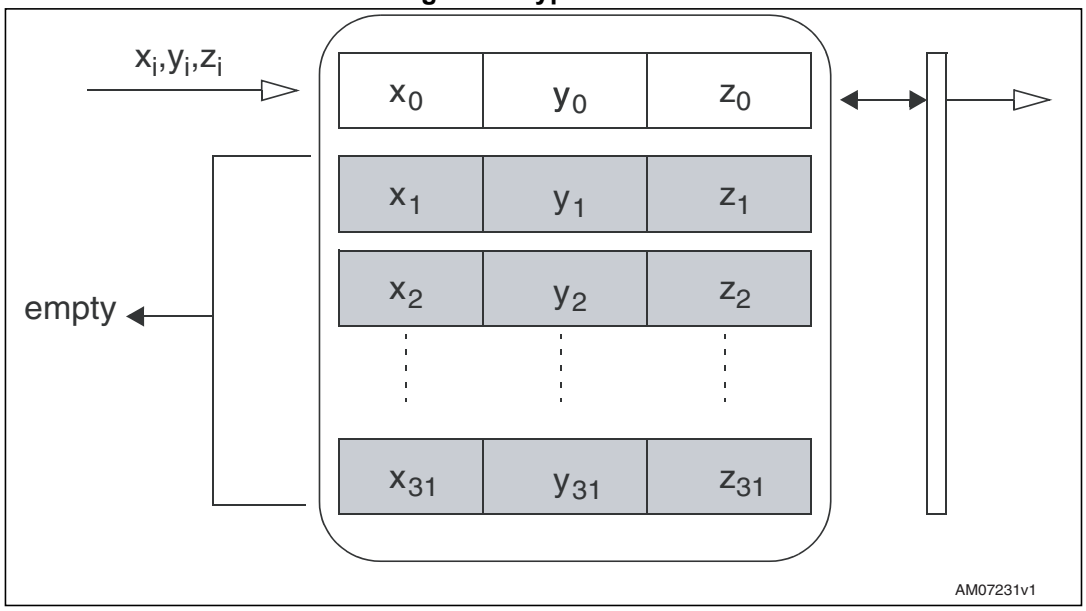
4.3.1 FIFO

The LSM9DS0 embeds 32 slots of 16-bit data FIFO for each of the three output channels: yaw, pitch and roll. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but can wake up only when needed and burst the significant data out from the FIFO. This buffer can work accordingly in five different modes: Bypass mode, FIFO mode, Stream mode, Bypass-to-Stream mode and Stream-to-FIFO mode. Each mode is selected by the FIFO_MODE bits in *FIFO_CTRL_REG_G (2Eh)*. A programmable watermark level, FIFO_Empty or FIFO_Full events can be enabled to generate dedicated interrupts on the DRDY_G pin (configured through *CTRL_REG3_G (22h)* and event detection information is available in *FIFO_SRC_REG_G (2Fh)*. The watermark level can be configured to WTM4:0 in *FIFO_CTRL_REG_G (2Eh)*.

4.3.2 Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. As described in *Figure 6*, for each channel only the first address is used. The remaining FIFO slots are empty. When new data is available, the old data is overwritten.

Figure 6. Bypass mode

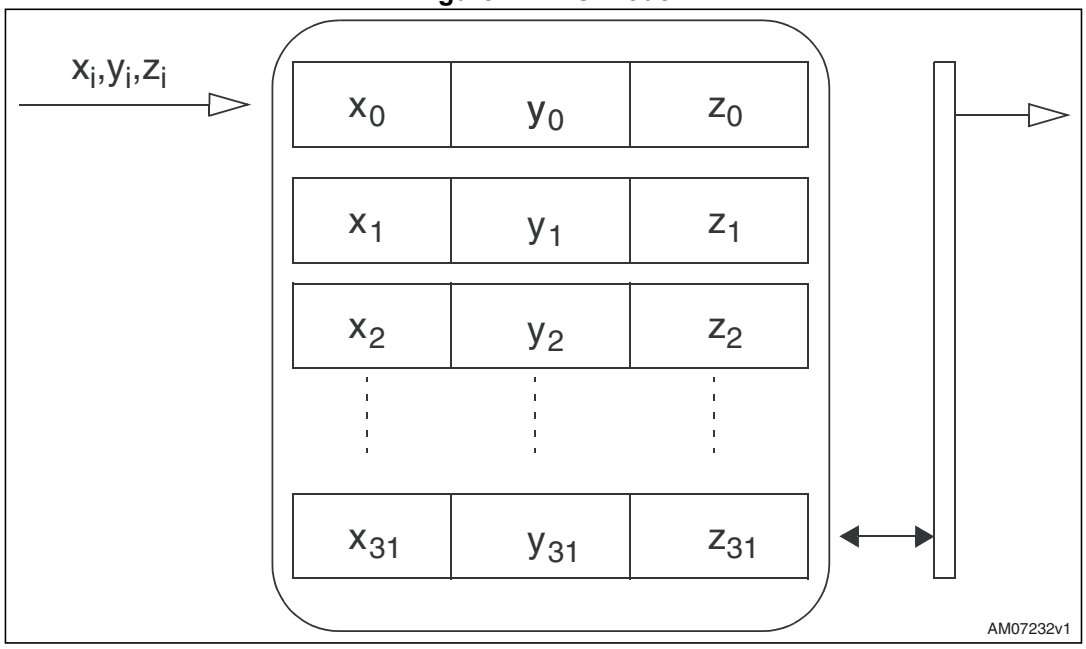


4.3.3 FIFO mode

In FIFO mode, data from the yaw, pitch and roll channels is stored in the FIFO. A watermark interrupt can be enabled (I2_WMK bit in *CTRL_REG3_G (22h)*) in order to be raised when the FIFO is filled to the level specified in the WTM 4:0 bits of *FIFO_CTRL_REG_G (2Eh)*. The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO stops collecting data from the input channels. To restart data collection, *FIFO_CTRL_REG_G (2Eh)* must be written back to Bypass mode.

FIFO mode is represented in *Figure 7*.

Figure 7. FIFO mode

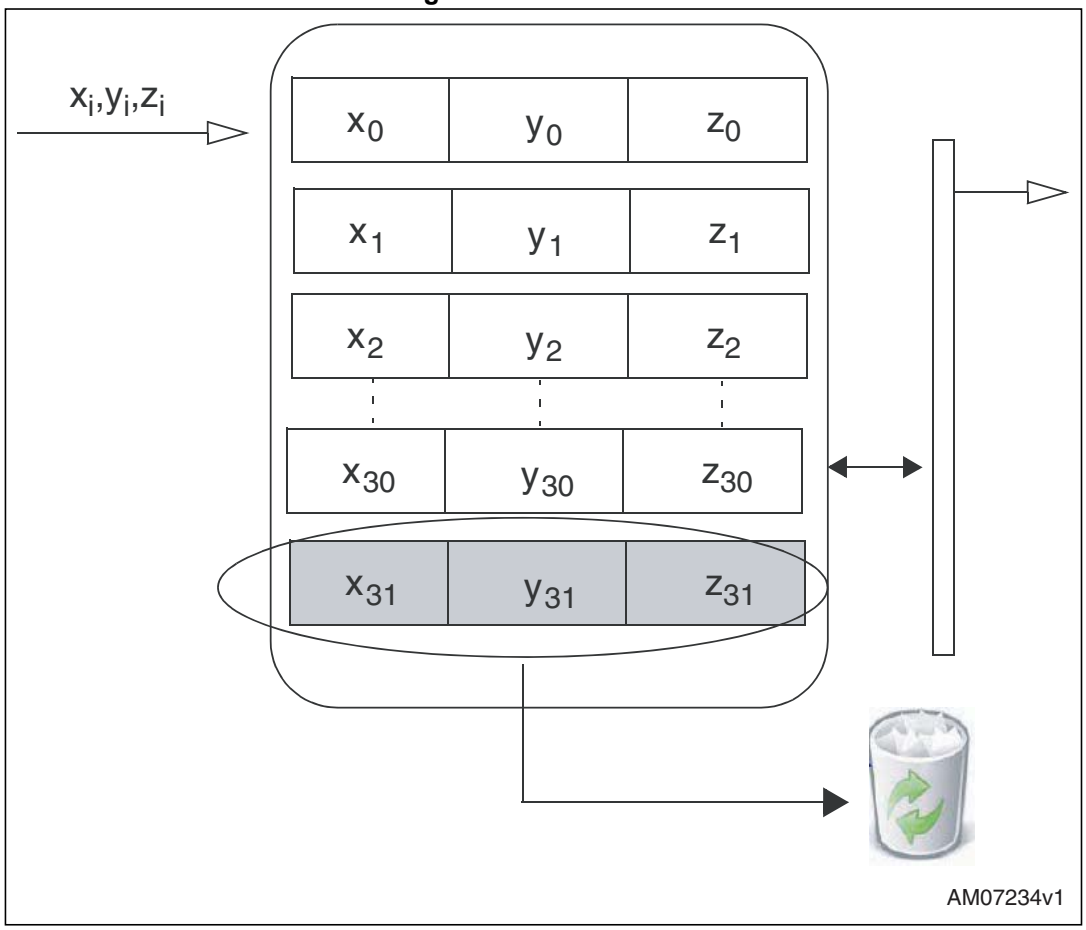


4.3.4 Stream mode

In Stream mode, data from the yaw, pitch and roll measurements is stored in the FIFO. A watermark interrupt can be enabled and set as in FIFO mode. The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO discards the older data as the new data arrives. Programmable watermark level events can be enabled to generate dedicated interrupts on the DRDY_G pin (configured through *CTRL_REG3_G (22h)*.

Stream mode is represented in *Figure 8*.

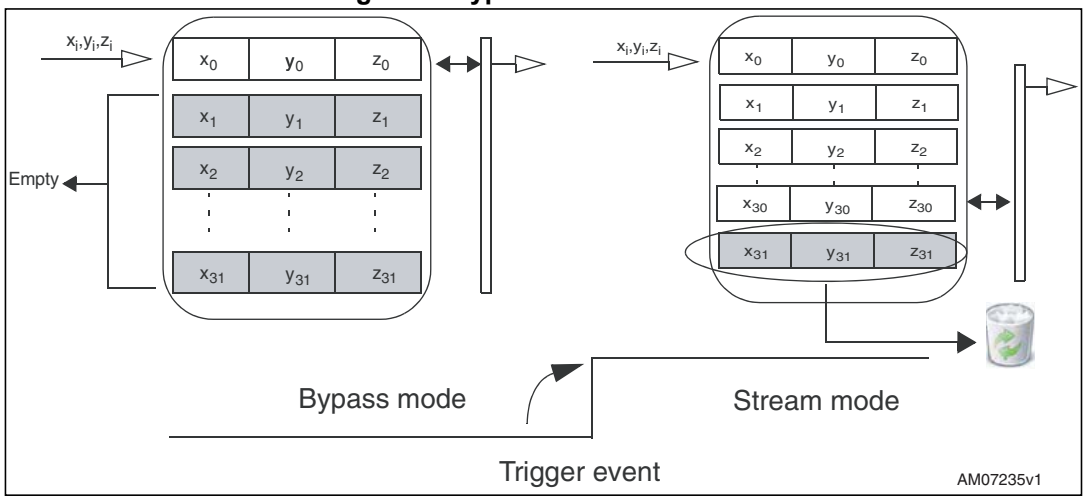
Figure 8. Stream mode



4.3.5 Bypass-to-stream mode

In Bypass-to-stream mode, the FIFO starts operating in Bypass mode and once a trigger event occurs (related to *INT1_CFG_G (30h)* events) the FIFO starts operating in Stream mode. Refer to *Figure 9* below.

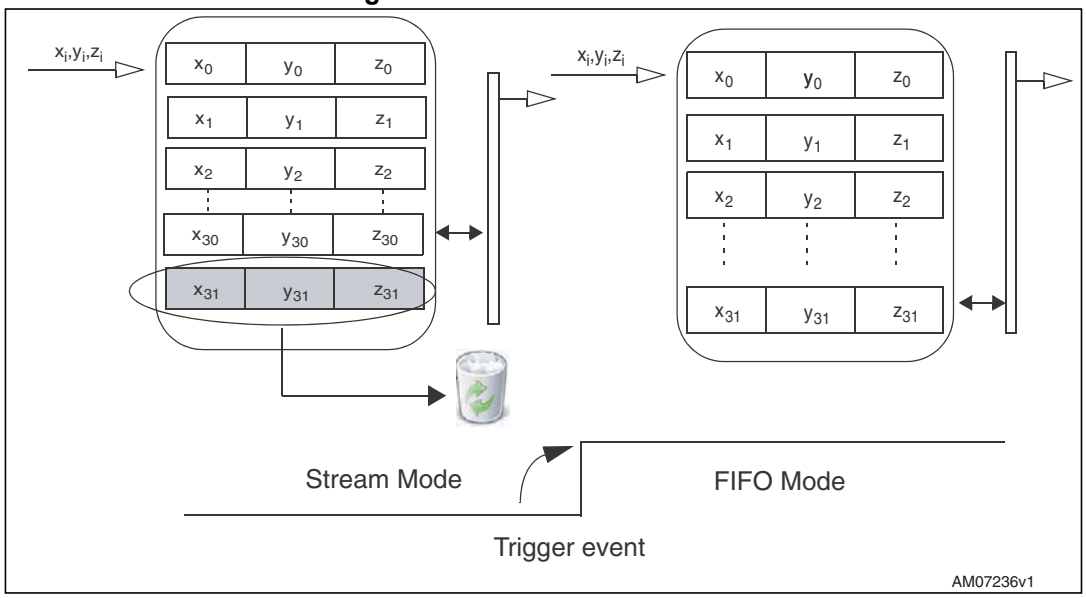
Figure 9. Bypass-to-stream mode



4.3.6 Stream-to-FIFO mode

In Stream-to-FIFO mode, data from the yaw, pitch and roll measurement is stored in the FIFO. A watermark interrupt can be enabled on pin DRDY_G by setting the I2_WTM bit in *CTRL_REG3_G (22h)* to be raised when the FIFO is filled to the level specified in the WTM4:0 bits of *FIFO_CTRL_REG_G (2Eh)*. The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO discards the older data as the new data arrives. Once a trigger event occurs (related to *INT1_CFG_G (30h)* events), the FIFO starts operating in FIFO mode. Refer to *Figure 10*.

Figure 10. Stream-to-FIFO mode



4.3.7 Retrieving data from FIFO

A read operation from the *OUT_X_L_G (28h), OUT_X_H_G (29h)*, *OUT_Y_L_G (2Ah), OUT_Y_H_G (2Bh)* or *OUT_Z_L_G (2Ch), OUT_Z_H_G (2Dh)* registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest pitch, roll and yaw data are placed in the *OUT_X_L_G (28h), OUT_X_H_G (29h)*, *OUT_Y_L_G (2Ah), OUT_Y_H_G (2Bh)* and *OUT_Z_L_G (2Ch), OUT_Z_H_G (2Dh)* registers and both single read and read_burst (X,Y & Z with auto-incremental address) operations can be used. When data included in *OUT_Z_H_G* is read, the system again starts to read information from addr *OUT_X_L_G*.

4.4 Temperature sensor

The LSM9DS0 features an embedded temperature sensor.

Temperature data can be enabled by setting the TEMP_EN bit in the *CTRL_REG5_XM (24h)* register to 1.

Both OUT_TEMP_H_XM and OUT_TEMP_L_XM registers must be read.

Temperature data is stored inside *OUT_TEMP_L_XM (05h), OUT_TEMP_H_XM (06h)* as two's complement data in 12-bit format, right justified.

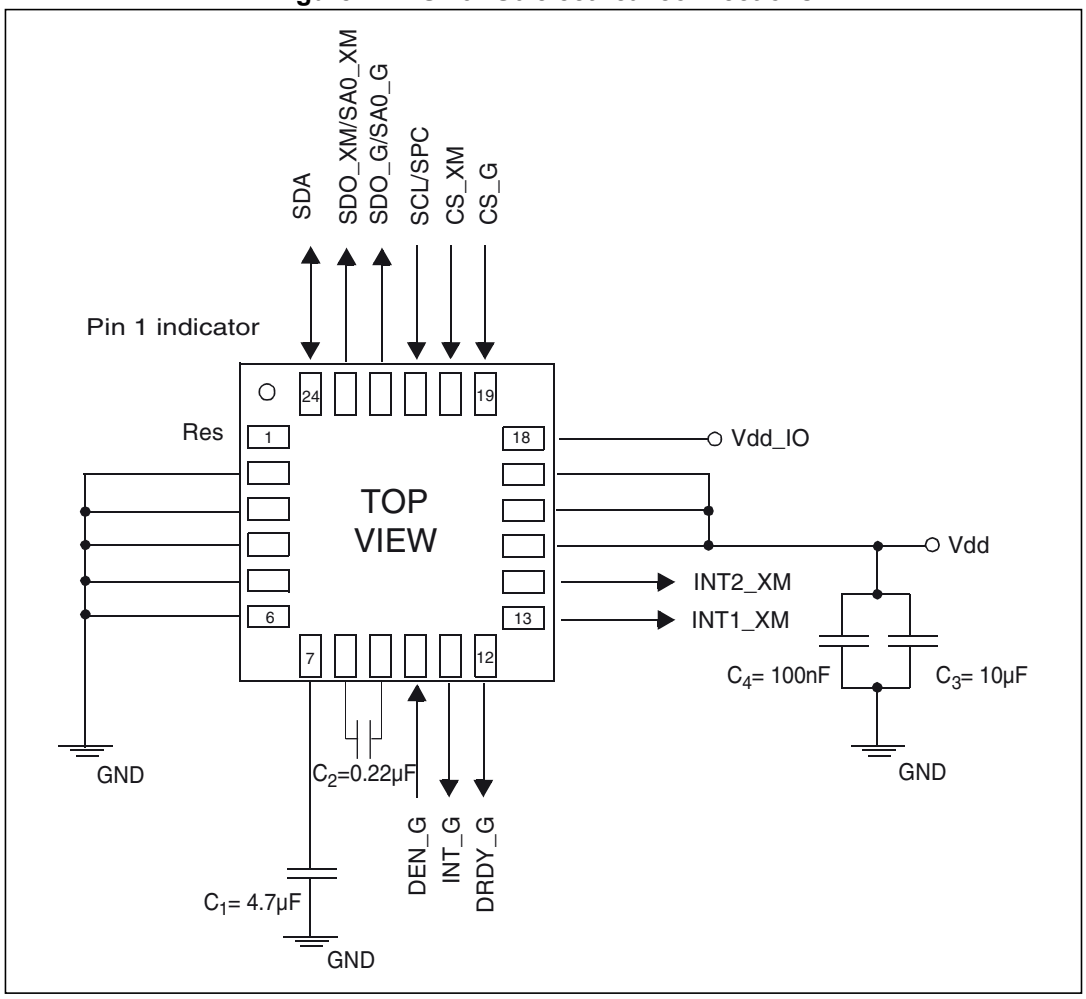
The output data rate of the temperature sensor is set by M_ODR in *CTRL_REG5_XM (24h)* and is equal to the magnetic sensor output data rate.

4.5 Factory calibration

The IC interface is factory calibrated. The trimming values are stored inside the non-volatile memory of the device. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during normal operation. This allows the using the device without further calibration.

5 Application hints

Figure 11. LSM9DS0 electrical connections



5.1 External capacitors

The C1 and C2 external capacitors should be low SR value, ceramic type construction (typ recommended value 200 mOhm). Reservoir capacitor C1 is nominally 4.7 µF in capacitance, with the set/reset capacitor C2 nominally 0.22 µF in capacitance.

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C4 = 100 nF ceramic, C3 = 10 µF Al) should be placed as near as possible to the supply pin of the device (common design practice). All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 11*).

The functions of the device and the measured acceleration/magnetic field data are selectable and accessible through the I^2C / SPI interfaces.

The functions, the threshold and the timing of the three interrupt pins (INT_G, INT1_XM and INT2_XM) can be completely programmed by the user through the I^2C / SPI interfaces.

5.2 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendation are available at www.st.com/mems.

5.3 High current wiring effects

High current in wiring and printed circuit traces can be culprits in causing errors in magnetic field measurements for compassing.

Conductor-generated magnetic fields will add to the Earth’s magnetic field leading to errors in compass-heading computation.

Keep currents higher than 10 mA a few millimeters further away from the sensor IC.

6 Digital interfaces

The registers embedded in the LSM9DS0 may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW-configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped to the same pins. To select/exploit the I^2C interface, the CS line must be tied high (i.e connected to Vdd_IO).

Table 9. Serial interface pin description

Pin name	Pin description
CS	I^2C/SPI mode selection 1: SPI idle mode / I^2C communication enabled 0: SPI communication mode / I^2C disabled
SCL/SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA/SDI/SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO	SPI serial data output (SDO) I^2C less significant bit of the device address

6.1 I^2C serial interface

The LSM9DS0 I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 10. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines must be connected to Vdd_IO through external pull-up resistors. When the bus is free, both lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with normal mode.

6.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its own address. If they match, the device considers itself addressed by the master.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LSM9DS0 behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) will be transmitted: the 7 LSb represents the actual register address while the MSB enables the address auto increment. If the MSb of the SUB field is ‘1’, the SUB (register address) will be automatically increased to allow multiple data read/writes.

Table 11. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 12. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 13. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 14. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DAT A		DAT A		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can’t receive another complete byte of data until it has performed

some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of first register to be read.

In the presented communication format MAK is Master Acknowledge and NMAK is No Master Acknowledge.

Default address:

The **SDO**/**SA0** pins (SDO_XM/SA0_XM or SDO_G/SA0_G) can be used to modify the least significant bit of the device address. If the SA0 pin is connected to the voltage supply, LSb is '1' (ex. address 0011101b) else if SA0 pad is connected to ground, the LSb value is '0' (ex. address 0011110b).

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition will have to be issued after the two sub-address bytes; if the bit is '0' (Write) the master will transmit to the slave with the direction unchanged. *Table 15* and *Table 16* explain how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Linear acceleration and magnetic sensor address:

Table 15. Linear acceleration and magnetic sensor SAD+read/write patterns

Command	SDO_XM/SA0_XM pin	SAD[6:2]	SAD[1:0]	R/W	SAD+R/W
Read	0	00111	10	1	00111101 (3D)
Write	0	00111	10	0	00111100 (3C)
Read	1	00111	01	1	00111011 (3B)
Write	1	00111	01	0	00111010 (3A)

Angular rate sensor address:

Table 16. Angular rate SAD+read/write patterns

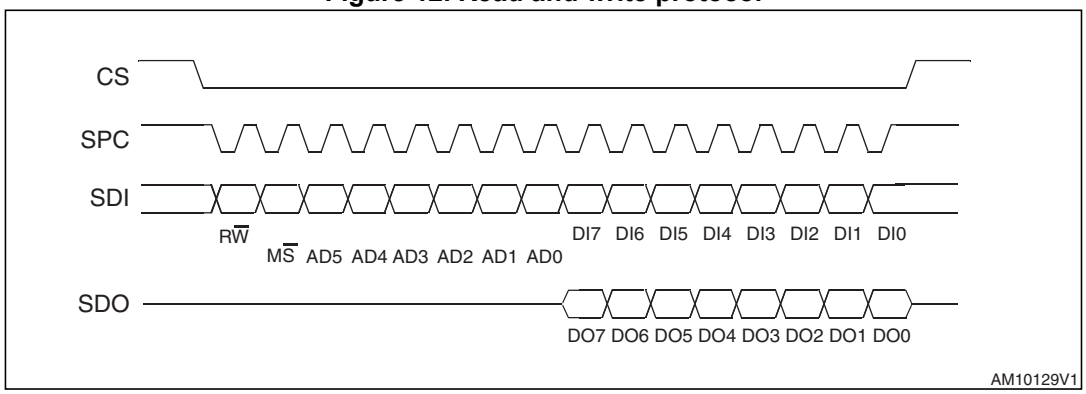
Command	SAD[6:1]	SAD[0] = SDO_G/SA0_G pin	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

6.2 SPI bus interface

The SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface interacts with the outside world through 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 12. Read and write protocol



CS is the Serial Port Enable and is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the Serial Port Clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the Serial Port Data Input and Output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the Read Register and Write Register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple bytes read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written to the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip will drive **SDO** at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address will be auto-incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written to the device (MSb first).

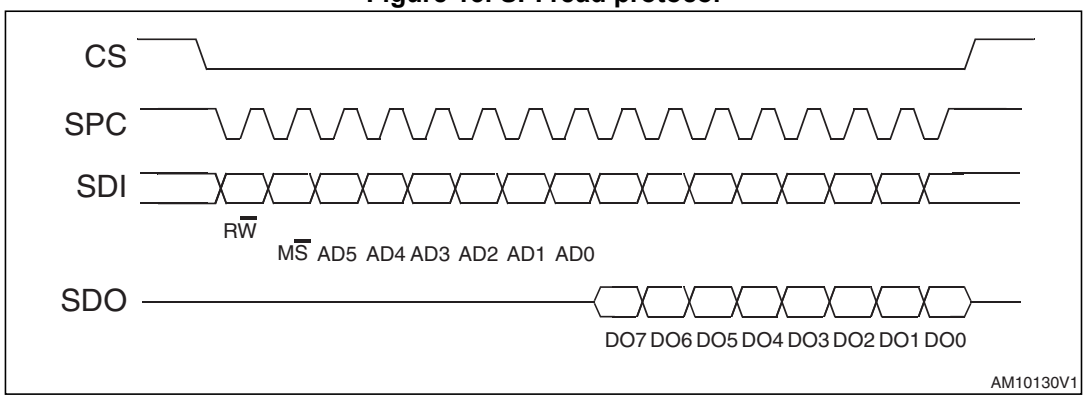
bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

In multiple read/write commands, further blocks of 8 clock periods will be added. When the M$\overline{S}$ bit is 0, the address used to read/write data remains the same for every block. When the M$\overline{S}$ bit is 1, the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

6.2.1 SPI read

Figure 13. SPI read protocol



The SPI read command is performed with 16 clock pulses. The multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: READ bit. The value is 1.

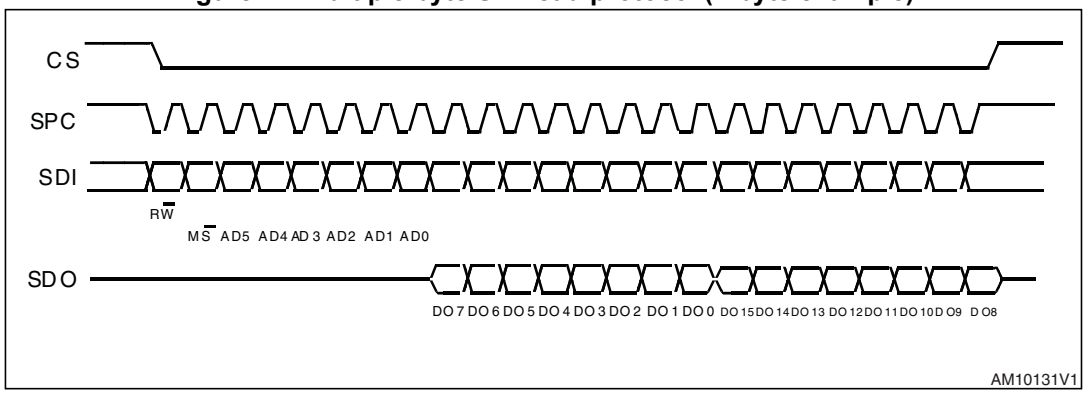
bit 1: MS bit. When 0, does not increment address; when 1, increments address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

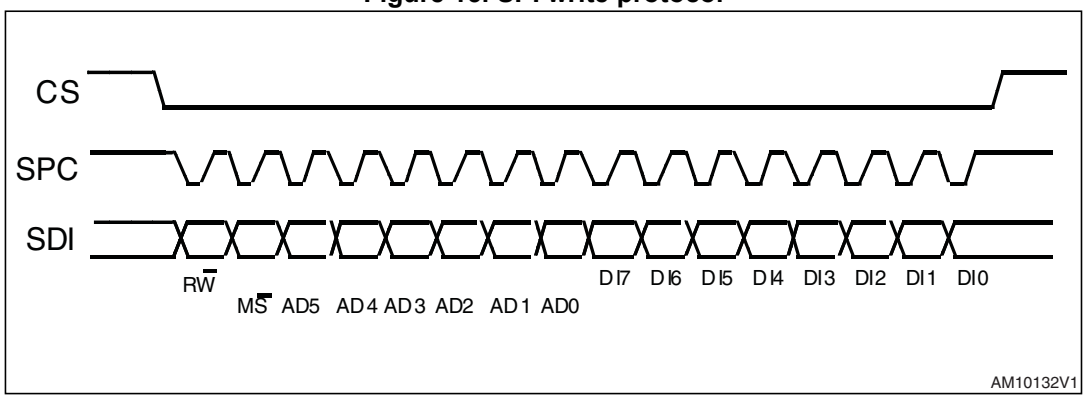
bit 16-... : data DO(...-8). Further data in multiple byte reads.

Figure 14. Multiple byte SPI read protocol (2-byte example)



6.2.2 SPI write

Figure 15. SPI write protocol



The SPI Write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

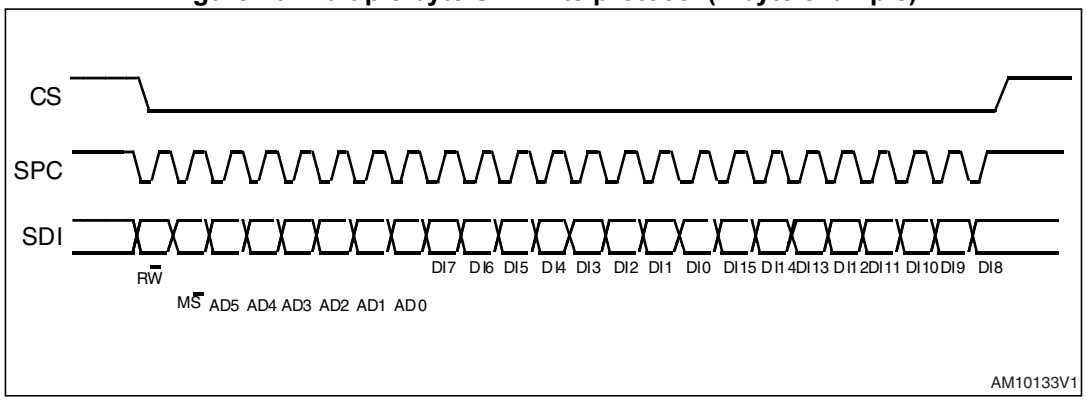
bit 1: MS bit. When 0, does not increment address; when 1, increments address in multiple writes.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written to the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

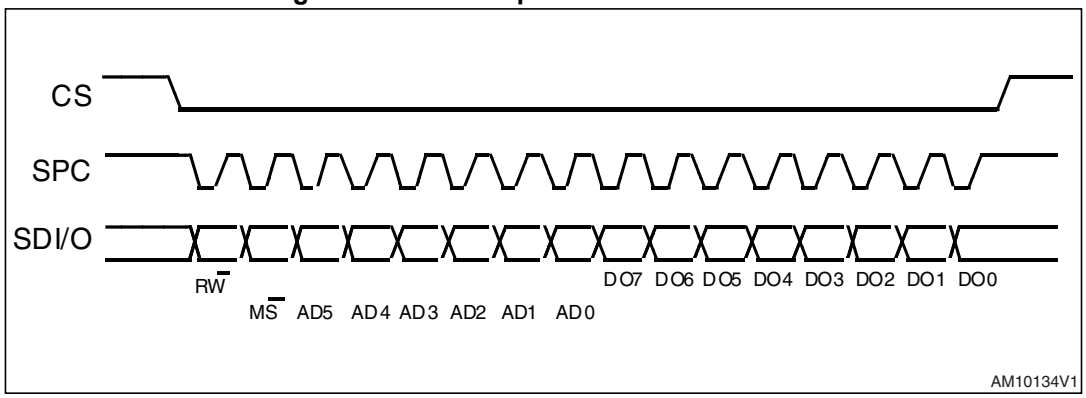
Figure 16. Multiple byte SPI write protocol (2-byte example)



6.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the bit SIM (SPI serial interface mode selection) to ‘1’ in *CTRL_REG2_XM (21h)* for the accelerometer and magnetic sensor and in *CTRL_REG4_G (23h)* for the gyroscope.

Figure 17. SPI read protocol in 3-wire mode



The SPI Read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: M$\overline{S}$ bit. When 0, does not increment address; when 1, increments address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

The multiple read command is also available in 3-wire mode.

7 Register mapping

The table given below provides a listing of the 8-bit registers embedded in the device and their respective addresses.

Table 17. Register address map

Name	Slave Address	Type	Register address		Default
			Hex	Binary	
Reserved	*Table 16*	--	00-0E	--	--
WHO_AM_I_G	*Table 16*	r	0F	000 1111	11010100
Reserved	*Table 16*	--	10-1F	--	--
CTRL_REG1_G	*Table 16*	rw	20	010 0000	00000111
CTRL_REG2_G	*Table 16*	rw	21	010 0001	00000000
CTRL_REG3_G	*Table 16*	rw	22	010 0010	00000000
CTRL_REG4_G	*Table 16*	rw	23	010 0011	00000000
CTRL_REG5_G	*Table 16*	rw	24	010 0100	00000000
REFERENCE_G	*Table 16*	rw	25	010 0101	00000000
Reserved	*Table 16*	--	26	--	--
STATUS_REG_G	*Table 16*	r	27	010 0111	output
OUT_X_L_G	*Table 16*	r	28	010 1000	output
OUT_X_H_G	*Table 16*	r	29	010 1001	output
OUT_Y_L_G	*Table 16*	r	2A	010 1010	output
OUT_Y_H_G	*Table 16*	r	2B	010 1011	output
OUT_Z_L_G	*Table 16*	r	2C	010 1100	output
OUT_Z_H_G	*Table 16*	r	2D	010 1101	output
FIFO_CTRL_REG_G	*Table 16*	rw	2E	010 1110	00000000
FIFO_SRC_REG_G	*Table 16*	r	2F	010 1111	output
INT1_CFG_G	*Table 16*	rw	30	011 0000	00000000
INT1_SRC_G	*Table 16*	r	31	011 0001	output
INT1_TSH_XH_G	*Table 16*	rw	32	011 0010	00000000
INT1_TSH_XL_G	*Table 16*	rw	33	011 0011	00000000
INT1_TSH_YH_G	*Table 16*	rw	34	011 0100	00000000
INT1_TSH_YL_G	*Table 16*	rw	35	011 0101	00000000
INT1_TSH_ZH_G	*Table 16*	rw	36	011 0110	00000000
INT1_TSH_ZL_G	*Table 16*	rw	37	011 0111	00000000
INT1_DURATION_G	*Table 16*	rw	38	011 1000	00000000
Reserved	*Table 15*	--	00-04	--	--

Table 17. Register address map (continued)

Name	Slave Address	Type	Register address		Default
			Hex	Binary	
OUT_TEMP_L_XM	Table 15	r	05	000 0101	output
OUT_TEMP_H_XM	Table 15	r	06	000 0110	output
STATUS_REG_M	Table 15	r	07	000 0111	output
OUT_X_L_M	Table 15	r	08	000 1000	output
OUT_X_H_M	Table 15	r	09	000 1001	output
OUT_Y_L_M	Table 15	r	0A	000 1010	output
OUT_Y_H_M	Table 15	r	0B	000 1011	output
OUT_Z_L_M	Table 15	r	0C	000 1100	output
OUT_Z_H_M	Table 15	r	0D	000 1101	output
Reserved	Table 15	--	0E	000 1110	--
WHO_AM_I_XM	Table 15	r	0F	000 1111	01001001
Reserved	Table 15	--	10-11	--	--
INT_CTRL_REG_M	Table 15	rw	12	001 0010	11101000
INT_SRC_REG_M	Table 15	r	13	001 0011	output
INT_THS_L_M	Table 15	rw	14	001 0100	00000000
INT_THS_H_M	Table 15	rw	15	001 0101	00000000
OFFSET_X_L_M	Table 15	rw	16	001 0110	00000000
OFFSET_X_H_M	Table 15	rw	17	001 0111	00000000
OFFSET_Y_L_M	Table 15	rw	18	001 01000	00000000
OFFSET_Y_H_M	Table 15	rw	19	001 01001	00000000
OFFSET_Z_L_M	Table 15	rw	1A	001 01010	00000000
OFFSET_Z_H_M	Table 15	rw	1B	001 01011	00000000
REFERENCE_X	Table 15	rw	1C	001 01100	00000000
REFERENCE_Y	Table 15	rw	1D	001 01101	00000000
REFERENCE_Z	Table 15	rw	1E	001 01110	00000000
CTRL_REG0_XM	Table 15	rw	1F	001 1111	00000000
CTRL_REG1_XM	Table 15	rw	20	010 0000	00000111
CTRL_REG2_XM	Table 15	rw	21	010 0001	00000000
CTRL_REG3_XM	Table 15	rw	22	010 0010	00000000
CTRL_REG4_XM	Table 15	rw	23	010 0011	00000000
CTRL_REG5_XM	Table 15	rw	24	010 0100	00011000
CTRL_REG6_XM	Table 15	rw	25	010 0101	00100000
CTRL_REG7_XM	Table 15	rw	26	010 0110	00000001

Table 17. Register address map (continued)

Name	Slave Address	Type	Register address		Default
			Hex	Binary	
STATUS_REG_A	Table 15	r	27	010 0111	output
OUT_X_L_A	Table 15	r	28	010 1000	output
OUT_X_H_A	Table 15	r	29	010 1001	output
OUT_Y_L_A	Table 15	r	2A	010 1010	output
OUT_Y_H_A	Table 15	r	2B	010 1011	output
OUT_Z_L_A	Table 15	r	2C	010 1100	output
OUT_Z_H_A	Table 15	r	2D	010 1101	output
FIFO_CTRL_REG	Table 15	rw	2E	010 1110	00000000
FIFO_SRC_REG	Table 15	r	2F	010 1111	output
INT_GEN_1_REG	Table 15	rw	30	011 0000	00000000
INT_GEN_1_SRC	Table 15	r	31	011 0001	output
INT_GEN_1_THS	Table 15	rw	32	011 0010	00000000
INT_GEN_1_DURATION	Table 15	rw	33	011 0011	00000000
INT_GEN_2_REG	Table 15	rw	34	011 0100	00000000
INT_GEN_2_SRC	Table 15	r	35	011 0101	output
INT_GEN_2_THS	Table 15	rw	36	011 0110	00000000
INT_GEN_2_DURATION	Table 15	rw	37	011 0111	00000000
CLICK_CFG	Table 15	rw	38	011 1000	00000000
CLICK_SRC	Table 15	r	39	011 1001	output
CLICK_THS	Table 15	rw	3A	011 1010	00000000
TIME_LIMIT	Table 15	rw	3B	011 1011	00000000
TIME _LATENCY	Table 15	rw	3C	011 1100	00000000
TIME_WINDOW	Table 15	rw	3D	011 1101	00000000
Act_THS	Table 15	rw	3E	011 1110	00000000
Act_DUR	Table 15	rw	3F	011 1111	00000000

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory-calibrated values. Their content is automatically restored when the device is powered up.

8 Register description

The device contains a set of registers which are used to control its behavior and to retrieve angular rate data. The register address, consisting of 7 bits, is used to identify them and to write the data through the serial interface.

8.1 WHO_AM_I_G (0Fh)

Table 18. WHO_AM_I_G register

1	1	0	1	0	1	0	0

Device identification register.

8.2 CTRL_REG1_G (20h)

Table 19. CTRL_REG1_G register

DR1	DR0	BW1	BW0	PD	Zen	Xen	Yen

Table 20. CTRL_REG1_G description

DR1-DR0	Output data rate selection. Refer to *Table 21*
BW1-BW0	Bandwidth selection. Refer to *Table 21*
PD	Power-down mode enable. Default value: 0 (0: power-down mode, 1: normal mode or sleep mode)
Zen	Z-axis enable. Default value: 1 (0: Z-axis disabled; 1: Z-axis enabled)
Yen	Y-axis enable. Default value: 1 (0: Y-axis disabled; 1: Y-axis enabled)
Xen	X-axis enable. Default value: 1 (0: X-axis disabled; 1: X-axis enabled)

DR[1:0] is used for ODR selection. **BW [1:0]** is used for Bandwidth selection.

In *Table 21* all frequencies resulting in combinations of DR / BW bits are given.

Table 21. DR and BW configuration setting

DR [1:0]	BW [1:0]	ODR (Hz)	Cutoff
00	00	95	12.5
00	01	95	25
00	10	95	25

Table 21. DR and BW configuration setting (continued)

DR [1:0]	BW [1:0]	ODR (Hz)	Cutoff
00	11	95	25
01	00	190	12.5
01	01	190	25
01	10	190	50
01	11	190	70
10	00	380	20
10	01	380	25
10	10	380	50
10	11	380	100
11	00	760	30
11	01	760	35
11	10	760	50
11	11	760	100

A combination of **PD, Zen, Yen, Xen** is used to set device to different modes (power-down / normal / sleep mode) in accordance with *Table 22* below.

Table 22. Power mode selection configuration

Mode	PD	Zen	Yen	Xen
Power-down	0	-	-	-
Sleep	1	0	0	0
Normal	1	-	-	-

8.3 CTRL_REG2_G (21h)

Table 23. CTRL_REG2_G register

0(1)	0(1)	HPM1	HPM1	HPCF3	HPCF2	HPCF1	HPCF0

1. These bits must be set to ‘0’ to ensure proper operation of the device

Table 24. CTRL_REG2_G description

HPM1-HPM0	High-pass filter mode selection. Default value: 00 Refer to *Table 25*
HPCF3-HPCF0	High-pass filter cutoff frequency selection Refer to *Table 26*

Table 25. High-pass filter mode configuration

HPM1	HPM0	High-pass filter mode
0	0	Normal mode (reset reading HP_RESET_FILTER)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Autoreset on interrupt event

Table 26. High-pass filter cutoff frequency configuration (Hz)

HPCF[3:0]	ODR = 95 Hz	ODR = 190 Hz	ODR = 380 Hz	ODR = 760 Hz
0000	7.2	13.5	27	51.4
0001	3.5	7.2	13.5	27
0010	1.8	3.5	7.2	13.5
0011	0.9	1.8	3.5	7.2
0100	0.45	0.9	1.8	3.5
0101	0.18	0.45	0.9	1.8
0110	0.09	0.18	0.45	0.9
0111	0.045	0.09	0.18	0.45
1000	0.018	0.045	0.09	0.18
1001	0.009	0.018	0.045	0.09

8.4 CTRL_REG3_G (22h)

Table 27. CTRL_REG3_G register

I1_Int1	I1_Boot	H_Lactive	PP_OD	I2_DRDY	I2_WTM	I2_ORun	I2_Empty

Table 28. CTRL_REG3_G description

I1_Int1	Interrupt enable on INT_G pin. Default value 0. (0: disable; 1: enable)
I1_Boot	Boot status available on INT_G. Default value 0. (0: disable; 1: enable)
H_Lactive	Interrupt active configuration on INT_G. Default value 0. (0: high; 1:low)
PP_OD	Push-pull / Open drain. Default value: 0. (0: push- pull; 1: open drain)
I2_DRDY	Date-ready on DRDY_G. Default value 0. (0: disable; 1: enable)
I2_WTM	FIFO watermark interrupt on DRDY_G. Default value: 0. (0: disable; 1: enable)
I2_ORun	FIFO overrun interrupt on DRDY_G. Default value: 0. (0: disable; 1: enable)
I2_Empty	FIFO empty interrupt on DRDY_G. Default value: 0. (0: disable; 1: enable)

8.5 CTRL_REG4_G (23h)

Table 29. CTRL_REG4_G register

BDU	BLE	FS1	FS0	-	ST1	ST0	SIM

Table 30. CTRL_REG4_G description

BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSb and LSb read)
BLE	Big/little endian data selection. Default value 0. (0: Data LSb @ lower address; 1: Data MSb @ lower address)
FS1-FS0	Full-scale selection. Default value: 00 (00: 245 dps; 01: 500 dps; 10: 2000 dps; 11: 2000 dps)
ST1-ST0	Self-test enable. Default value: 00 (00: Self-test disabled; Other: See *Table 31*)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface).

Table 31. Self-test mode configuration

ST1	ST0	Self-test mode
0	0	Normal mode
0	1	Self-test 0 (1)(X positive sign, Y and Z negative sign)
1	0	--
1	1	Self-test 1 (1) (X negative sign, Y and Z positive sign)

1. DST sign (absolute value in *Table 3*)

8.6 CTRL_REG5_G (24h)

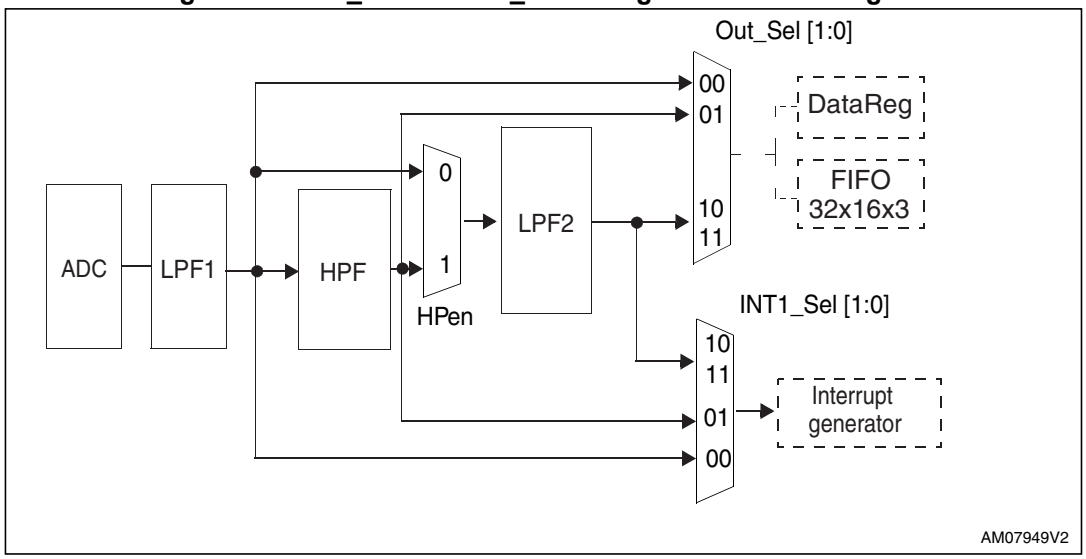
Table 32. CTRL_REG5_G register

BOOT	FIFO_EN	--	HPen	INT1_Sel1	INT1_Sel0	Out_Sel1	Out_Sel0

Table 33. CTRL_REG5_G description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disable; 1: FIFO enable)
HPen	High-pass filter enable. Default value: 0 (0: HPF disabled; 1: HPF enabled) (See *Figure 18*)
INT1_Sel1-INT1_Sel0	INT1 selection configuration. Default value: 00 (See *Figure 18*)
Out_Sel1-Out_Sel0	Out selection configuration. Default value: 00 (See *Figure 18*)

Figure 18. INT1_Sel and Out_Sel configuration block diagram



8.7 REFERENCE/DATACAPTURE_G (25h)

Table 34. REFERENCE/DATACAPTURE_G register

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0

Table 35. REFERENCE/DATACAPTURE_G description

Ref 7-Ref0	Reference value for interrupt generation. Default value: 0

8.8 STATUS_REG_G (27h)

Table 36. STATUS_REG_G register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 37. STATUS_REG_G description

ZYXOR	X, Y, Z -axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data has overwritten the previous data before it was read)
ZOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YOR	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)

Table 37. STATUS_REG_G description (continued)

ZYXDA	X, Y, Z -axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z-axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y-axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available;1: new data for the Y-axis is available)
XDA	X-axis new data available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

8.9 OUT_X_L_G (28h), OUT_X_H_G (29h)

X-axis angular rate data. The value is expressed as two's complement.

8.10 OUT_Y_L_G (2Ah), OUT_Y_H_G (2Bh)

Y-axis angular rate data. The value is expressed as two's complement.

8.11 OUT_Z_L_G (2Ch), OUT_Z_H_G (2Dh)

Z-axis angular rate data. The value is expressed as two's complement.

8.12 FIFO_CTRL_REG_G (2Eh)

Table 38. FIFO_CTRL_REG_G register

FM2	FM1	FM0	WTM4	WTM3	WTM2	WTM1	WTM0

Table 39. FIFO_CTRL_REG_G description

FM2-FM0	FIFO mode selection. Default value: 00 (see *Table 40*)
WTM4-WTM0	FIFO threshold. Watermark level setting

Table 40. FIFO mode configuration

FM2	FM1	FM0	FIFO mode
0	0	0	Bypass mode
0	0	1	FIFO mode
0	1	0	Stream mode
0	1	1	Stream-to-FIFO mode
1	0	0	Bypass-to-Stream mode

8.13 FIFO_SRC_REG_G (2Fh)

Table 41. FIFO_SRC_REG_G register

WTM	OVRN	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 42. FIFO_SRC_REG_G description

WTM	Watermark status. (0: FIFO filling is lower than WTM level; 1: FIFO filling is equal to or higher than WTM level)
OVRN	Overrun bit status. (0: FIFO is not completely filled; 1: FIFO is completely filled)
EMPTY	FIFO empty bit. (0: FIFO not empty; 1: FIFO empty)
FSS4-FSS1	FIFO stored data level

8.14 INT1_CFG_G (30h)

Table 43. INT1_CFG_G register

AND/OR	LIR	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 44. INT1_CFG_G description

AND/OR	AND/OR combination of interrupt events. Default value: 0 (0: OR combination of interrupt events 1: AND combination of interrupt events
LIR	Latch interrupt request. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched) Cleared by reading INT1_SRC reg.
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)

Table 44. INT1_CFG_G description (continued)

XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)

8.15 INT1_SRC_G (31h)

Interrupt source register. Read-only register.

Table 45. INT1_SRC_G register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 46. INT1_SRC_G description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Reading at this address clears the INT1_SRC IA bit (and eventually the interrupt signal on the INT_G pin) and allows the refresh of data in the INT1_SRC register if the latched option was chosen.

8.16 INT1_THS_XH_G (32h)

Table 47. INT1_THS_XH_G register

-	THSX14	THSX13	THSX12	THSX11	THSX10	THSX9	THSX8

Table 48. INT1_THS_XH_G description

THSX14 - THSX8	Interrupt threshold. Default value: 000 0000

8.17 INT1_THS_XL_G (33h)

Table 49. INT1_THS_XL_G register

THSX7	THSX6	THSX5	THSX4	THSX3	THSX2	THSX1	THSX0

Table 50. INT1_THS_XL_G description

THSX7 - THSX0	Interrupt threshold. Default value: 0000 0000

8.18 INT1_THS_YH_G (34h)

Table 51. INT1_THS_YH_G register

-	THSY14	THSY13	THSY12	THSY11	THSY10	THSY9	THSY8

Table 52. INT1_THS_YH_G description

THSY14 - THSY8	Interrupt threshold. Default value: 000 0000

8.19 INT1_THS_YL_G (35h)

Table 53. INT1_THS_YL_G register

THSR7	THSY6	THSY5	THSY4	THSY3	THSY2	THSY1	THSY0

Table 54. INT1_THS_YL_G description

THSY7 - THSY0	Interrupt threshold. Default value: 0000 0000

8.20 INT1_THS_ZH_G (36h)

Table 55. INT1_THS_ZH_G register

-	THSZ14	THSZ13	THSZ12	THSZ11	THSZ10	THSZ9	THSZ8

Table 56. INT1_THS_ZH_G description

THSZ14 - THSZ8	Interrupt threshold. Default value: 000 0000

8.21 INT1_THS_ZL_G (37h)

Table 57. INT1_THS_ZL_G register

THSZ7	THSZ6	THSZ5	THSZ4	THSZ3	THSZ2	THSZ1	THSZ0

Table 58. INT1_THS_ZL_G description

THSZ7 - THSZ0	Interrupt threshold. Default value: 0000 0000

8.22 INT1_DURATION_G (38h)

Table 59. INT1_DURATION_G register

WAIT	D6	D5	D4	D3	D2	D1	D0

Table 60. INT1_DURATION_G description

WAIT	WAIT enable. Default value: 0 (0: disable; 1: enable)
D6 - D0	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the interrupt event to be recognized. Duration steps and maximum values depend on the ODR chosen.

The **WAIT** bit has the following definitions:

Wait = ‘0’: the interrupt falls immediately if the signal crosses the selected threshold

Wait = ‘1’: if the signal crosses the selected threshold, the interrupt falls only after the duration has counted the number of samples at the selected data rate, written into the duration counter register.

Figure 19. Wait bit disabled

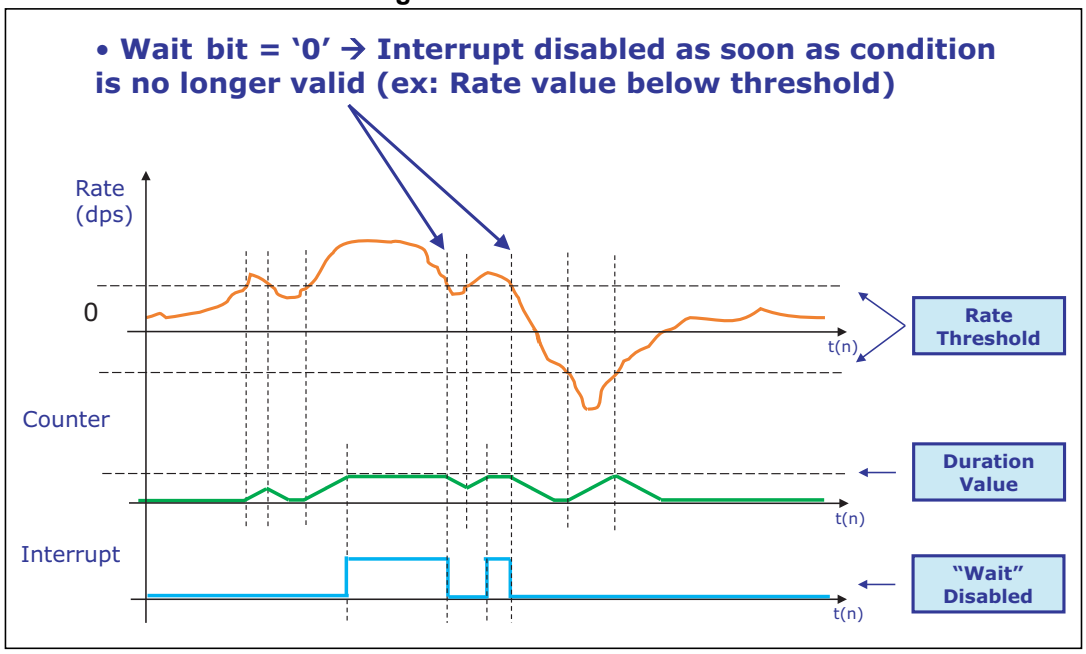
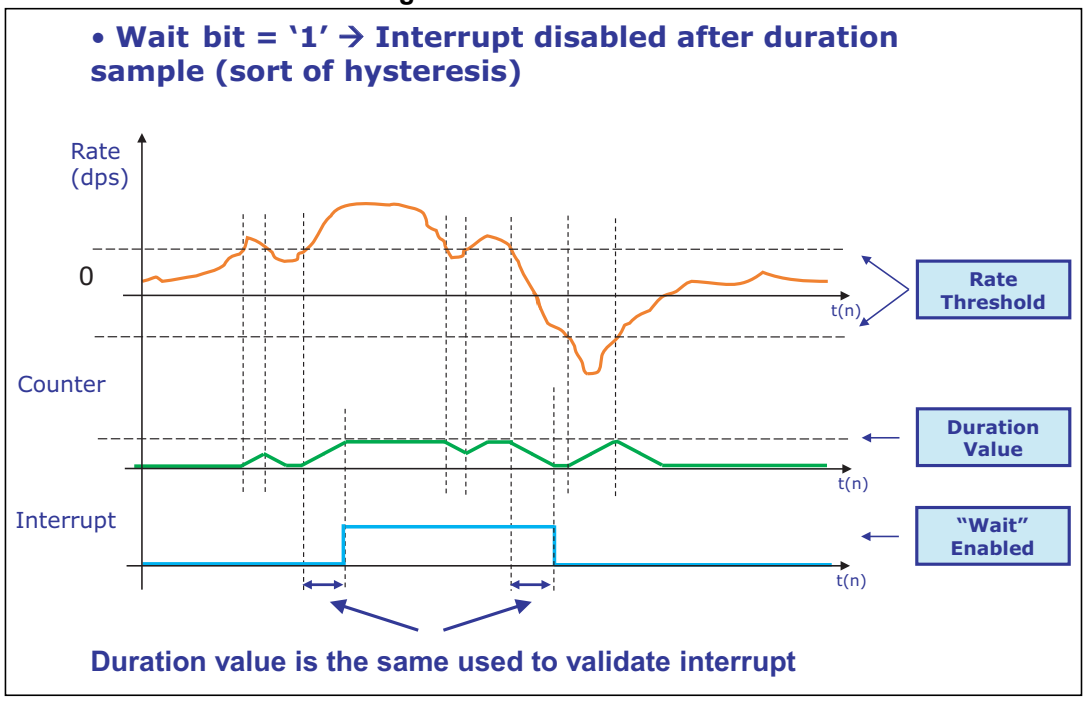


Figure 20. Wait bit enabled



8.23 OUT_TEMP_L_XM (05h), OUT_TEMP_H_XM (06h)

Temperature sensor data.

Refer to *Section 4.4: Temperature sensor* for details on how to enable and read the temperature sensor output data.

8.24 STATUS_REG_M (07h)

Table 61. STATUS_REG_M register

ZYXMOR	ZMOR	YMOR	XMOR	ZYXMDA	ZMDA	YMDA	XMDA

Table 62. STATUS_REG_M description

ZYXMOR	Magnetic X, Y and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous ones).
ZMOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the Z-axis has overwritten the previous one)
YMOR	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the Y-axis has overwritten the previous one)
XMOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the X-axis has overwritten the previous one)
ZYXMDA	X, Y and Z-axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available).
ZMDA	Z-axis new data available. Default value: 0 (0: a new set of data for the Z-axis is not yet available; 1: a new set of data for the Z-axis is available)
YMDA	Y-axis new data available. Default value: 0 (0: a new set of data for the Y-axis is not yet available; 1: a new set of data for the Y-axis is available)
XMDA	X-axis new data available. Default value: 0 (0: a new set of data for the X-axis is not yet available; 1: a new set of data for the X-axis is available)

8.25 OUT_X_L_M (08h), OUT_X_H_M (09h)

X-axis magnetic data.

The value is expressed in 16-bit as two’s complement left justified.

8.26 OUT_Y_L_M (0Ah), OUT_Y_H_M (0Bh)

Y-axis magnetic data.

The value is expressed in 16-bit as two’s complement left justified.

8.27 OUT_Z_L_M (0Ch), OUT_Z_H_M (0Dh)

Z-axis magnetic data.

The value is expressed in 16-bit as two's complement left justified.

8.28 WHO_AM_I_XM (0Fh)

Table 63. WHO_AM_I_XM register

0	1	0	0	1	0	0	1

Device identification register.

8.29 INT_CTRL_REG_M (12h)

Table 64. INT_CTRL_REG_M register

XMIEN	YMIEN	ZMIEN	PP_OD	IEA	IEL	4D	MIEN

Table 65. INT_CTRL_REG_M description

XMIEN	Enable interrupt recognition on X-axis for magnetic data. Default value: 0. (0: disable interrupt recognition;1: enable interrupt recognition)
YMIEN	Enable interrupt recognition on Y-axis for magnetic data. Default value: 0. (0: disable interrupt recognition;1: enable interrupt recognition)
ZMIEN	Enable interrupt recognition on Z-axis for magnetic data. Default value: 0. (0: disable interrupt recognition;1: enable interrupt recognition)
PP_OD	Interrupt pin configuration. Default value: 0. (0: push-pull; 1: open drain)
IEA	Interrupt polarity for both accelerometer and magnetometer. Default value: 0. (0: interrupt active-low; 1: interrupt active-high)
IEL	Latch interrupt request on accelerometer *INT_GEN_1_SRC (31h)* and *INT_GEN_2_SRC (35h)* registers, and magnetometer *INT_SRC_REG_M (13h)* register. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched) Once the IEL is set to '1' the interrupt is cleared by reading for the accelerometer the *INT_GEN_1_SRC (31h)* and *INT_GEN_2_SRC (35h)* registers, and for the magnetometer the *INT_SRC_REG_M (13h)* register.
4D	4D enable: 4D detection on acceleration data is enabled when 6D bit in *INT_GEN_1_REG (30h)* is set to 1.
MIEN	Enable interrupt generation for magnetic data. Default value: 0. (0: disable interrupt generation;1: enable interrupt generation)

8.30 INT_SRC_REG_M (13h)

Table 66. INT_SRC_REG_M register

M_PTH_X	M_PTH_Y	M_PTH_Z	M_NTH_X	M_NTH_Y	M_NTH_Z	MROI	MINT

Table 67. INT_SRC_REG_M description

M_PTH_X	Magnetic value on X-axis exceeds the threshold on the positive side. Default value: 0.
M_PTH_Y	Magnetic value on Y-axis exceeds the threshold on the positive side. Default value: 0.
M_PTH_Z	Magnetic value on Z-axis exceeds the threshold on the positive side. Default value: 0.
M_NTH_X	Magnetic value on X-axis exceeds the threshold on the negative side. Default value: 0.
M_NTH_Y	Magnetic value on Y-axis exceeds the threshold on the negative side. Default value: 0.
M_NTH_Z	Magnetic value on Z-axis exceeds the threshold on the negative side. Default value: 0.
MROI	Internal measurement range overflow on magnetic value. Default value: 0. To enable this feature need to set to 1 MIEN bit in *8.29: INT_CTRL_REG_M (12h)*
MINT	Magnetic interrupt event. The magnetic field value exceeds the threshold. Default value: 0.

8.31 INT_THS_L_M (14h), INT_THS_H_M (15h)

Magnetic interrupt threshold. Default value: 0.

The value is expressed in 16-bit unsigned.

Even if the threshold is expressed in absolute value, the device detects both positive and negative thresholds.

8.32 OFFSET_X_L_M (16h), OFFSET_X_H_M (17h)

Magnetic offset for X-axis. Default value: 0.

The value is expressed in 16-bit as two’s complement left justified.

8.33 OFFSET_Y_L_M (18h), OFFSET_Y_H_M (19h)

Magnetic offset for Z-axis. Default value: 0.

The value is expressed in 16-bit as two’s complement left justified.

8.34 OFFSET_Z_L_M (1Ah), OFFSET_Z_H_M (1Bh)

Magnetic offset for Y-axis. Default value: 0.

The value is expressed in 16-bit as two’s complement left justified.

8.35 REFERENCE_X (1Ch)

Reference value for high-pass filter for x-axis acceleration data.

8.36 REFERENCE_Y (1Dh)

Reference value for high-pass filter for y-axis acceleration data.

8.37 REFERENCE_Z (1Eh)

Reference value for high-pass filter for z-axis acceleration data.

8.38 CTRL_REG0_XM (1Fh)

Table 68. CTRL_REG0_XM register

BOOT	FIFO_EN	WTM_EN	0(1)	0(1)	HP_Click	HPIS1	HPIS2

1. These bits must be set to '0' for the correct operation of the device

Table 69. CTRL_REG0_XM description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disable; 1: FIFO Enable)
WTM_EN	FIFO programmable watermark enable. Default value: 0 (0: disable; 1: Enable)
HP_Click	High-pass filter enabled for Click function. Default value: 0 (0: filter bypassed; 1: filter enabled)
HPIS1	High-pass filter enabled for interrupt generator 1. Default value: 0 (0: filter bypassed; 1: filter enabled)
HPIS2	High-pass filter enabled for interrupt generator 2. Default value: 0 (0: filter bypassed; 1: filter enabled)

8.39 CTRL_REG1_XM (20h)

Table 70. CTRL_REG1_XM register

AODR3	AODR2	AODR1	AODR0	BDU	AZEN	AYEN	AXEN

Table 71. CTRL_REG1_XM description

AODR3-AODR0	Acceleration data rate selection. Default value: 0000 (0000: power-down mode; others: refer to *Table 72: Acceleration data rate configuration*)
BDU	Block data update for acceleration and magnetic data. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB have been read)
AZEN	Acceleration Z-axis enable. Default value: 1 (0: Z-axis disabled; 1: Z-axis enabled)
AYEN	Acceleration Y-axis enable. Default value: 1 (0: Y-axis disabled; 1: Y-axis enabled)
AXEN	Acceleration X-axis enable. Default value: 1 (0: X-axis disabled; 1: X-axis enabled)

AODR[3:0] is used to set the power mode and ODR selection. The following table indicates all frequencies resulting from the combination of AODR[3:0].

Table 72. Acceleration data rate configuration

AODR3	AODR2	AODR1	AODR0	Power mode selection
0	0	0	0	Power-down mode
0	0	0	1	3.125 Hz
0	0	1	0	6.25 Hz
0	0	1	1	12.5 Hz
0	1	0	0	25 Hz
0	1	0	1	50 Hz
0	1	1	0	100 Hz
0	1	1	1	200 Hz
1	0	0	0	400 Hz
1	0	0	1	800 Hz
1	0	1	0	1600 Hz

8.40 CTRL_REG2_XM (21h)

Table 73. CTRL_REG2_XM register

ABW1	ABW0	AFS2	AFS1	AFS0	AST1	AST0	SIM

Table 74. CTRL_REG2_XM description

ABW[1:0]	Accelerometer anti-alias filter bandwidth. Default value: 00 Refer to *Table 75: Acceleration anti-alias filter bandwidth*
AFS[2:0]	Acceleration full-scale selection. Default value: 000 Refer to *Table 76: Acceleration full-scale selection*
AST[1:0]	Acceleration self-test enable. Default value: 00 (00: self-test disabled; see *Table 77: Self-test mode configuration*)
SIM	SPI Serial Interface Mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)

Table 75. Acceleration anti-alias filter bandwidth

ABW1	ABW0	Anti-alias filter bandwidth
0	0	773 Hz
0	1	194 Hz
1	0	362 Hz
1	1	50 Hz

Table 76. Acceleration full-scale selection

AFS2	AFS1	AFS0	Acceleration full scale
0	0	0	±2 *g*
0	0	1	±4 *g*
0	1	0	±6 *g*
0	1	1	±8 *g*
1	0	0	±16 *g*

Table 77. Self-test mode configuration

AST1	AST0	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Negative sign self-test
1	1	Not allowed

8.41 CTRL_REG3_XM (22h)

Table 78. CTRL_REG3_XM register

P1_BOOT	P1_TAP	P1_INT1	P1_INT2	P1_INTM	P1_DRDYA	P1_DRDYM	P1_EMPTY

Table 79. CTRL_REG3_XM description

P1_BOOT	Boot on INT1_XM pin enable. Default value: 0 (0: disable; 1: enable)
P1_TAP	Tap generator interrupt on INT1_XM pin. Default value: 0 (0: disable; 1: enable)
P1_INT1	Inertial interrupt generator 1 on INT1_XM pin. Default value: 0 (0: disable; 1: enable)
P1_INT2	Inertial interrupt generator 2 on INT1_XM pin. Default value: 0 (0: disable; 1: enable)
P1_INTM	Magnetic interrupt generator on INT1_XM pin. Default value: 0 (0: disable; 1: enable)
P1_DRDYA	Accelerometer data-ready signal on INT1_XM pin. Default value: 0 (0: disable; 1: enable)
P1_DRDYM	Magnetometer data-ready signal on INT1_XM pin. Default value: 0 (0: disable; 1: enable)
P1_EMPTY	FIFO empty indication on INT1_XM pin. Default value: 0 (0: disable; 1: enable)

8.42 CTRL_REG4_XM (23h)

Table 80. CTRL_REG4_XM register

P2_TAP	P2_INT1	P2_INT2	P2_INTM	P2_DRDYA	P2_DRDYM	P2_Overrun	P2_WTM

Table 81. CTRL_REG4_XM description

P2_TAP	Tap generator interrupt on INT2_XM pin. Default value: 0 (0: disable; 1: enable)
P2_INT1	Inertial interrupt generator 1 on INT2_XM pin. Default value: 0 (0: disable; 1: enable)
P2_INT2	Inertial interrupt generator 2 on INT2_XM pin. Default value: 0 (0: disable; 1: enable)
P2_INTM	Magnetic interrupt generator on INT2_XM pin. Default value: 0 (0: disable; 1: enable)
P2_DRDYA	Accelerometer data-ready signal on INT2_XM pin. Default value: 0 (0: disable; 1: enable)
P2_DRDYM	Magnetometer data-ready signal on INT2_XM pin. Default value: 0 (0: disable; 1: enable)
P2_Overrun	FIFO overrun interrupt on INT2_XM pin. Default value: 0 (0: disable; 1: enable)
P2_WTM	FIFO watermark interrupt on INT2_XM pin. Default value: 0 (0: disable; 1: enable)

8.43 CTRL_REG5_XM (24h)

Table 82. CTRL_REG5_XM register

TEMP_EN	M_RES1	M_RES0	M_ODR2	M_ODR1	M_ODR0	LIR2	LIR1

Table 83. CTRL_REG5_XM description

TEMP_EN	Temperature sensor enable. Default value: 0 (0: temperature sensor disabled; 1: temperature sensor enabled)
M_RES[1:0]	Magnetic resolution selection. Default value: 00 (00: low resolution, 11: high resolution)
M_ODR[2:0]	Magnetic data rate selection. Default value: 110 Refer to *Table 84: Magnetic data rate configuration*
LIR2	Latch interrupt request on INT2_SRC register, with INT2_SRC register cleared by reading INT2_SRC itself. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)
LIR1	Latch interrupt request on INT1_SRC register, with INT1_SRC register cleared by reading INT1_SRC itself. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)

Table 84. Magnetic data rate configuration

M_ODR2	M_ODR1	M_ODR0	Power mode selection
0	0	0	3.125 Hz
0	0	1	6.25 Hz
0	1	0	12.5 Hz
0	1	1	25 Hz
1	0	0	50 Hz
1	0	1	100 Hz(1)
1	1	0	Reserved
1	1	1	Reserved

1. Available only for accelerometer ODR > 50 Hz or accelerometer in power-down mode (refer to *Table 72,* AODR setting).

8.44 CTRL_REG6_XM (25h)

Table 85. CTRL_REG6_XM register

0(1)	MFS1	MFS0	0(1)	0(1)	0(1)	0(1)	0(1)

1. These bits must be set to ‘0’ for the correct operation of the device

Table 86. CTRL_REG6_XM description

MFS1-MFS0	Magnetic full-scale selection. Default value: 01 Refer to *Table 87: Magnetic full-scale selection*

Table 87. Magnetic full-scale selection

MFS1	MFS0	Magnetic full scale
0	0	± 2 gauss
0	1	± 4 gauss
1	0	± 8 gauss
1	1	± 12 gauss

8.45 CTRL_REG7_XM (26h)

Table 88. CTRL_REG7_XM register

AHPM1	AHPM0	AFDS	0(1)	0(1)	MLP	MD1	MD0

1. These bits must be set to '0' for the correct operation of the device

Table 89. CTRL_REG7_XM description

AHPM1-AHPM0	High-pass filter mode selection for acceleration data. Default value: 00 Refer to *Table 90: High-pass filter mode selection*
AFDS	Filtered acceleration data selection. Default value: 0 (0: internal filter bypassed; 1: data from internal filter sent to output register and FIFO)
MLP	Magnetic data low-power mode. Default value: 0 If this bit is '1' the MODR is set to 3.125 Hz independently from the MODR settings. Once the bit is set to '0' the magnetic data rate is configured by MODR bits in *CTRL_REG5_XM (24h)* register.
MD1-MD0	Magnetic sensor mode selection. Default 10 Refer to *Table 91: Magnetic sensor mode selection*

Table 90. High-pass filter mode selection

AHPM1	AHPM0	High-pass filter mode
0	0	Normal mode (resets x, y and z-axis reading *REFERENCE_X (1Ch)*, *REFERENCE_Y (1Dh)* and *REFERENCE_Y (1Dh)* registers respectively)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Autoreset on interrupt event

Table 91. Magnetic sensor mode selection

MD1-0	MD1-0	Magnetic sensor mode
0	0	Continuous-conversion mode
0	1	Single-conversion mode
1	0	Power-down mode
1	1	Power-down mode

8.46 STATUS_REG_A (27h)

Table 92. STATUS_REG_A register

ZYXAOR	ZAOR	YAOR	XAOR	ZYXADA	ZADA	YADA	XADA

Table 93. STATUS_REG_A description

ZYXAOR	Acceleration X-, Y- and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous one)
ZAOR	Acceleration Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data for the Z-axis has overwritten the previous one)
YAOR	Acceleration Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data for the Y-axis has overwritten the previous one)
XAOR	Acceleration X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data for the X-axis has overwritten the previous one)
ZYXADA	Acceleration X-, Y- and Z-axis new value available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZADA	Acceleration Z-axis new value available. Default value: 0 (0: a new set of data for the Z-axis is not yet available; 1: a new set of data for the Z-axis is available)
YADA	Acceleration Y-axis new value available. Default value: 0 (0: a new set of data for the Y-axis is not yet available; 1: a new set of data for the Y-axis is available)
XADA	Acceleration X-axis new value available. Default value: 0 (0: a new set of data for the X-axis is not yet available; 1: a new set of data for the X-axis is available)

8.47 OUT_X_L_A (28h), OUT_X_H_A (29h)

X-axis acceleration data.

The value is expressed in 16 bit as two’s complement left justified.

8.48 OUT_Y_L_A (2Ah), OUT_Y_H_A (2Bh)

Y-axis acceleration data.

The value is expressed in 16-bit as two's complement left justified.

8.49 OUT_Z_L_A (2Ch), OUT_Z_H_A (2Dh)

Z-axis acceleration data.

The value is expressed in 16-bit as two's complement left justified.

8.50 FIFO_CTRL_REG (2Eh)

Table 94. FIFO_CTRL_REG register

FM2	FM1	FM0	FTH4	FTH3	FTH2	FTH1	FTH0

Table 95. FIFO_CTRL_REG description

FM2-FM0	FIFO mode selection. Default value: 000
FTH4-FTH0	FIFO watermark level. Default value: 00000

Table 96. FIFO mode configuration

FM2	FM1	FM0	FIFO mode
0	0	0	Bypass mode
0	0	1	FIFO mode
0	1	0	Stream mode
0	1	1	Stream-to-FIFO mode
1	0	0	Bypass-to-Stream mode

Interrupt generator 2 can change the FIFO mode.

8.51 FIFO_SRC_REG (2Fh)

Table 97. FIFO_SRC_REG register

WTM	OVRN	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 98. FIFO_SRC_REG description

WTM	Watermark status. WTM bit is set to '1' when FIFO content exceeds watermark level.
OVRN	FIFO Overrun status. OVRN bit is set to '1' when FIFO buffer is full.

Table 98. FIFO_SRC_REG description (continued)

EMPTY	Empty status. EMPTY bit is set to '1' when all FIFO samples have been read and FIFO is empty.
FSS4-FSS0	FIFO stored data level. FSS4-FSS0 bits contain the current number of unread FIFO levels.

8.52 INT_GEN_1_REG (30h)

This register contains the settings for the inertial interrupt generator 1.

Table 99. INT_GEN_1_REG register

AOI	6D	ZHIE/ ZUPE	ZLIE/ ZDOWNE	YHIE/ YUPE	YLIE/ YDOWNE	XHIE/ XUPE	XLIE/ XDOWNE

Table 100. INT_GEN_1_REG description

AOI	And/Or combination of Interrupt events. Default value: 0. Refer to *Table 101: Interrupt mode*
6D	6-direction detection function enabled. Default value: 0. Refer to *Table 101: Interrupt mode*
ZHIE/ ZUPE	Enable interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request;1: enable interrupt request)
ZLIE/ ZDOWNE	Enable interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request;1: enable interrupt request)
YHIE/ YUPE	Enable interrupt generation on Y high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
YLIE/ YDOWNE	Enable interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XHIE/ XUPE	Enable interrupt generation on X high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XLIE/XDOWNE	Enable interrupt generation on X low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)

Table 101. Interrupt mode

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6-direction movement recognition
1	0	AND combination of interrupt events
1	1	6-direction position recognition

The difference between AOI-6D = ‘01’ and AOI-6D = ‘11’ is as follows:

AOI-6D = ‘01’ is movement recognition. An interrupt is generated when the orientation moves from an unknown zone to a known zone. The interrupt signal stays for a duration ODR.

AOI-6D = ‘11’ is direction recognition. An interrupt is generated when the orientation is inside a known zone. The interrupt signal stays until the orientation is inside the zone.

8.53 INT_GEN_1_SRC (31h)

This register contains the status for the inertial interrupt generator 1.

Table 102. INT_GEN_1_SRC register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 103. INT_GEN_1_SRC description

IA	Interrupt Status. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Reading at this address clears the *INT_GEN_1_SRC (31h)* IA bit (and the interrupt signal on the corresponding interrupt pin) and allows the refreshment of data in the *INT_GEN_1_SRC (31h)* register if the latched option was chosen.

8.54 INT_GEN_1_THS (32h)

Table 104. INT1_THS register

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 105. INT1_THS description

THS6 - THS0	Interrupt 1 threshold. Default value: 000 0000

8.55 INT_GEN_1_DURATION (33h)

Table 106. INT1_DURATION register

0	D6	D5	D4	D3	D2	D1	D0

Table 107. INT1_DURATION description

D6 - D0	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the Interrupt 1 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

8.56 INT_GEN_2_REG (34h)

This register contains the settings for the inertial interrupt generator 2.

Table 108. INT_GEN_2_REG register

AOI	6D	ZHIE/ ZUPE	ZLIE/ ZDOWNE	YHIE/ YUPE	YLIE/ YDOWNE	XHIE/ XUPE	XLIE/ XDOWNE

Table 109. INT_GEN_2_REG description

AOI	And/Or combination of Interrupt events. Default value: 0. Refer to *Table 109: INT_GEN_2_REG description*
6D	6 direction detection function enabled. Default value: 0. Refer to *Table 109: INT_GEN_2_REG description*
ZHIE/ ZUPE	Enable interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request;1: enable interrupt request)
ZLIE/ ZDOWNE	Enable interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request;1: enable interrupt request)
YHIE/ YUPE	Enable interrupt generation on Y high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
YLIE/ YDOWNE	Enable interrupt generation on Y low event or on Direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XHIE/ XUPE	Enable interrupt generation on X high event or on Direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XLIE/XDOWNE	Enable interrupt generation on X low event or on Direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)

Table 110. Interrupt mode

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6-direction movement recognition
1	0	AND combination of interrupt events
1	1	6-direction position recognition

The difference between AOI-6D = ‘01’ and AOI-6D = ‘11’ is as follows:

AOI-6D = ‘01’ is movement recognition. An interrupt is generated when the orientation moves from an unknown zone to a known zone. The interrupt signal stays for a duration ODR.

AOI-6D = ‘11’ is direction recognition. An interrupt is generated when the orientation is inside a known zone. The interrupt signal stays until the orientation is inside the zone.

8.57 INT_GEN_2_SRC (35h)

This register contains the status for the inertial interrupt generator 2.

Table 111. INT_GEN_2_SRC register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 112. INT_GEN_2_SRC description

IA	Interrupt status. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Reading at this address clears the *INT_GEN_2_SRC (35h)* IA bit (and the interrupt signal on the corresponding interrupt pin) and allows the refreshment of data in the *INT_GEN_2_SRC (35h)* register if the latched option was chosen.

8.58 INT_GEN_2_THS (36h)

Table 113. INT_GEN_2_THS register

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 114. INT_GEN_2_THS description

THS6 - THS0	Interrupt 1 threshold. Default value: 000 0000

8.59 INT_GEN_2_DURATION (37h)

Table 115. INT_GEN_2_DURATION register

0	D6	D5	D4	D3	D2	D1	D0

Table 116. INT_GEN_2_DURATION description

D6 - D0	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the Interrupt 2 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

8.60 CLICK_CFG (38h)

Table 117. CLICK_CFG register

--	--	ZD	ZS	YD	YS	XD	XS

Table 118. CLICK_CFG description

ZD	Enable interrupt double-click on Z-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
ZS	Enable interrupt single-click on Z-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YD	Enable interrupt double-click on Y-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YS	Enable interrupt single-click on Y-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)

Table 118. CLICK_CFG description

XD	Enable interrupt double-click on X-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XS	Enable interrupt single-click on X-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)

8.61 CLICK_SRC (39h)

Table 119. CLICK_SRC register

--	IA	DClick	SClick	Sign	Z	Y	X

Table 120. CLICK_SRC description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
DClick	Double-click enable. Default value: 0 (0: double-click detection disabled, 1: double-click detection enabled)
SClick	Single-click enable. Default value: 0 (0: single-click detection disabled, 1: single-click detection enabled)
Sign	Click sign. 0: positive detection, 1: negative detection
Z	Z click detection. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
Y	Y click detection. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
X	X click detection. Default value: 0 (0: no interrupt, 1: X high event has occurred)

8.62 CLICK_THS (3Ah)

Table 121. CLICK_THS register

-	Ths6	Ths5	Ths4	Ths3	Ths2	Ths1	Ths0

Table 122. CLICK_SRC description

Ths6-Ths0	Click threshold. Default value: 000 0000

8.63 TIME_LIMIT (3Bh)

Table 123. TIME_LIMIT register

-	TLI6	TLI5	TLI4	TLI3	TLI2	TLI1	TLI0

Table 124. TIME_LIMIT description

TLI7-TLI0	Click time limit. Default value: 000 0000

8.64 TIME_LATENCY (3Ch)

Table 125. TIME_LATENCY register

TLA7	TLA6	TLA5	TLA4	TLA3	TLA2	TLA1	TLA0

Table 126. TIME_LATENCY description

TLA7-TLA0	Click time latency. Default value: 0000 0000

8.65 TIME WINDOW (3Dh)

Table 127. TIME_WINDOW register

TW7	TW6	TW5	TW4	TW3	TW2	TW1	TW0

Table 128. TIME_WINDOW description

TW7-TW0	Click time window

8.66 Act_THS (3Eh)

Table 129. TIME_WINDOW register

--	Acth6	Acth5	Acth4	Acth3	Acth2	Acth1	Acth0

Table 130. TIME_WINDOW description

Acth[6:0]	Sleep-to-Wake, Return-to-Sleep activation threshold 1 LSb = 16 mg

8.67 Act_DUR (3Fh)

Table 131. Act_DUR register

ActD7	ActD6	ActD5	ActD4	ActD3	ActD2	ActD1	ActD0

Table 132. Act_DUR description

ActD[7:0]	Sleep-to-Wake, Return-to-Sleep duration DUR = (Act_DUR + 1)*8/ODR

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 133. LGA 4x4x1 mm 24-lead mechanical data (see note 1 and 2)

Databook				
Symbol	**Min.**	**Typ.**	**Max.**	**Note**
A			1.070	
A1	0.000	-	0.050	4
b		0.200		7
D		4.000		6
D2		1.750		
E		4.000		6
E2		1.750		
e1		0.500		
e2		2.500		
L		0.350		7
L1	-	0.100	-	
L2	-	0.100	-	
N		24		5
R1	-	0.080	-	

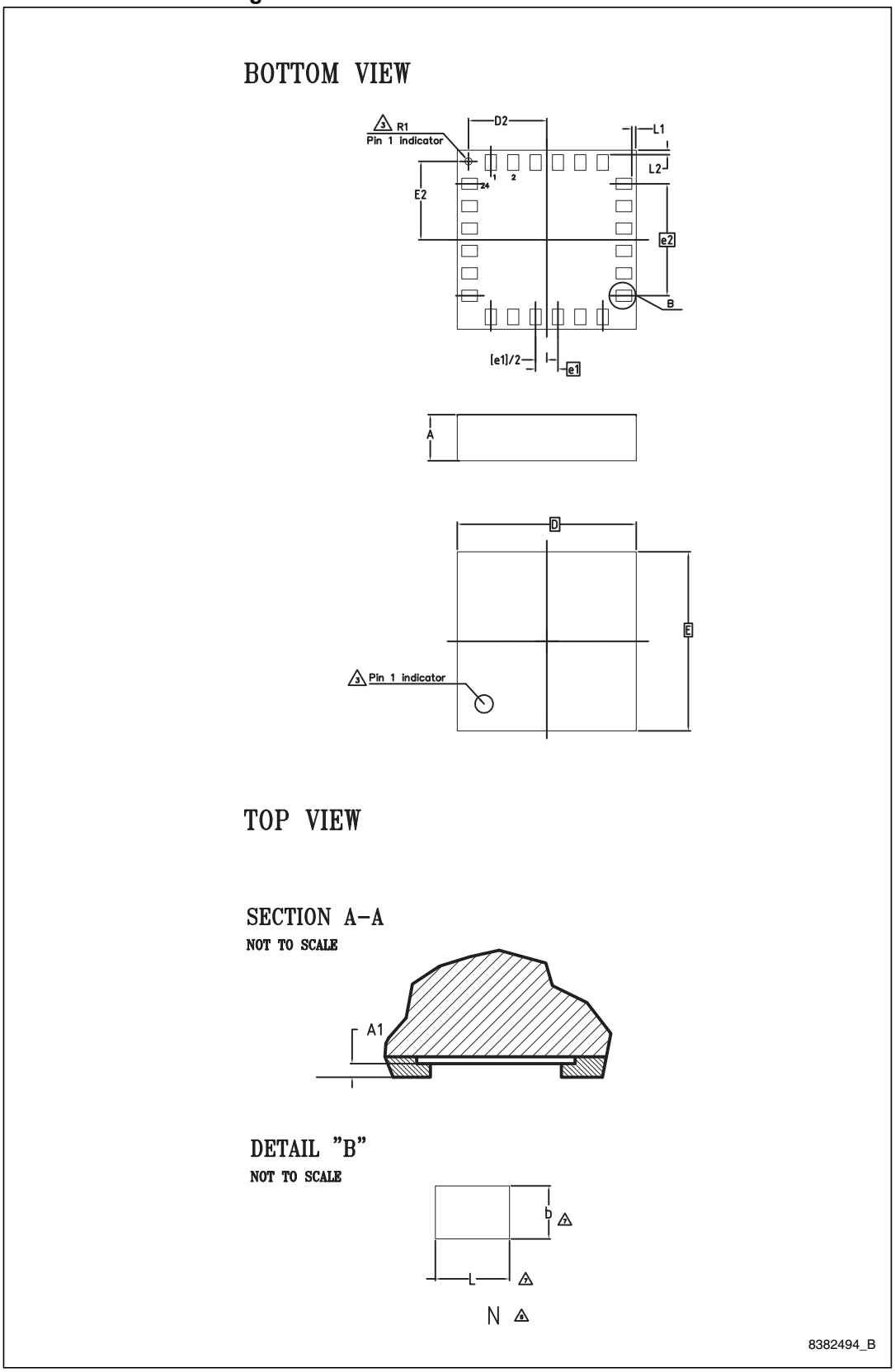
Symbol	**Tolerance of Form and Position**
	Databook
D/E	0.15
Notes	1 and 2
REF	-

Δ

Note:

1. *Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.*
2. *All dimensions are in millimeters.*
3. *The “Pin 1 Indicator” is identified on top and/or bottom surfaces of the package.*
4. *A1 is defined as the distance from the seating plane to the land.*
5. *“N” is the maximum number of terminal positions for the specified body size.*
6. *The tolerance of the typical value is specified in table "Tolerance of Form and Position".*
7. *Dimensions “b” and “L” are specified:*
   For solder mask defined: at terminal plating surface
   For non-solder mask defined: at solder mask opening

Figure 21. LGA 4x4x1 mm 24-lead outline



10 Revision history

Table 134. Document revision history

Date	Revision	Changes
24-Jun-2013	1	Initial release
05-Aug-2013	2	Updated LA_So in *Table 3* Updated *Figure 4*, *Figure 5*, and *Table 7* Updated *Section 5.1* Updated *Section 9: Package information* Minor textual updates throughout *Section 8: Register description*

19-2556; Rev 1; 10/02

EVALUATION KIT AVAILABLE

Switch-Mode 1-Cell Li+ Chargers

General Description

The MAX1925/MAX1926 single-cell lithium-ion (Li+) switch-mode battery chargers use an external PMOS pass element step-down configuration. Charge current is programmable, and an external capacitor sets the maximum charge time.

Additional features include automatic input power detection ($\overline{ACON}$ output), logic-controlled enable, and temperature monitoring with an external thermistor. The MAX1925 disables charging for inputs greater than 6.1V, while the MAX1926 charges for inputs between 4.25V and 12V.

The MAX1925/MAX1926 feature two precondition levels to restore near-dead cells. The devices source 4mA to a cell that is below 2V while sourcing C/10 to a cell between 2V and 3V. Full charge current is then applied above 3V. A $\overline{CHG}$ output drives an LED to indicate charging (LED on) and fault conditions (LED blinking).

The MAX1925/MAX1926 are available in a 12-pin 4mm × 4mm thin QFN package and are specified over the extended temperature range (-40°C to +85°C). An evaluation kit is available to speed design.

Applications

Digital Cameras

Self-Charging Battery Packs

PDAs

Cradle Chargers

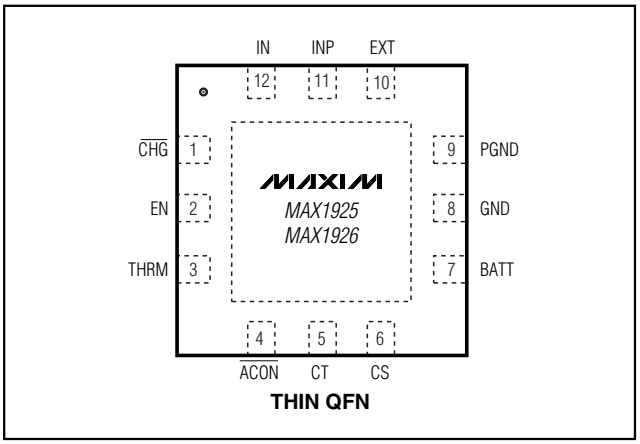
Features

- **Small (4mm × 4mm) Package**
- **4.25V to 12V Input Range (MAX1926)**
- **Overvoltage Lockout at 6.1V (MAX1925)**
- **±0.75% Battery Regulation Voltage**
- **Set Charge Current with One Resistor**
- **Automatic Input Power Sense**
- **LED (or Logic-Out) Charge Status and Fault Indicator**
- **Programmable Safety Timer**
- **Autorestart at Cell = 4V**
- **Thermistor Monitor Input**

Ordering Information

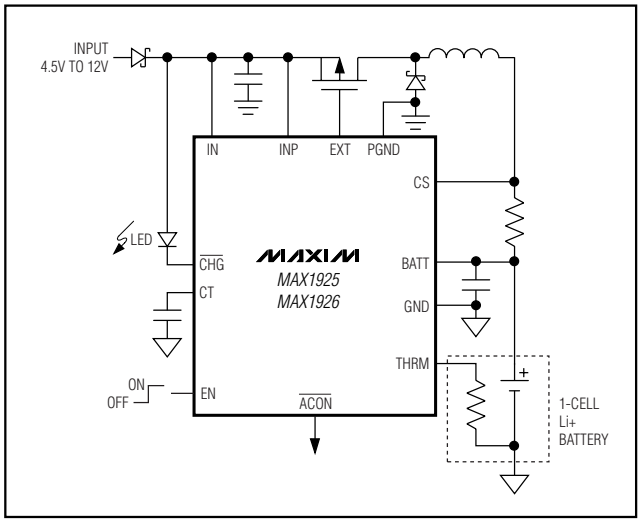
PART	TEMP RANGE	PIN-PACKAGE	INPUT CHARGING RANGE
MAX1925ETC	-40°C to +85°C	12 Thin QFN 4mm x 4mm	4.5V to 6.1V
MAX1926ETC	-40°C to +85°C	12 Thin QFN 4mm x 4mm	4.25V to 12V

Pin Configuration



THIN QFN

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

IN, INP, $\overline{ACON}$ to GND .....-0.3V to +14V
$\overline{CHG}$, EXT to PGND .....-0.3V to (V_{INP} + 0.3V)
CS, BATT, EN, THRM to GND .....-0.3V to +6V
CT to GND .....-0.3V to +4V
EN, THRM, CT to IN.....-14V to +0.3V
INP to IN .....-0.3V to +0.3V
PGND to GND .....-0.3V to +0.3V
CS to BATT .....-0.3V to +0.3V
EXT Continuous RMS Current.....±100mA

Continuous Power Dissipation (T_A = +70°C)
Exposed Paddle Soldered to Board
(derate 16.9mW/°C above +70°C).....1349mW
Exposed Paddle Unsoldered
(derate 9mW/°C above +70°C).....721mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{PGND} = V_{GND} = 0, V_{INP} = V_{IN} = $V_{\overline{CHG}}$ = 5V, V_{BATT} = V_{CS} = V_{EN} = 4V, THRM = 10kΩ to GND, C_{CT} = 100nF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{INP}, V_{IN} (MAX1925 does not charge above 6.1V)		4.5		12.0	V
$\overline{ACON}$ Trip Point	V_{INP}, V_{IN} rising	MAX1925	4.30	4.50	4.78	V
		MAX1926	4.00	4.25	4.50	
	V_{INP}, V_{IN} falling	MAX1925	4.17	4.30	4.43	
		MAX1926	3.90	4.15	4.40	
INP, IN Shutdown Threshold	MAX1925	Rising	5.8		6.4	V
		Falling	5.3		5.9	
EN Input Resistance	MAX1926 internally pulled up to 3V		125	300	550	kΩ
EN Leakage Current	MAX1925		-1		+1	µA
EN Logic Input High Threshold			2			V
EN Logic Input Low Threshold					0.8	V
BATT + CS Input Current (Total Current into BATT and CS)	DONE state, V_{BATT} = 4.1V			25	50	µA
	EN = GND (Note 1)			2	10	
	V_{BATT} = V_{INP} = V_{IN} = 4V, shutdown (Note 1)			2	10	
CS Input Current	Charging			39		µA
IN + INP Total Input Current	EN = GND			5	8	mA
	V_{BATT} = V_{INP} = V_{IN} = 4V, shutdown			2	10	µA
	V_{BATT} = 4.1V; charging				10	mA
	V_{BATT} = 4.3V; done			5	8	
VOLTAGE LOOP						
Voltage Loop Set Point			4.1685	4.2000	4.2315	V
Voltage Loop Hysteresis				15		mV
BATT Prequal1 Voltage Threshold			1.9	2	2.1	V
BATT Prequal2 Voltage Threshold			2.85	3	3.15	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{PGND} = V_{GND} = 0, V_{INP} = V_{IN} = $V_{\overline{CHG}}$ = 5V, V_{BATT} = V_{CS} = V_{EN} = 4V, THRM = 10kΩ to GND, C_{CT} = 100nF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Restart Threshold	Charging restarts when BATT falls to this point	3.92	4.00	4.08	V
BATT Voltage Fault Threshold	If BATT exceeds this threshold, EXT is high (external MOSFET is off) and $\overline{CHG}$ blinks	4.275	4.350	4.425	V
CURRENT LOOP					
CS - BATT Sense Threshold	V_{CS} - V_{BATT}, average value	132	142	152	mV
	Rise/fall hysteresis		30		
Prequal1 Charge Current	V_{BATT} < 2V	3	4	6	mA
Prequal2 CS - BATT Sense Threshold	Average value, 2V < V_{BATT} < 3V (charge current is C/10)		14		mV
	Rise/fall hysteresis, 2V < V_{BATT} < 3V		12		
Current Threshold for Full-Battery Indication	I_{LOAD} falling, as percentage of fast charge current	6	12	20	%
DRIVER FUNCTIONS					
EXT Sink/Source Current			1		A
EXT On-Resistance	EXT high or low		5	12	Ω
Nominal Switching Frequency	V_{BATT} = 3.6V, L =10µH		235		kHz
TIMER FUNCTIONS					
Full-Time Timeout - t_{FULL}	C_{CT} = 100nF		3.02		hours
Prequal1 Timeout	C_{CT} = 100nF		$t_{FULL/1088}$ (10s)		s
Prequal2 Timeout	C_{CT} = 100nF		$t_{FULL/17}$ (10.67 min)		min
Timer Accuracy	C_{CT} = 100nF for 3 hours	-15		+15	%
$\overline{CHG}$ Output Low Current	$V_{\overline{CHG}}$ = 1V	7	10	14	mA
$\overline{CHG}$ Output High Leakage Current	$V_{\overline{CHG}}$ = 12V			1	µA
$\overline{CHG}$ Blink Rate - Fault	Fault state (50% duty cycle), C_{CT} = 100nF		0.5		Hz
$\overline{ACON}$ High Leakage	$V_{\overline{ACON}}$ = 12V		0.01	1.00	µA
$\overline{ACON}$ Sink Current	$V_{\overline{ACON}}$ = 0.4V	2			mA
THERMISTOR MONITOR (Note 2)					
THRM Sense Current for Hot Qualification		344.1	352.9	361.7	µA
THRM Sense Current for Cold Qualification		47.58	48.80	50.02	µA
THRM Sense-Voltage Trip Point	(Note 3)	1.386	1.400	1.414	V

ELECTRICAL CHARACTERISTICS

(V_{PGND} = V_{GND} = 0, V_{INP} = V_{IN} = $V_{\overline{CHG}}$ = 5V, V_{BATT} = V_{CS} = V_{EN} = 4V, THRM = 10kΩ to GND, C_{CT} = 100nF, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{INP}, V_{IN} (MAX1925 does not charge above 6.1V)		4.5		12.0	V
$\overline{ACON}$ Trip point	V_{INP}, V_{IN} rising	MAX1925	4.30		4.78	V
		MAX1926	4.0		4.5	
	V_{INP}, V_{IN} falling	MAX1925	4.17		4.43	
		MAX1926	3.9		4.4	
INP, IN Shutdown Threshold	MAX1925	Rising	5.8		6.4	V
		Falling	5.3		5.9	
EN Input Resistance	MAX1926 internally pulled up to 3V		125		550	kΩ
EN Leakage Current	MAX1925		-1		+1	µA
EN Logic Input High Threshold			2			V
EN Logic Input Low Threshold					0.8	V
BATT + CS Input Current (Total Current into BATT and CS)	DONE State, V_{BATT} = 4.1V				50	µA
	EN = GND (Note 2)				10	
	V_{BATT} = V_{INP} = V_{IN} = 4V, shutdown (Note 1)				10	
IN + INP Total Input Current	EN = GND				8	mA
	V_{BATT} = V_{INP} = V_{IN} = 4V, shutdown				10	µA
	V_{BATT} = 4.1V, charging				10	mA
	V_{BATT} = 4.3V, done				8	
VOLTAGE LOOP						
Voltage Loop Set Point			4.158		4.242	V
BATT Prequal1 Voltage Threshold			1.9		2.1	V
BATT Prequal2 Voltage Threshold			2.85		3.15	V
Restart Threshold	Charging restarts when BATT falls to this point		3.92		4.08	V
BATT Voltage Fault Threshold	If BATT exceeds this threshold, EXT is high (external MOSFET is off) and $\overline{CHG}$ blinks		4.275		4.425	V
CURRENT LOOP						
CS - BATT Sense Threshold	V_{CS} - V_{BATT}, average value		127		157	mV
Prequal1 Charge Current	V_{BATT} < 2V		3		6	mA
Current Threshold for Full-Battery Indication	I_{LOAD} falling, as percentage of fast charge current		4		20	%
DRIVER FUNCTIONS						
EXT On-Resistance	EXT high or low				12	Ω
TIMER FUNCTIONS						
Timer Accuracy	C_{CT} = 100nF for 3 hours		-16		+16	%
$\overline{CHG}$ Output Low Current	$V_{\overline{CHG}}$ = 1V		7		14	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{PGND} = V_{GND} = 0, V_{INP} = V_{IN} = $V_{\overline{CHG}}$ = 5V, V_{BATT} = V_{CS} = V_{EN} = 4V, THRM = 10kΩ to GND, C_{CT} = 100nF, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CHG}$ Output High Leakage Current	$V_{\overline{CHG}}$ = 12V			1	µA
$\overline{ACON}$ High Leakage	$V_{\overline{ACON}}$ = 12V			1	µA
$\overline{ACON}$ Sink Current	$V_{\overline{ACON}}$ = 0.4V	2			mA
THERMISTOR MONITOR					
THRM Sense Current for Hot Qualification		342		363	µA
THRM Sense Current for Cold Qualification		47.3		50.3	µA
THRM Sense-Voltage Trip Point	(Note 3)	1.379		1.421	V

Note 1: When the AC adapter is unplugged or if the charger is shut down, BATT drain is less than 10µA.

Note 2: These specifications guarantee the thermistor interface detects a fault at the correct temperature (0°C to +5°C cold temperature and 45°C to +50°C hot temperature) with Philips NTC Thermistor Series 640-6, 2322-640-63103, 10.0K at +25°C, ±5% (or equivalent).

Note 3: A fault is generated if V_{THRM} lower than 1.4V during the cold test or higher than 1.4V during the hot test. Hot and cold tests occur on alternate CT clock transitions.

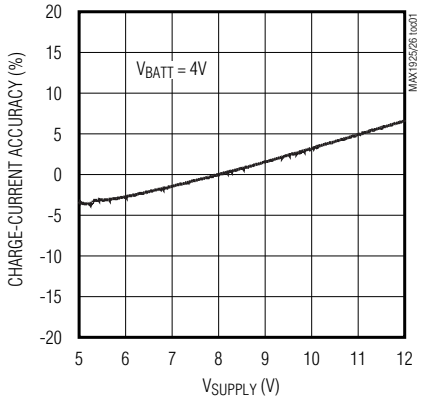
Note 4: Specifications to -40°C are guaranteed by design and not production tested.

Switch-Mode 1-Cell Li+ Chargers

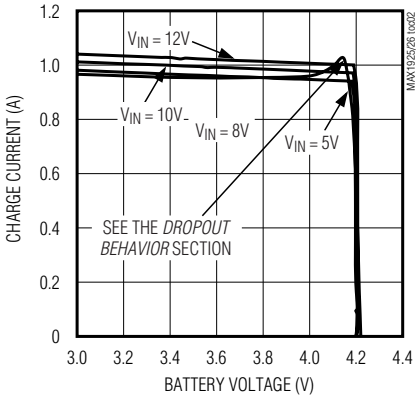
Typical Operating Characteristics

(Circuit of Figure 1, V_{SUPPLY} = 5V, V_{BATT} = 4V, T_A = +25°C, unless otherwise noted.)

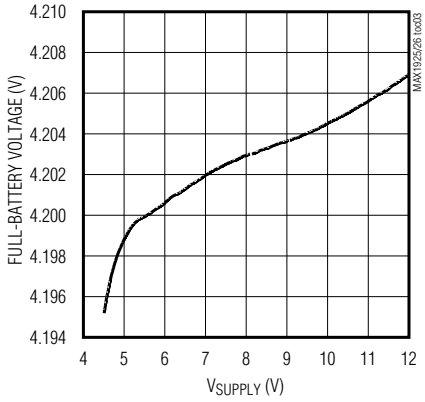
CHARGE-CURRENT ACCURACY vs. SUPPLY VOLTAGE



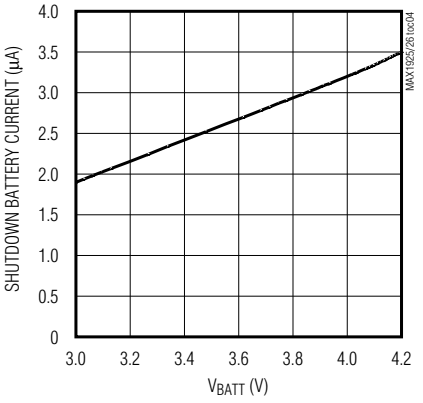
CHARGE CURRENT vs. BATTERY VOLTAGE



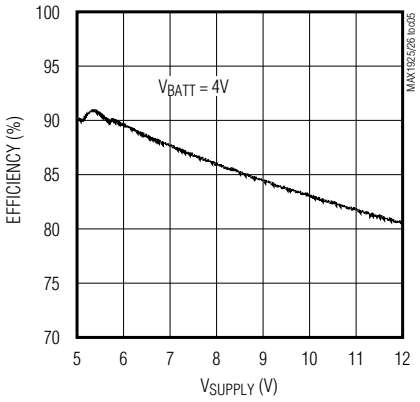
FULL-BATTERY VOLTAGE vs. SUPPLY VOLTAGE



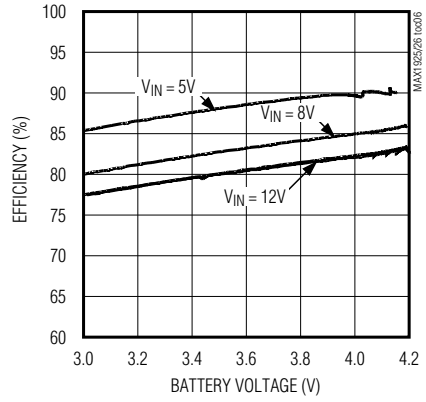
SHUTDOWN BATTERY CURRENT vs. BATTERY VOLTAGE



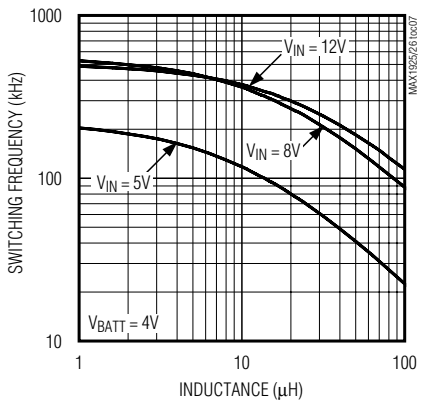
EFFICIENCY vs. SUPPLY VOLTAGE



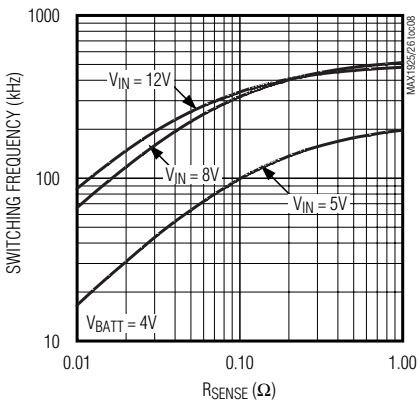
EFFICIENCY vs. BATTERY VOLTAGE



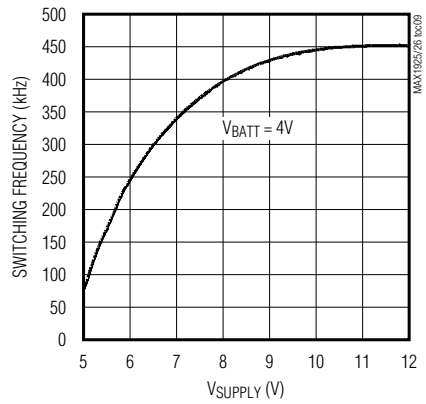
SWITCHING FREQUENCY vs. INDUCTANCE



SWITCHING FREQUENCY vs. RSENSE



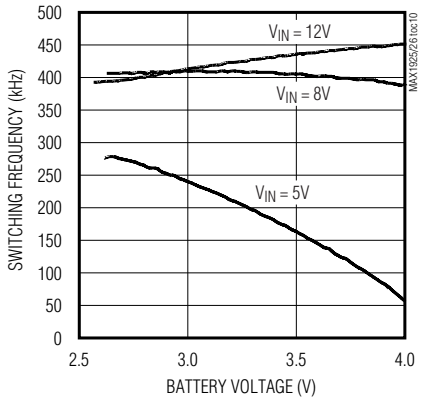
SWITCHING FREQUENCY vs. SUPPLY VOLTAGE



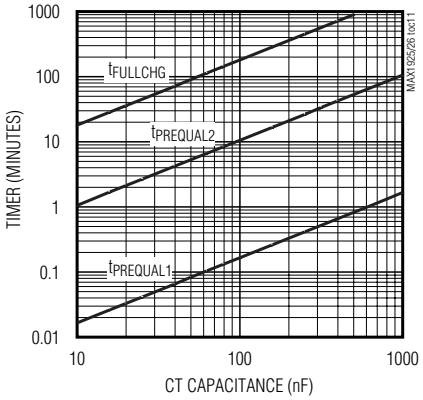
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{SUPPLY} = 5V, V_{BATT} = 4V, T_A = +25°C, unless otherwise noted.)

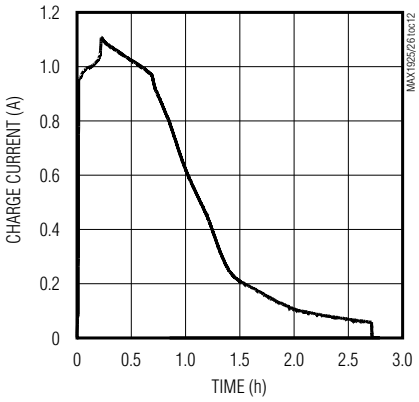
FREQUENCY vs. BATTERY VOLTAGE



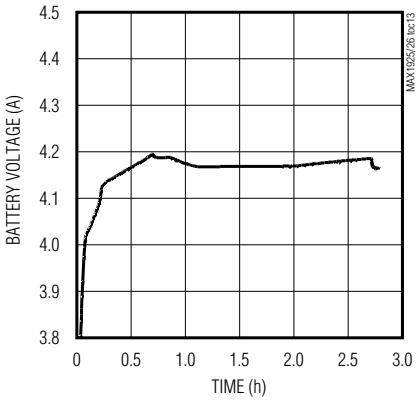
TIMER vs. CT CAPACITANCE



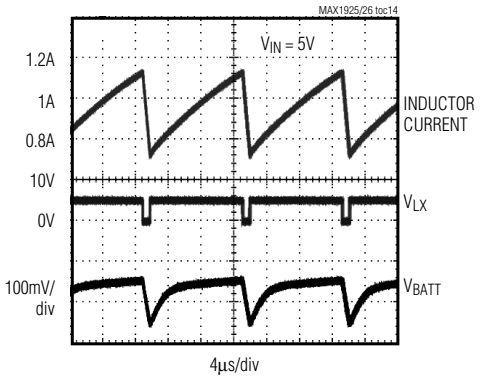
CHARGE CURRENT vs. TIME



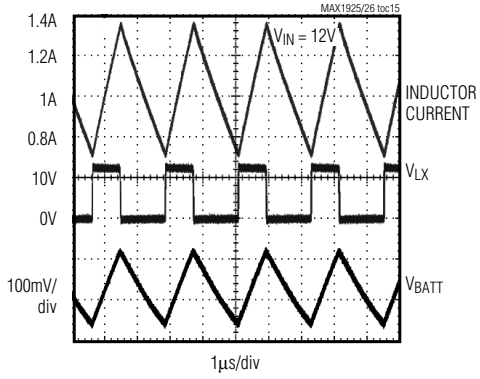
BATTERY VOLTAGE vs. TIME



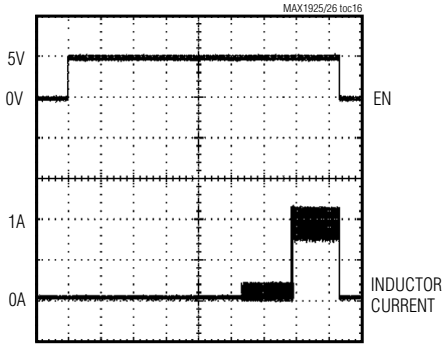
SWITCHING WAVEFORM



SWITCHING WAVEFORM



CHARGE-ENABLE REPSONSE



Pin Description

PIN	NAME	FUNCTION
1	$\overline{CHG}$	Charge Status LED Driver. Open-drain LED driver sinks 10mA when the MAX1925/MAX1926 are charging. $\overline{CHG}$ also blinks at a 0.5Hz rate during fault states (see the *Timing* section). High impedance when charger is in shutdown. See Tables 1 and 2.
2	EN	Enable. Drive EN high to enable charger. Logic level input for normal ON/OFF control. In the MAX1926 EN is internally pulled up to 3V with a 300kΩ resistor.
3	THRM	Thermistor Input. Monitors external thermistor (10kΩ at +25°C). When external temperature is lower than 0°C or above +50°C, charging stops and the charger enters fault mode. Charging resumes when the temperature returns to normal. During a temperature fault the MAX1926 blinks the $\overline{CHG}$ output, while MAX1925 $\overline{CHG}$ remains off (high).
4	$\overline{ACON}$	Power-OK Indicator Output. Open-drain output goes low when AC adapter power is valid. See Table 2 for $\overline{ACON}$ states.
5	CT	Timing Capacitor Connection. Connect timer cap to program full-charge safety timeout interval and prequalification fault times. Timeouts with C_{CT} = 100nF are: Full Timer ($t_{FULLCHG}$): 3 hours—If FASTCHG is not completed within this time a fault is asserted. Prequal2 Timer: Full Timer/17 (10.67 min) Prequal1 Timer: Full Timer/1088 (10s)
6	CS	Charge-Current Sense Input. 142mV nominal regulation threshold. CS is high impedance during shutdown.
7	BATT	Battery-Sense Input. Also negative side of charge-current sense. BATT is high impedance during shutdown.
8	GND	Ground
9	PGND	Power Ground
10	EXT	PMOS Gate-Driver Output. Drives gate of external PMOS switching transistor from IN to GND. When using the MAX1926, ensure that the MOSFET V_{GS} rating is greater than V_{IN}.
11	INP	Supply Voltage Input
12	IN	Supply-Sense Input. Connect IN to INP.

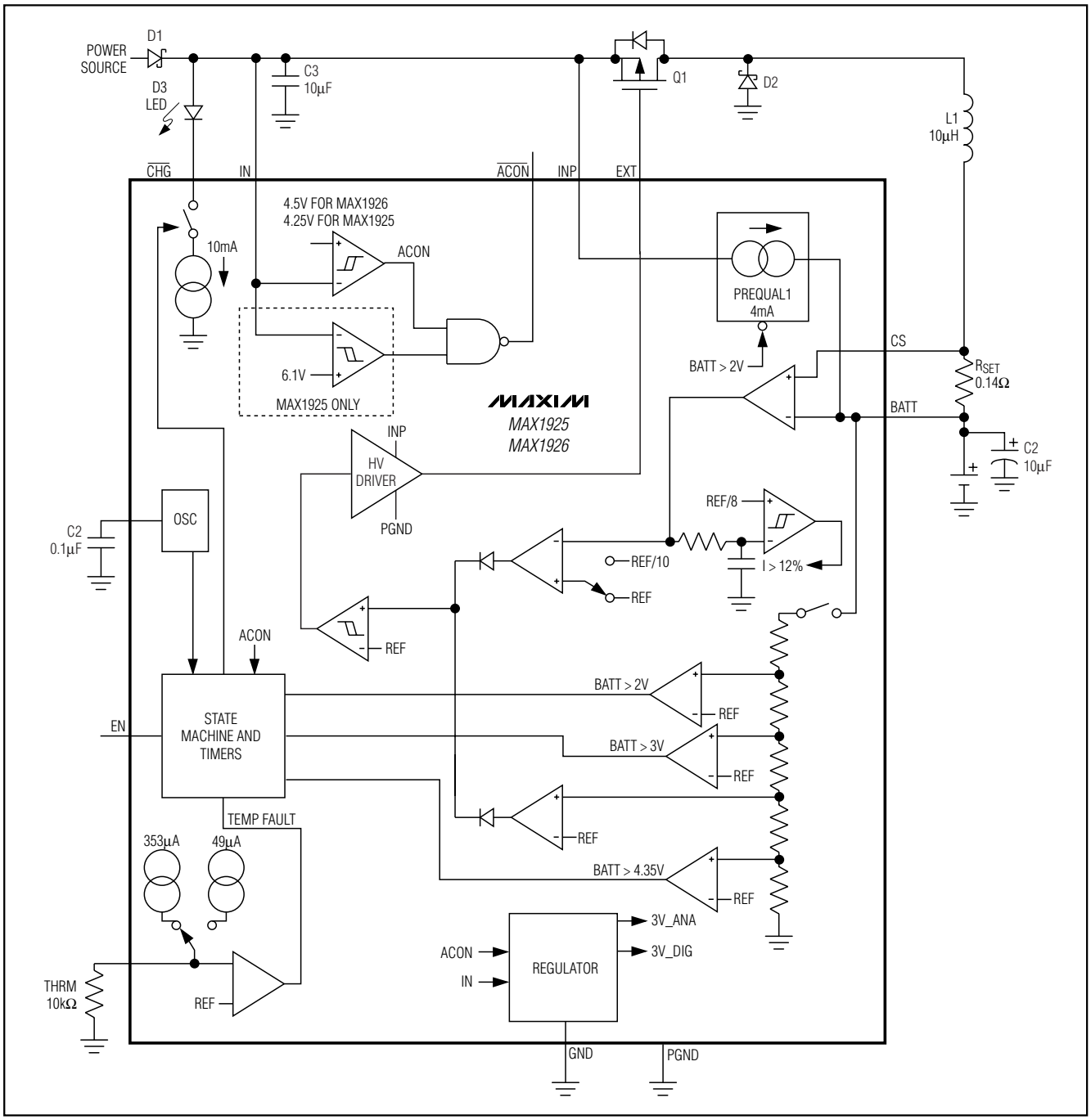


Figure 1. Functional Diagram

Switch-Mode 1-Cell Li+ Chargers

Detailed Description

The MAX1925/MAX1926 switch-mode battery chargers form a complete solution for a single-cell Li+ battery. The devices include battery undervoltage/overvoltage fault protection. The MAX1925/MAX1926 use EN and THRM for shutdown, battery detection, and temperature monitoring. The devices provide outputs to indicate charge status ($\overline{CHG}$) and presence of input power ($\overline{ACON}$).

The MAX1925/MAX1926 include two prequalification modes that must be passed before the charger enters the fast-charge state. During fast charge, the charger operates initially in constant-current mode until the battery voltage reaches 4.2V. When the battery voltage has reached 4.2V, the charger operates in constant-voltage mode. In constant-current mode, the charger acts as a hysteretic current source, controlling the inductor's peak and valley currents. In constant-voltage mode, the charger regulates the peak and valley of the output ripple.

Charge Cycle

The MAX1925/MAX1926 initiate PREQUAL when one of the following occurs:

- When an external power source is connected
- The cell voltage falls to 4V after charging is finished
- EB is toggled
- Input power is cycled

Some Li+ cells can be damaged when fast-charged from a completely dead state. Moreover, an over-discharged cell may indicate a dangerous abnormal cell condition. As a built-in safety feature, the MAX1925/MAX1926 use a two-level prequalification charge to determine if it is safe to charge. When the cell voltage is less than 2V, the cell is charged from an internal

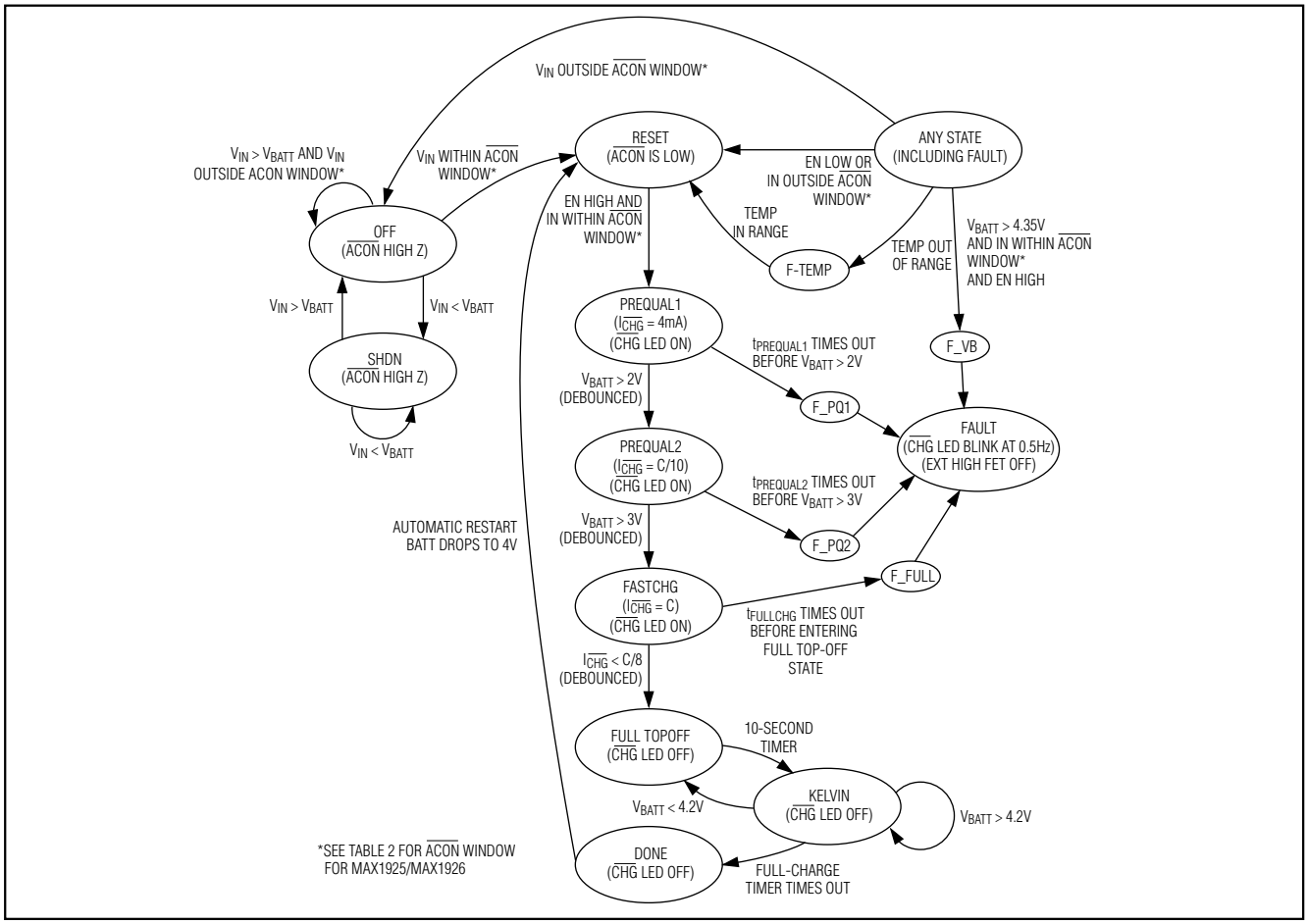


Figure 2. MAX1925/MAX1926 State Diagram

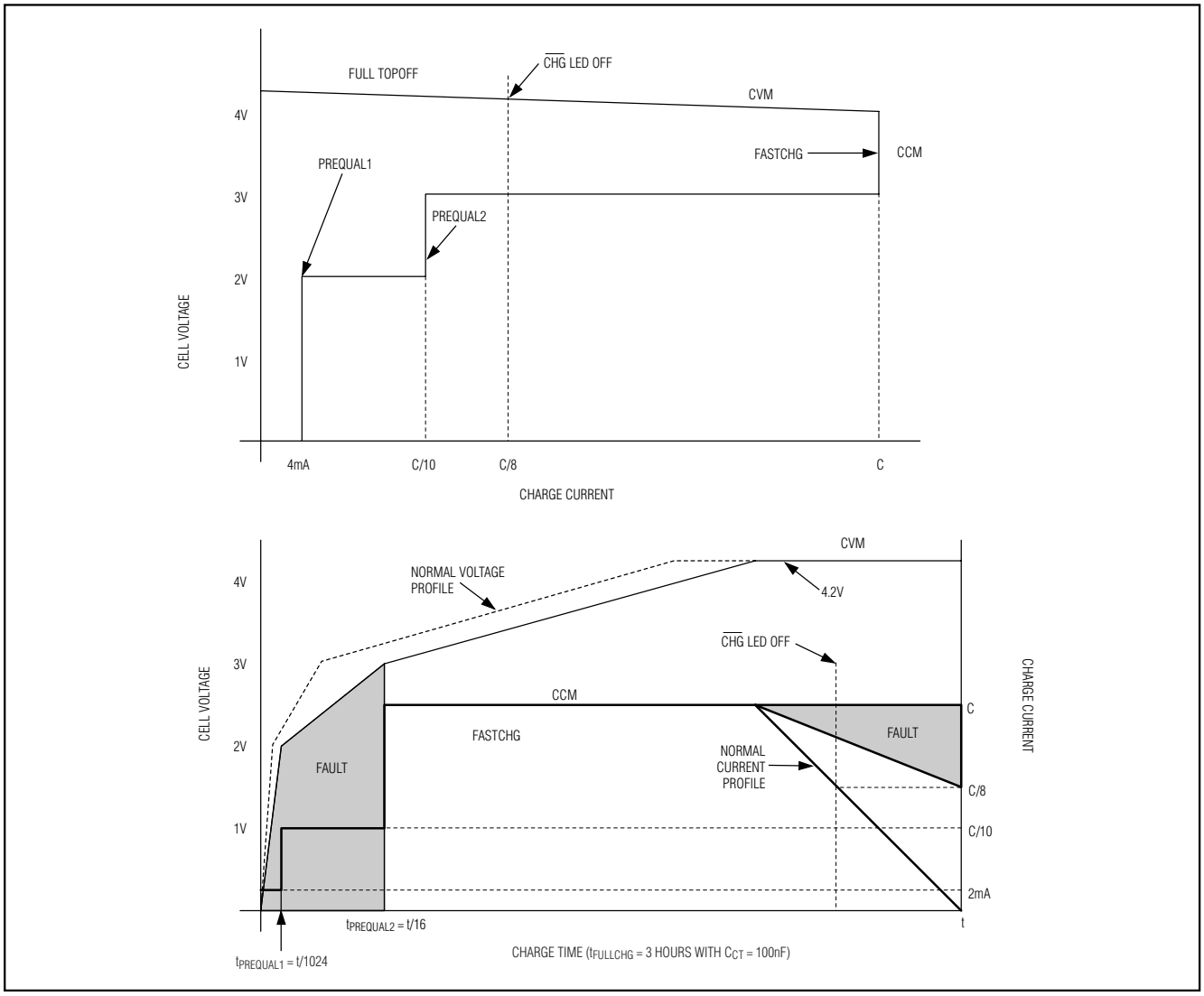


Figure 3. Charging Current and Voltage Timing Diagrams

linear 4mA current source (PREQUAL1). When the cell voltage exceeds 2V, the cell is charged with 10% of the programmed fast-charge current ($I_{FASTCHG}$) until it reaches 3V. When the cell voltage is above 3V, fast charging occurs at the full set current. If the cell fails to reach the next prequalification threshold before a set time (see $t_{PREQUAL1}$ and $t_{PREQUAL2}$ in the *Timer Capacitor and Fault Modes* section), charging stops, a fault alarm is set, and the $\overline{CHG}$ output blinks.

Figures 2 and 3 show charging behavior typical Li+ cell. The MAX1925/MAX1926 remain in fast-charge mode until the battery voltage reaches regulation and the charge current drops below 1/8th of $I_{FASTCHG}$. The charger then enters full topoff mode and the $\overline{CHG}$ LED is turned off. In full topoff mode, the controller continues to operate as in fast-charge mode, except that it remains in constant-voltage mode (CVM) unless the battery voltage falls. After every $t_{PREQUAL1}$ (see the *Timer Capacitor and Fault Modes* section) the charger enters the Kelvin state (for 2 CT clock cycles, 60ms with C_{CT} = 100nF) where charge current is interrupted so that the battery voltage can be accurately measured.

The MAX1925/MAX1926 do not enter done mode until $t_{FULLCHG}$ has been reached. If the battery is removed

and a new battery is connected during either fast-charge or full topoff modes, the charger begins with full charge current without prequalification unless the part is reset. Detect battery insertion by connecting THRM to a thermistor on the battery, if a thermistor is used, or to a 10kΩ resistor linked to a battery door mechanism.

Constant-Current Mode (CCM)

When the battery voltage is below 4.2V, the MAX1925/MAX1926 regulate the charging current by controlling the peak and valley inductor currents. When the inductor current exceeds the 158mV/R_{SET}, the MAX1925/MAX1926 turn the external PFET off. When the inductor current falls below 128mV/R_{SET}, the MAX1925/MAX1926 turns the external PFET on, but only if the battery voltage is below regulation. The maximum cell charging current is programmed by selecting the external R_{SET} (see Figure 1) resistor connected between BATT and CS. Select the external resistor value using RSET = 142mV/$I_{FASTCHG}$.

The accuracy of the charge current is a function of input voltage, battery voltage, inductance, and comparator delay (300ns typ). Determine the charge-current error according to the following equation:

$$\Delta I_{CHG} = \frac{(V_{IN} - 2 \times V_{BATT}) \times t_{IDelay}}{2 \times L}$$

where ΔI_{CHG} is the charge-current error, and t_{IDelay} is the current-sense comparator delay.

For this reason choose L for an on-time and off-time greater than $2 \times t_{IDelay}$ to minimize error in the charging current.

Constant-Voltage Mode (CVM)

In constant-voltage mode (CVM), the controller regulates the peak and valley of the output ripple. The maximum cell voltage is regulated to 4.2V. If, for any reason, the cell voltage exceeds 4.35V, a fault alarm is set, the $\overline{CHG}$ output blinks, and the PFET power switch is held off. The charger can then be restarted only by cycling input power or the EN input.

Indication of Charge Completion ($\overline{CHG}$)

The $\overline{CHG}$ output is a 10mA current-sink output that indicates the cell's charging status. Connect an LED from IN to $\overline{CHG}$ for a visible indicator. Alternatively, a pullup resistor (typically 200kΩ) from a logic supply to $\overline{CHG}$ provides a logic-level output. Table 1 relates the status of the LED to the condition of the charger and battery.

$\overline{ACON}$ Output

The $\overline{ACON}$ open-drain output indicates when usable power is applied to IN. In the MAX1926 when V_{IN} exceeds $\overline{ACON}$ threshold (nominally 4.25V with IN rising—see the *Electrical Characteristics* table), $\overline{ACON}$ goes low. In the MAX1925, $\overline{ACON}$ goes low when the input voltage is between 4.5V and 6.1V (see Table 2).

Re-Initiating a Charging Cycle

The MAX1925/MAX1926 feature automatic restart that resumes charging when the cell voltage drops to 4V and t_{FULL_CHG} is completed. By automatically resuming charg-

Table 1. $\overline{CHG}$ Output States

STATE	CONDITION	$\overline{CHG}$
OFF	EN low or no battery or input power	High impedance (LED off)
PREQUAL1	Charge current = 4mA until BATT reaches 2V.	Low (LED on)
PREQUAL2	Charge current = C/10 until BATT reaches 3V.	Low (LED on)
FAST CHARGE	Charge current = C = 142mV/R_{SET}.	Low (LED on)
FULL CHARGE	Charge current has fallen to C/8.	High impedance (LED off)
FAULT PREQUAL1	BATT does not reach 2V before PREQUAL1 timeout.	Blinking. LED on 50% f_{BLINK} (0.5Hz). Can only be cleared by cycling input power, THRM, or EN.
FAULT PREQUAL2	BATT does not reach 3V before PREQUAL2 timeout.	
FAULT FULL	Charge current does not drop to C/8 before FULL CHARGE timeout.	
FAULT BATT VOLTAGE	Battery voltage has exceeded 4.35V.	Blinking. LED on 50% f_{BLINK} (0.5Hz).
FAULT TEMP	Temperature has risen above +50°C or fallen below 0°C. Temp fault clears by itself.	MAX1925—High impedance (LED off)
		MAX1926—Blinking (LED on 50% 0.5Hz)
NONE	Initial power-up or enable with battery not present.	Blinking at rapid rate as charger cycles through RESET, PREQUAL1, and DONE.

Table 2. $\overline{ACON}$ Behavior vs. V_{IN}

PART	V_{IN}	$\overline{ACON}$	CHARGING	$\overline{CHG}$ LED
MAX1925	V_{IN} > $V_{\overline{ACON}}$ threshold (4.5V nom) and < 6.1V, and V_{IN} > V_{BATT}	LOW	YES	ON (until charge complete)
	V_{IN} > $V_{\overline{ACON}}$ threshold and V_{IN} < V_{BATT} (Note: This state should never occur)	High Z	NO	OFF
	V_{IN} < $V_{\overline{ACON}}$ threshold	High Z	NO	OFF
MAX1926	V_{IN} > $V_{\overline{ACON}}$ threshold (4.25V nom) and V_{IN} > V_{BATT}	LOW	YES	ON (until charge complete)
	V_{IN} > $V_{\overline{ACON}}$ threshold and V_{IN} < V_{BATT} (Note: This state should never occur)	High Z	NO	OFF
	V_{IN} < $V_{\overline{ACON}}$ Threshold	High Z	NO	OFF

ing when the battery voltage drops, the MAX1925/MAX1926 ensure that the cell does not remain partially charged after use when charger power is available.

Charging also restarts if input power is cycled or if the charger is restarted by the EN or THRM input. If a new battery is inserted, the charger must be restarted. If the THRM functionality is used, the charger is automatically restarted upon battery insertion. When THRM is not used, toggle EN or connect THRM through a resistor to be grounded with a battery-door latch switch.

Applications Information

Timer Capacitor and Fault Modes

The on-chip timer checks charge progress and issues an alarm signal through a blinking $\overline{CHG}$ output when one of the safety timers times out (see Table 1). All timers are set by one external capacitor at CT. A 100nF value sets the full-charge timer ($t_{FULLCHG}$) to 3 hours, the $t_{PREQUAL1}$ timer to ($t_{FULLCHG}$)/1088 (10s), and the $t_{PREQUAL2}$ timer at ($t_{FULLCHG}$)/17 (10.67 minutes).

If the charger enters full-charge state (after the charging current has fallen below C/8) before the full-charge timer expires, no fault occurs, but if the timer expires before full charge is reached, a fault is indicated (see Table 1).

A fault is also indicated if the battery voltage exceeds 4.35V. When the cell voltage exceeds 4.35V a fault alarm is set, the $\overline{CHG}$ output blinks, and the PFET turns off.

To restart the charger after a fault occurs, the fault state must be cleared by toggling EN, or by cycling input power at IN (see Figure 1). Temperature faults do not need to be cleared by EN. The MAX1925/MAX1926 resume charging after the temperature returns to within the set window.

Inductor Selection

Because the MAX1925/MAX1926 is hysteretic, the constant-current mode switching frequency is a function of the inductance, sense resistance, and current-sense hysteresis (30mV, from the *Electrical Characteristics*). To minimize charge-current error:

$$L > \frac{(V_{IN} - 2 \times V_{BATT}) \times t_{Delay}}{2 \times \Delta I_{CHG}}$$

where ΔI_{CHG} is the acceptable charge-current error and should usually be less than 1/4th the full charge current. t_{IDelay} is the current-sense comparator delay (300ns typical). Calculate L for $V_{IN} = V_{IN,MAX}$, $V_{BATT} = V_{BATT,MIN}$, with positive ΔI_{CHG} and $V_{IN} = V_{IN,MIN}$, $V_{BATT} = V_{BATT,MAX}$, with negative ΔI_{CHG}. Use the larger calculated value for L.

The resulting switching frequency in CCM is:

$$f_{Switch} > \left(\frac{I_{HYST} \times L + t_{IDelay} V_{BATT}}{V_{IN} - V_{BATT}} + 2 \times t_{IDelay} + \frac{I_{HYST} \times L + t_{IDelay} \times (V_{IN} - V_{BATT})}{V_{BATT}} \right)^{-1}$$

Choose an inductor with an RMS and saturation current rating according to the following equation:

$$I_{SAT/RMS} > \frac{V_{IPK}}{R_{SET}} + \frac{(V_{IN} - V_{BATT}) t_{IDelay}}{L}$$

where V_{IPK} is the peak current-sense threshold (158mV typ).

Output Capacitor Selection

The ESR of the output capacitor influences the switching frequency of the charger during voltage regulation

mode. To ensure stable transition from CCM to CVM choose a capacitor with the following ESR:

$$R_{ESR} > \frac{V_{VHIST}}{V_{IHIST}} \times R_{SET}$$

where V_{VHIST} is the voltage hysteresis (15mV typ) and V_{IHIST} is the current-sense threshold hysteresis (typically 30mV). Tantalum capacitors are recommended. However a ceramic capacitor (typically 10µF) with a series resistor can also be used.

MOSFET Selection

The MAX1925/MAX1926 drive an external P-channel MOSFET's gate from IN to GND. Choose a P-channel MOSFET with a $|V_{DS,MAX}| > V_{IN}$. Since EXT drives from rail to rail the MOSFET must also be rated for $|V_{GS,MAX}| > V_{IN}$. At the lower operating frequencies and currents for typical MAX1925/MAX1926 applications resistive and diode losses dominate switching losses. For this reason choose a MOSFET with a low R_{DSON}. The resistive losses are:

$$P_{Resistive\_losses} \cong D \times I_{CHG}^2 \times R_{DSON} + I_{CHG}^2 \times (R_{SET} + R_L)$$

where D is the operating duty cycle (V_{OUT}/V_{IN}) and R_L is the inductor resistance. The MOSFET's power dissipation must exceed $D \times I_{CHG}^2 \times R_{DSON}$.

Diode Selection

In the event of a short-circuited source, the body diode inherent in the external PFET allows the cell to discharge. To prevent this and to protect against negative input voltages, add a Schottky or silicon diode between the power source and IN.

The MAX1925/MAX1926 use a diode for catching the inductor current during the off cycle. Select a Schottky diode with a current rating greater than V_{IPK}/R_{SET} and a voltage rating greater than V_{IN}.

Dropout Behavior

The MAX1925/MAX1926 regulate charging current by ramping inductor current between upper and lower thresholds, typically 128mV and 158mV across R_{SET}. This results in an average current of 142mV/R_{SET}. At input voltages near dropout (4.6V at IN for the typical circuit), the inductor current ramp waveform becomes somewhat flattened as inductor, MOSFET, input diode, and battery resistance limit inductor current. When the inductor current waveform flattens, it's average value rises with respect to the upper and lower current thresholds. This creates a slight peak (about 5%) in charging current at high battery voltages as seen in the Charging Current vs. Battery Voltage plot in the *Typical Operating Characteristics*. Charging current is still controlled in dropout and the charger operates normally. The dropout current peak can be minimized by reducing MOSFET and inductor resistance, as well as forward voltage in the input diode.

Thermistor Interface

An external thermistor inhibits charging by setting a fault flag when the cell is cold (<0°C) or hot (>+50°C). The THRM time-multiplexes two sense currents to test for both hot and cold qualification. Connect the thermistor between THRM and GND. If no temperature qualification is desired, replace the thermistor with a 10kΩ resistor connected through the battery-latch mechanism. The thermistor should be 10kΩ at +25°C and have a negative temperature coefficient, as defined by the expression below:

$$R_T = R_{25°C} \times e^{\left\{\beta\left[\left(\frac{1}{T+273}\right)-\left(\frac{1}{298}\right)\right]\right\}}$$

Table 3 shows nominal fault detection temperatures that result from a wide range of available thermistor temperature curves.

For a given thermistor characteristic, it is possible to adjust the fault-detection temperatures by adding a resistor in series with the thermistor or a parallel resistor from THRM to GND.

Chip Information

TRANSISTOR COUNT: 5722

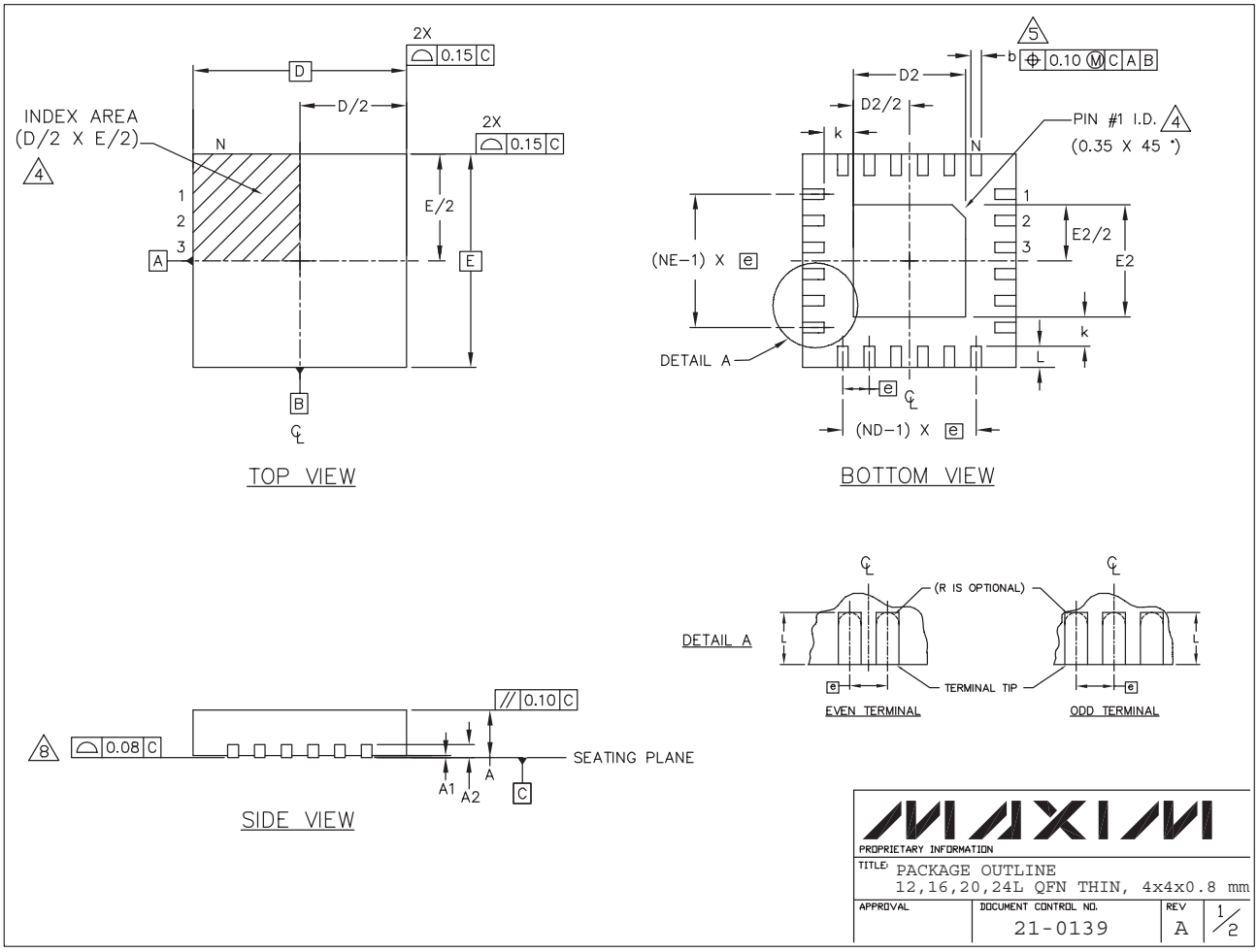
PROCESS: BiCMOS

Table 3. Fault Temperature for Different Thermistors

THERMISTOR BETA	3000	3250	3500	3750
Resistance at +25°C	10000Ω	10000Ω	10000Ω	10000Ω
Resistance at +50°C	4587.78Ω	4299.35Ω	4029.06Ω	3775.75Ω
Resistance at 0°C	25140.55Ω	27148.09Ω	29315.94Ω	31656.90Ω
Nominal Hot Trip Temperature	55.14°C	52.60°C	50.46°C	48.63°C
Nominal Cold Trip Temperature	-3.24°C	-1.26°C	0.46°C	1.97°C

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Switch-Mode 1-Cell Li+ Chargers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS												
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95–1 SPP–012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
12,16,20,24L QFN THIN, 4x4x0.8 mm

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0139	A	2/2

NEO-6

u-blox 6 GPS Modules

Data Sheet

Abstract

Technical data sheet describing the cost effective, high-performance u-blox 6 based NEO-6 series of GPS modules, that brings the high performance of the u-blox 6 positioning engine to the miniature NEO form factor.

These receivers combine a high level of integration capability with flexible connectivity options in a small package. This makes them perfectly suited for mass-market end products with strict size and cost requirements.

16.0 x 12.2 x 2.4 mm

Document Information	
Title	NEO-6
Subtitle	u-blox 6 GPS Modules
Document type	Data Sheet
Document number	GPS.G6-HW-09005-E
Document status	

Document status information	
Objective Specification	This document contains target values. Revised and supplementary data will be published later.
Advance Information	This document contains data based on early testing. Revised and supplementary data will be published later.
Preliminary	This document contains data from product verification. Revised and supplementary data may be published later.
Released	This document contains the final product specification.

This document applies to the following products:

Name	Type number	ROM/FLASH version	PCN reference
NEO-6G	NEO-6G-0-001	ROM7.03	UBX-TN-11047-1
NEO-6Q	NEO-6Q-0-001	ROM7.03	UBX-TN-11047-1
NEO-6M	NEO-6M-0-001	ROM7.03	UBX-TN-11047-1
NEO-6P	NEO-6P-0-000	ROM6.02	N/A
NEO-6V	NEO-6V-0-000	ROM7.03	N/A
NEO-6T	NEO-6T-0-000	ROM7.03	N/A

Contents

1 Functional description

1.1 Overview

The NEO-6 module series is a family of stand-alone GPS receivers featuring the high performance u-blox 6 positioning engine. These flexible and cost effective receivers offer numerous connectivity options in a miniature 16 x 12.2 x 2.4 mm package. Their compact architecture and power and memory options make NEO-6 modules ideal for battery operated mobile devices with very strict cost and space constraints.

The 50-channel u-blox 6 positioning engine boasts a Time-To-First-Fix (TTFF) of under 1 second. The dedicated acquisition engine, with 2 million correlators, is capable of massive parallel time/frequency space searches, enabling it to find satellites instantly. Innovative design and technology suppresses jamming sources and mitigates multipath effects, giving NEO-6 GPS receivers excellent navigation performance even in the most challenging environments.

1.2 Product features

Model	Type					Supply		Interfaces				Features						
	GPS	PPP	Timing	Raw Data	Dead Reckoning	1.75 V - 2.0 V	2.7 V - 3.6 V	UART	USB	SPI	DDC (I²C compliant)	Programmable (Flash) FW update	TCXO	RTC crystal	Antenna supply and supervisor	Configuration pins	Timepulse	External interrupt/ Wakeup
NEO-6G	●					●		●	●	●	●		●	●	o	3	1	●
NEO-6Q	●						●	●	●	●	●		●	●	o	3	1	●
NEO-6M	●						●	●	●	●	●			●	o	3	1	●
NEO-6P	●	●		●			●	●	●	●	●			●	o	3	1	●
NEO-6V	●				●		●	●	●	●	●			●	o	3	1	●
NEO-6T	●		●	●			●	●	●	●	●		●	●	o	3	1	●

o = Requires external components and integration on application processor

Table 1: Features of the NEO-6 Series

☞ All NEO-6 modules are based on GPS chips qualified according to AEC-Q100. See Chapter 5.1 for further information.

1.3 GPS performance

Parameter	Specification			
Receiver type	50 Channels GPS L1 frequency, C/A Code SBAS: WAAS, EGNOS, MSAS			
Time-To-First-Fix[1]		NEO-6G/Q/T	NEO-6M/V	NEO-6P
	Cold Start[2]	26 s	27 s	32 s
	Warm Start[2]	26 s	27 s	32 s
	Hot Start[2]	1 s	1 s	1 s
	Aided Starts[3]	1 s	<3 s	<3 s
Sensitivity[4]		NEO-6G/Q/T	NEO-6M/V	NEO-6P
	Tracking & Navigation	-162 dBm	-161 dBm	-160 dBm
	Reacquisition[5]	-160 dBm	-160 dBm	-160 dBm
	Cold Start (without aiding)	-148 dBm	-147 dBm	-146 dBm
	Hot Start	-157 dBm	-156 dBm	-155 dBm
Maximum Navigation update rate		NEO-6G/Q/M/T	NEO-6P/V	
		5Hz	1 Hz	
Horizontal position accuracy[6]	GPS	2.5 m		
	SBAS	2.0 m		
	SBAS + PPP[7]	< 1 m (2D, R50)[8)]		
	SBAS + PPP[7]	< 2 m (3D, R50)[8]		
Configurable Timepulse frequency range		NEO-6G/Q/M/P/V	NEO-6T	
		0.25 Hz to 1 kHz	0.25 Hz to 10 MHz	
Accuracy for Timepulse signal	RMS	30 ns		
	99%	<60 ns		
	Granularity	21 ns		
	Compensated[9]	15 ns		
Velocity accuracy[6]		0.1m/s		
Heading accuracy[6]		0.5 degrees		
Operational Limits	Dynamics	≤ 4 g		
	Altitude[10]	50,000 m		
	Velocity[10]	500 m/s		

Table 2: NEO-6 GPS performance

[1] All satellites at -130 dBm
[2] Without aiding
[3] Dependent on aiding data connection speed and latency
[4] Demonstrated with a good active antenna
[5] For an outage duration ≤10s
[6] CEP, 50%, 24 hours static, -130dBm, SEP: <3.5m
[7] NEO-6P only
[8] Demonstrated under following conditions: 24 hours, stationary, first 600 seconds of data discarded. HDOP < 1.5 during measurement period, strong signals. Continuous availability of valid SBAS correction data during full test period.
[9] Quantization error information can be used with NEO-6T to compensate the granularity related error of the timepulse signal
[10] Assuming Airborne <4g platform

1.4 Block diagram

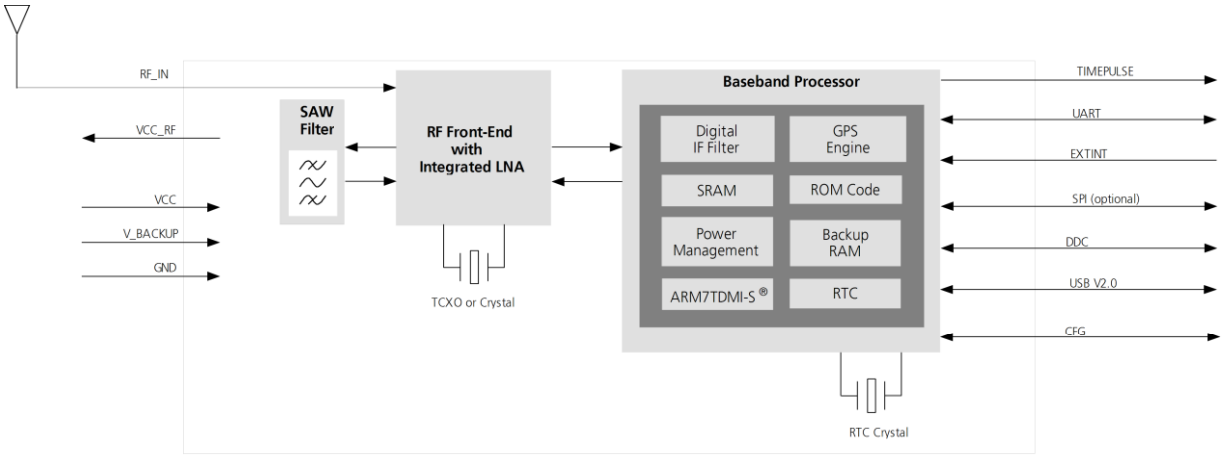


Figure 1: Block diagram (For available options refer to the product features table in section 1.2).

1.5 Assisted GPS (A-GPS)

Supply of aiding information like ephemeris, almanac, rough last position and time and satellite status and an optional time synchronization signal will reduce time to first fix significantly and improve the acquisition sensitivity. All NEO-6 modules support the u-blox AssistNow Online and AssistNow Offline A-GPS services[11] and are OMA SUPL compliant.

1.6 AssistNow Autonomous

AssistNow Autonomous provides functionality similar to Assisted-GPS without the need for a host or external network connection. Based on previously broadcast satellite ephemeris data downloaded to and stored by the GPS receiver, AssistNow Autonomous automatically generates accurate satellite orbital data ("AssistNow Autonomous data") that is usable for future GPS position fixes. AssistNow Autonomous data is reliable for up to 3 days after initial capture.

u-blox' AssistNow Autonomous benefits are:

- Faster position fix
- No connectivity required
- Complementary with AssistNow Online and Offline services
- No integration effort, calculations are done in the background

☞ For more details see the u-blox 6 Receiver Description including Protocol Specification [2].

[11] AssistNow Offline requires external memory.

1.7 Precision Timing

1.7.1 Time mode

NEO-6T provides a special Time Mode to provide higher timing accuracy. The NEO-6T is designed for use with stationary antenna setups. The Time Mode features three different settings described in Table 3: Disabled, Survey-In and Fixed Mode. For optimal performance entering the position of the antenna (when known) is recommended as potential source of errors will be reduced.

Time Mode Settings	Description
Disabled	Standard PVT operation
Survey-In	The GPS receiver computes the average position over an extended time period until a predefined maximum standard deviation has been reached. Afterwards the receiver will be automatically set to Fixed Mode and the timing features will be activated.
Fixed Mode	In this mode, a fixed 3D position and known standard deviation is assumed and the timing features are activated. Fixed Mode can either be activated directly by feeding pre-defined position coordinates (ECEF - Earth Center Earth Fixed format) or by performing a Survey-In. In Fixed mode, the timing errors in the TIMEPULSE signal which otherwise result from positioning errors are eliminated. Single-satellite operation is supported. For details, please refer to the u-blox 6 Receiver Description including Protocol Specification [2].

Table 3: Time mode settings

1.7.2 Timepulse and frequency reference

NEO-6T comes with a timepulse output which can be configured from 0.25 Hz up to 10 MHz. The timepulse can either be used for time synchronization (i.e. 1 pulse per second) or as a reference frequency in the MHz range. A timepulse in the MHz range provides excellent long-term frequency accuracy and stability.

1.7.3 Time mark

NEO-6T can be used for precise time measurements with sub-microsecond resolution using the external interrupt (EXTINT0). Rising and falling edges of these signals are time-stamped to the GPS or UTC time and counted. The Time Mark functionality can be enabled with the UBX-CFG-TM2 message

For details, please refer to the u-blox 6 Receiver Description including Protocol Specification [2].

1.8 Raw data

Raw data output is supported at an update rate of 5 Hz on the NEO-6T and NEO-6P. The UBX-RXM-RAW message includes carrier phase with half-cycle ambiguity resolved, code phase and Doppler measurements, which can be used in external applications that offer precision positioning, real-time kinematics (RTK) and attitude sensing.

1.9 Automotive Dead Reckoning

Automotive Dead Reckoning (ADR) is u-blox' industry proven off-the-shelf Dead Reckoning solution for tier-one automotive customers. u-blox' ADR solution combines GPS and sensor digital data using a tightly coupled Kalman filter. This improves position accuracy during periods of no or degraded GPS signal.

The NEO-6V provides ADR functionality over its software sensor interface. A variety of sensors (such as wheel ticks and gyroscope) are supported, with the sensor data received via UBX messages from the application processor. This allows for easy integration and a simple hardware interface, lowering costs. By using digital sensor data available on the vehicle bus, hardware costs are minimized since no extra sensors are required for Dead Reckoning functionality. ADR is designed for simple integration and easy configuration of different sensor options (e.g. with or without gyroscope) and vehicle variants, and is completely self-calibrating.

For more details contact the u-blox support representative nearest you to receive dedicated u-blox 6 Receiver Description Including Protocol Specification [3].

1.10 Precise Point Positioning

u-blox' industry proven PPP algorithm provides extremely high levels of position accuracy in static and slow moving applications, and makes the NEO-6P an ideal solution for a variety of high precision applications such as surveying, mapping, marine, agriculture or leisure activities.

Ionospheric corrections such as those received from local SBAS[12] geostationary satellites (WAAS, EGNOS, MSAS) or from GPS enable the highest positioning accuracy with the PPP algorithm. The maximum improvement of positioning accuracy is reached with PPP+SBAS and can only be expected in an environment with unobstructed sky view during a period in the order of minutes.

1.11 Oscillators

NEO-6 GPS modules are available in Crystal and TCXO versions. The TCXO allows accelerated weak signal acquisition, enabling faster start and reacquisition times.

1.12 Protocols and interfaces

Protocol	Type
NMEA	Input/output, ASCII, 0183, 2.3 (compatible to 3.0)
UBX	Input/output, binary, u-blox proprietary
RTCM	Input, 2.3

Table 4: Available protocols

All listed protocols are available on UART, USB, and DDC. For specification of the various protocols see the u-blox 6 Receiver Description including Protocol Specification [2].

1.12.1 UART

NEO-6 modules include one configurable UART interface for serial communication (for information about configuration see section 1.15).

1.12.2 USB

NEO-6 modules provide a USB version 2.0 FS (Full Speed, 12Mbit/s) interface as an alternative to the UART. The pull-up resistor on USB_DP is integrated to signal a full-speed device to the host. The VDDUSB pin supplies the USB interface. u-blox provides a Microsoft® certified USB driver for Windows XP, Windows Vista and Windows 7 operating systems.

1.12.3 Serial Peripheral Interface (SPI)

The SPI interface allows for the connection of external devices with a serial interface, e.g. serial flash to save configuration and AssistNow Offline A-GPS data or to interface to a host CPU. The interface can be operated in master or slave mode. In master mode, one chip select signal is available to select external slaves. In slave mode a single chip select signal enables communication with the host.

☞ The maximum bandwidth is 100kbit/s.

[12] Satellite Based Augmentation System

1.12.4 Display Data Channel (DDC)

The I²C compatible DDC interface can be used either to access external devices with a serial interface EEPROM or to interface with a host CPU. It is capable of master and slave operation. The DDC interface is I²C Standard Mode compliant. For timing parameters consult the I²C standard.

The DDC Interface supports serial communication with u-blox wireless modules. See the specification of the applicable wireless module to confirm compatibility.

The maximum bandwidth is 100kbit/s.

1.12.4.1 External serial EEPROM

NEO-6 modules allow an optional external serial EEPROM to be connected to the DDC interface. This can be used to store Configurations permanently.

For more information see the LEA-6/NEO-6/MAX-6 Hardware Integration Manual [1].

Use caution when implementing since forward compatibility is not guaranteed.

1.13 Antenna

NEO-6 modules are designed for use with passive and active[13] antennas.

Parameter	Specification	
Antenna Type		Passive and active antenna
Active Antenna Recommendations	Minimum gain	15 dB (to compensate signal loss in RF cable)
	Maximum gain	50 dB
	Maximum noise figure	1.5 dB

Table 5: Antenna Specifications for all NEO-6 modules

1.14 Power Management

u-blox receivers support different power modes. These modes represent strategies of how to control the acquisition and tracking engines in order to achieve either the best possible performance or good performance with reduced power consumption.

For more information about power management strategies, see the u-blox 6 Receiver Description including Protocol Specification [2].

1.14.1 Maximum Performance Mode

During a Cold start, a receiver in Maximum Performance Mode continuously deploys the acquisition engine to search for all satellites. Once the receiver has a position fix (or if pre-positioning information is available), the acquisition engine continues to be used to search for all visible satellites that are not being tracked.

1.14.2 Eco Mode

During a Cold start, a receiver in Eco Mode works exactly as in Maximum Performance Mode. Once a position can be calculated and a sufficient number of satellites are being tracked, the acquisition engine is powered off resulting in significant power savings. The tracking engine continuously tracks acquired satellites and acquires other available or emerging satellites.

Note that even if the acquisition engine is powered off, satellites continue to be acquired.

[13] For information on using active antennas with NEO-6 modules, see the LEA-6/NEO-6 Hardware Integration Manual [1].

1.14.3 Power Save Mode

Power Save Mode (PSM) allows a reduction in system power consumption by selectively switching parts of the receiver on and off.

Power Save mode is not available with NEO-6P, NEO-6T and NEO-6V.

1.15 Configuration

1.15.1 Boot-time configuration

NEO-6 modules provide configuration pins for boot-time configuration. These become effective immediately after start-up. Once the module has started, the configuration settings can be modified with UBX configuration messages. The modified settings remain effective until power-down or reset. If these settings have been stored in battery-backup RAM, then the modified configuration will be retained, as long as the backup battery supply is not interrupted.

NEO-6 modules include both **CFG_COM0** and **CFG_COM1** pins and can be configured as seen in Table 6. Default settings in bold.

CFG_COM1	CFG_COM0	Protocol	Messages	UARTBaud rate	USB power
1	**1**	**NMEA**	**GSV, RMC, GSA, GGA, GLL, VTG, TXT**	**9600**	**BUS Powered**
1	0	NMEA	GSV, RMC, GSA, GGA, GLL, VTG, TXT	38400	Self Powered
0	1	NMEA	GSV[14], RMC, GSA, GGA, VTG, TXT	4800	BUS Powered
0	0	UBX	NAV-SOL, NAV-STATUS, NAV-SVINFO, NAV-CLOCK, INF, MON-EXCEPT, AID-ALPSERV	57600	BUS Powered

Table 6: Supported COM settings

NEO-6 modules include a **CFG_GPS0** pin, which enables the boot-time configuration of the power mode. These settings are described in Table 7. Default settings in bold.

CFG_GPS0	Power Mode
0	Eco Mode
1	**Maximum Performance Mode**

Table 7: Supported CFG_GPS0 settings

Static activation of the **CFG_COM** and **CFG_GPS** pins is not compatible with use of the SPI interface.

1.16 Design-in

In order to obtain the necessary information to conduct a proper design-in, u-blox strongly recommends consulting the LEA-6/NEO-6/MAX-6 Hardware Integration Manual [1].

[14] Every 5th fix.

2 Pin Definition

2.1 Pin assignment

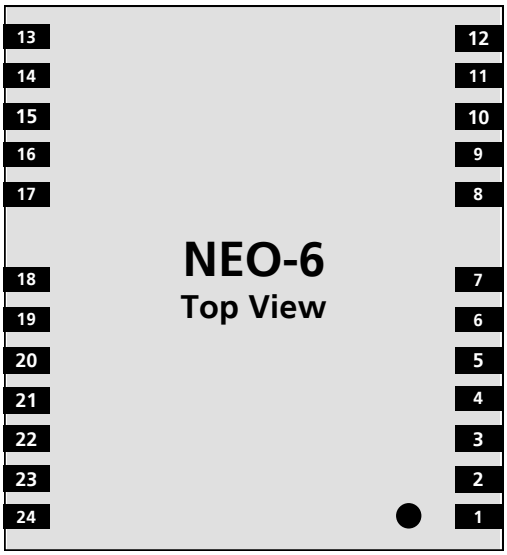


Figure 2 Pin Assignment

No	Module	Name	I/O	Description
1	All	Reserved	I	Reserved
2	All	SS_N	I	SPI Slave Select
3	All	TIMEPULSE	O	Timepulse (1PPS)
4	All	EXTINT0	I	External Interrupt Pin
5	All	USB_DM	I/O	USB Data
6	All	USB_DP	I/O	USB Data
7	All	VDDUSB	I	USB Supply
8	All	Reserved		See Hardware Integration Manual Pin 8 and 9 must be connected together.
9	All	VCC_RF	O	Output Voltage RF section Pin 8 and 9 must be connected together.
10	All	GND	I	Ground
11	All	RF_IN	I	GPS signal input
12	All	GND	I	Ground
13	All	GND	I	Ground
14	All	MOSI/CFG_COM0	O/I	SPI MOSI / Configuration Pin. Leave open if not used.
15	All	MISO/CFG_COM1	I	SPI MISO / Configuration Pin. Leave open if not used.
16	All	CFG_GPS0/SCK	I	Power Mode Configuration Pin / SPI Clock. Leave open if not used.
17	All	Reserved	I	Reserved
18	All	SDA2	I/O	DDC Data
19	All	SCL2	I/O	DDC Clock
20	All	TxD1	O	Serial Port 1
21	All	RxD1	I	Serial Port 1

No	Module	Name	I/O	Description
22	All	V_BCKP	I	Backup voltage supply
23	All	VCC	I	Supply voltage
24	All	GND	I	Ground

Table 8: Pinout

Pins designated Reserved should not be used. For more information about Pinouts see the LEA-6/NEO-6/MAX-6 Hardware Integration Manual [1].

3 Electrical specifications

3.1 Absolute maximum ratings

Parameter	Symbol	Module	Min	Max	Units	Condition
Power supply voltage	VCC	NEO-6G	-0.5	2.0	V	
		NEO-6Q, 6M, 6P, 6V, 6T	-0.5	3.6	V	
Backup battery voltage	V_BCKP	All	-0.5	3.6	V	
USB supply voltage	VDDUSB	All	-0.5	3.6	V	
Input pin voltage	Vin	All	-0.5	3.6	V	
	Vin_usb	All	-0.5	VDDUSB	V	
DC current trough any digital I/O pin (except supplies)	Ipin			10	mA	
VCC_RF output current	ICC_RF	All		100	mA	
Input power at RF_IN	Prfin	NEO-6Q, 6M, 6G, 6V, 6T		15	dBm	source impedance = 50Ω, continuous wave
		NEO-6P		-5	dBm	
Storage temperature	Tstg	All	-40	85	°C	

Table 9: Absolute maximum ratings

GPS receivers are Electrostatic Sensitive Devices (ESD) and require special precautions when handling. For more information see chapter 6.4.

Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification, given in table above, must be limited to values within the specified boundaries by using appropriate protection diodes. For more information see the *LEA-6/NEO-6/MAX-6 Hardware Integration Manual* [1].

3.2 Operating conditions

☞ All specifications are at an ambient temperature of 25°C.

Parameter	Symbol	Module	Min	Typ	Max	Units	Condition
Power supply voltage	VCC	NEO-6G	1.75	1.8	1.95	V	
		NEO-6Q/M NEO-6P/V/T	2.7	3.0	3.6	V	
Supply voltage USB	VDDUSB	All	3.0	3.3	3.6	V	
Backup battery voltage	V_BCKP	All	1.4		3.6	V	
Backup battery current	I_BCKP	All		22		µA	V_BCKP = 1.8 V, VCC = 0V
Input pin voltage range	Vin	All	0		VCC	V	
Digital IO Pin Low level input voltage	Vil	All	0		0.2*VCC	V	
Digital IO Pin High level input voltage	Vih	All	0.7*VCC		VCC	V	
Digital IO Pin Low level output voltage	Vol	All			0.4	V	Iol=4mA
Digital IO Pin High level output voltage	Voh	All	VCC -0.4			V	Ioh=4mA
USB_DM, USB_DP	VinU	All	Compatible with USB with 22 Ohms series resistance				
VCC_RF voltage	VCC_RF	All		VCC-0.1		V	
VCC_RF output current	ICC_RF	All			50	mA	
Antenna gain	Gant	All			50	dB	
Receiver Chain Noise Figure	NFtot	All		3.0		dB	
Operating temperature	Topr	All	-40		85	°C	

Table 10: Operating conditions

☞ Operation beyond the specified operating conditions can affect device reliability.

3.3 Indicative power requirements

Table 11 lists examples of the total system supply current for a possible application.

Parameter	Symbol	Module	Min	Typ	Max	Units	Condition
Max. supply current [15]	Iccp	All			67	mA	VCC = 3.6 V[16] / 1.95 V[17]
Average supply current[18]	Icc Acquisition	All		47[19]		mA	VCC = 3.0 V[16] / 1.8 V[17]
	Icc Tracking (Max Performance mode)	NEO-6G/Q/T		40[20]		mA	
		NEO-6M/P/V		39[20]		mA	
	Icc Tracking (Eco mode)	NEO-6G/Q/T		38[20]		mA	
		NEO-6M/P/V		37[20]		mA	
	Icc Tracking (Power Save mode / 1 Hz)	NEO-6G/Q		12[20]		mA	
		NEO-6M		11[20]		mA	

Table 11: Indicative power requirements

☞ Values in Table 11 are provided for customer information only as an example of typical power requirements. Values are characterized on samples, actual power requirements can vary depending on FW version used, external circuitry, number of SVs tracked, signal strength, type of start as well as time, duration and conditions of test.

[15] Use this figure to dimension maximum current capability of power supply. Measurement of this parameter with 1 Hz bandwidth.
[16] NEO-6Q, NEO-6M, NEO-6P, NEO-6V, NEO-6T
[17] NEO-6G
[18] Use this figure to determine required battery capacity.
[19] >8 SVs in view, CNo >40 dBHz, current average of 30 sec after cold start.
[20] With strong signals, all orbits available. For Cold Starts typical 12 min after first fix. For Hot Starts typical 15 s after first fix.

3.4 SPI timing diagrams

In order to avoid a faulty usage of the SPI, the user needs to comply with certain timing conditions. The following signals need to be considered for timing constraints:

Symbol	Description
SS_N	Slave Select signal
SCK	Slave Clock signal

Table 12: Symbol description

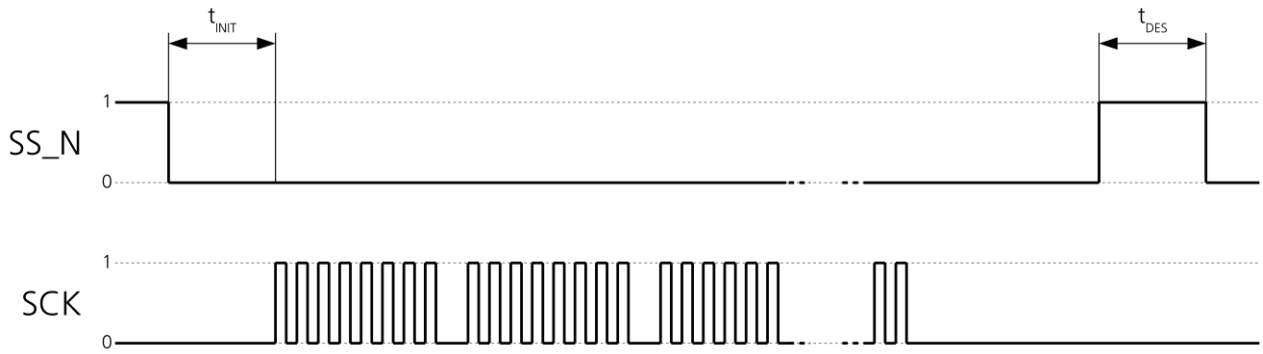


Figure 3: SPI timing diagram

3.4.1 Timing recommendations

Parameter	Description	Recommendation
t_{INIT}	Initialization Time	500 µs
t_{DES}	Deselect Time	1 ms
Bitrate		100 kbit/s

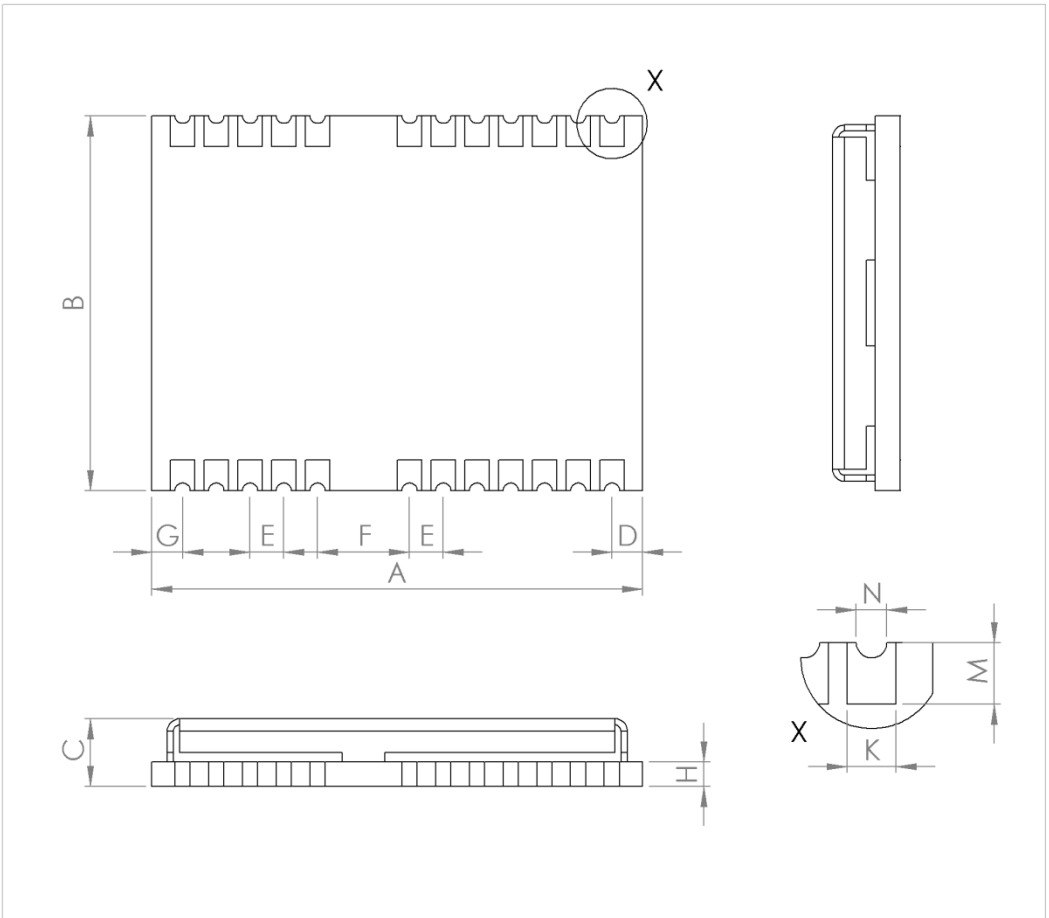
Table 13: SPI timing recommendations

☞ The values in the above table result from the requirement of an error-free transmission. By allowing just a few errors, the byte rate could be increased considerably. These timings – and therefore the byte rate – could also be improved by disabling other interfaces, e.g. the UART.

☞ The maximum bandwidth is 100 kbit/s[21].

[21] This is a theoretical maximum, the protocol overhead is not considered.

4 Mechanical specifications



Symbol	Min. (mm)	Typ. (mm)	Max. (mm)
A	15.9	16.0	16.6
B	12.1	12.2	12.3
C	2.2	2.4	2.6
D	0.9	1.0	1.3
E	1.0	1.1	1.2
F	2.9	3.0	3.1
G	0.9	1.0	1.3
H		0.82	
K	0.7	0.8	0.9
M	0.8	0.9	1.0
N	0.4	0.5	0.6
Weight		1.6g	

Figure 4: Dimensions

For information regarding the Paste Mask and Footprint see the LEA-6/NEO-6/MAX-6 Hardware Integration Manual [1].

5 Qualification and certification

5.1 Reliability tests

☞ All NEO-6 modules are based on AEC-Q100 qualified GPS chips.

Tests for product family qualifications according to ISO 16750 "Road vehicles - Environmental conditions and testing for electrical and electronic equipment", and appropriate standards.

5.2 Approvals

Products marked with this lead-free symbol on the product label comply with the "Directive 2002/95/EC of the European Parliament and the Council on the Restriction of Use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

All u-blox 6 GPS modules are RoHS compliant.

6 Product handling & soldering

6.1 Packaging

NEO-6 modules are delivered as hermetically sealed, reeled tapes in order to enable efficient production, production lot set-up and tear-down. For more information about packaging, see the u-blox Package Information Guide [4].

Figure 5: Reeled u-blox 6 modules

6.1.1 Reels

NEO-6 GPS modules are deliverable in quantities of 250pcs on a reel. NEO-6 modules are delivered using reel Type B as described in the u-blox Package Information Guide [4].

Parameter	Specification
Reel Type	B
Delivery Quantity	250

Table 14: Reel information for NEO-6 modules

6.1.1 Tapes

Figure 6 shows the position and orientation of NEO-6 modules as they are delivered on tape. The dimensions of the tapes are specified in Figure 7.

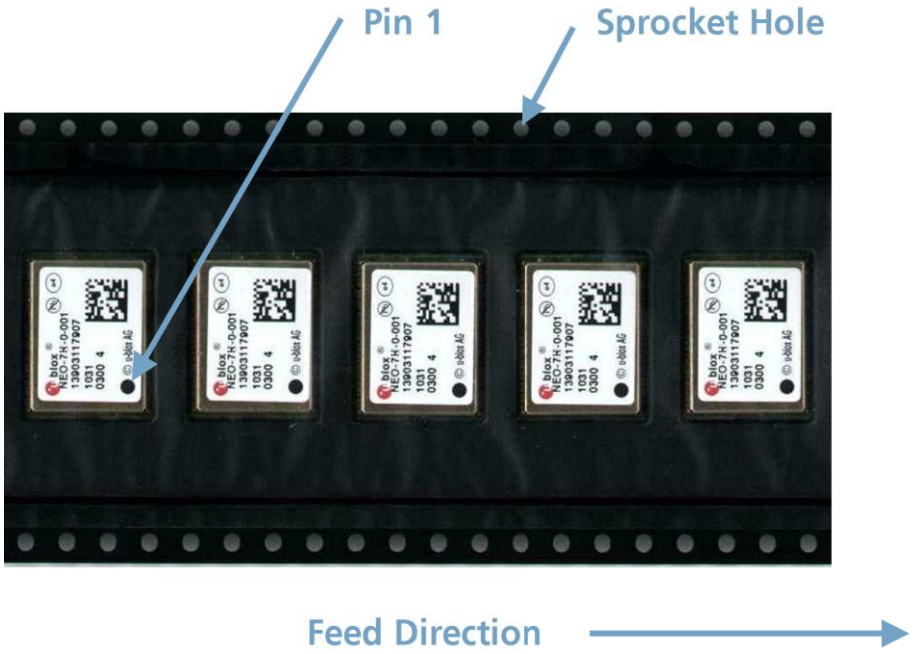


Figure 6: Orientation for NEO-6 modules on tape

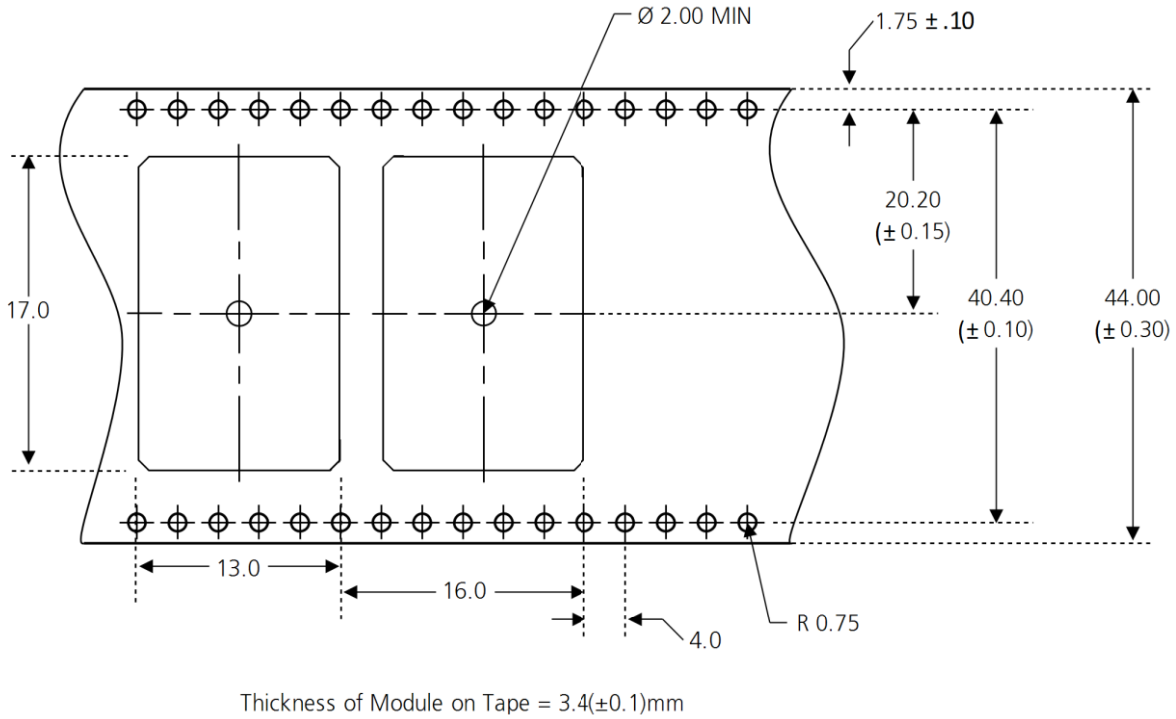


Figure 7: NEO tape dimensions (mm)

6.2 Moisture Sensitivity Levels

NEO-6 modules are Moisture Sensitive Devices (MSD) in accordance to the IPC/JEDEC specification.

NEO-6 modules are rated at MSL level 4. For more information regarding moisture sensitivity levels, labeling, storage and drying see the u-blox Package Information Guide [4].

For MSL standard see IPC/JEDEC J-STD-020, which can be downloaded from www.jedec.org.

6.3 Reflow soldering

Reflow profiles are to be selected according to u-blox recommendations (see LEA-6/NEO-6/MAX-6 Hardware Integration Manual [1]).

6.4 ESD handling precautions

NEO-6 modules contain highly sensitive electronic circuitry and are Electrostatic Sensitive Devices (ESD). Observe precautions for handling! Failure to observe these precautions can result in severe damage to the GPS receiver!

GPS receivers are Electrostatic Sensitive Devices (ESD) and require special precautions when handling. Particular care must be exercised when handling patch antennas, due to the risk of electrostatic charges. In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the receiver:

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB must always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect ground of the device
- When handling the RF pin, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna ~10pF, coax cable ~50-80pF/m, soldering iron, …)
- To prevent electrostatic discharge through the RF input, do not touch any exposed antenna area. If there is any risk that such exposed antenna area is touched in non ESD protected work area, implement proper ESD protection measures in the design.
- When soldering RF connectors and patch antennas to the receiver's RF pin, make sure to use an ESD safe soldering iron (tip).

7 Default settings

Interface	Settings
Serial Port 1 Output	9600 Baud, 8 bits, no parity bit, 1 stop bit Configured to transmit both NMEA and UBX protocols, but only following NMEA and no UBX messages have been activated at start-up: **GGA, GLL, GSA, GSV, RMC, VTG, TXT** (In addition to the 6 standard NMEA messages the NEO-6T includes **ZDA**).
USB Output	Configured to transmit both NMEA and UBX protocols, but only following NMEA and no UBX messages have been activated at start-up: **GGA, GLL, GSA, GSV, RMC, VTG, TXT** (In addition to the 6 standard NMEA messages the NEO-6T includes **ZDA**). USB Power Mode: Bus-Powered
Serial Port 1 Input	9600 Baud, 8 bits, no parity bit, 1 stop bit Automatically accepts following protocols without need of explicit configuration: **UBX, NMEA** The GPS receiver supports interleaved UBX and NMEA messages.
USB Input	Automatically accepts following protocols without need of explicit configuration: **UBX, NMEA** The GPS receiver supports interleaved UBX and NMEA messages. USB Power Mode: Bus-Powered
TIMEPULSE (1Hz Nav)	1 pulse per second, synchronized at rising edge, pulse length 100ms
Power Mode	Maximum Performance mode
AssistNow Autonomous	Disabled.

Table 15: Default settings

Refer to the u-blox 6 Receiver Description including Protocol Specification [2] for information about further settings.

8 Labeling and ordering information

8.1 Product labeling

The labeling of u-blox 6 GPS modules includes important product information. The location of the product type number is shown in Figure 8.

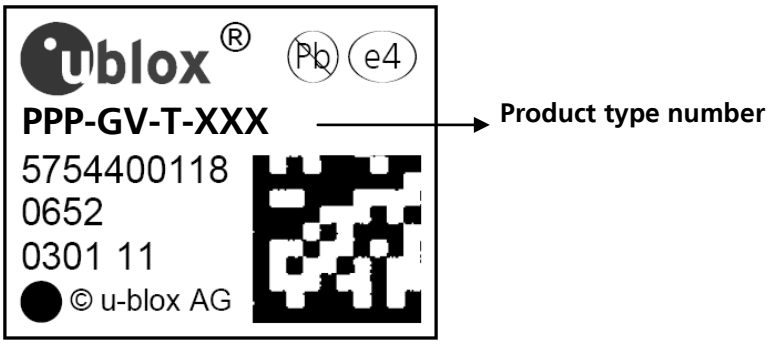


Figure 8: Location of product type number on u-blox 6 module label

8.2 Explanation of codes

3 different product code formats are used. The **Product Name** is used in documentation such as this data sheet and identifies all u-blox 6 products, independent of packaging and quality grade. The **Ordering Code** includes options and quality, while the **Type Number** includes the hardware and firmware versions. Table 16 below details these 3 different formats:

Format	Structure
Product Name	PPP-GV
Ordering Code	PPP-GV-T
Type Number	PPP-GV-T-XXX

Table 16: Product Code Formats

The parts of the product code are explained in Table 17.

Code	Meaning	Example
PPP	Product Family	NEO
G	Product Generation	6 = u-blox6
V	Variant	T = Timing, R = DR, etc.
T	Option / Quality Grade	Describes standardized functional element or quality grade such as Flash size, automotive grade etc.
XXX	Product Detail	Describes product details or options such as hard- and software revision, cable length, etc.

Table 17: part identification code

8.3 Ordering information

Ordering No.	Product
NEO-6G-0	u-blox 6 GPS Module, 1.8V, TCXO, 12x16mm, 250 pcs/reel
NEO-6M-0	u-blox 6 GPS Module, 12x16mm, 250 pcs/reel
NEO-6Q-0	u-blox 6 GPS Module, TCXO, 12x16mm, 250 pcs/reel
NEO-6P-0	u-blox 6 GPS Module, PPP, 12x16mm, 250 pcs/reel
NEO-6V-0	u-blox 6 GPS Module, Dead Reckoning SW sensor, 12x16mm, 250 pcs/reel
NEO-6T-0	u-blox 6 GPS Module, Precision Timing, TCXO, 12x16mm, 250 pcs/reel

Table 18: Product Ordering Codes

☞ Product changes affecting form, fit or function are documented by u-blox. For a list of Product Change Notifications (PCNs) see our website at: http://www.u-blox.com/en/notifications.html

Related documents

[1] LEA-6/NEO-6/MAX-6 Hardware Integration Manual, Docu. GPS.G6-HW-09007

[2] u-blox 6 Receiver Description Including Protocol Specification (Public version), Docu. No. GPS.G6-SW-10018

[3] u-blox 6 Receiver Description Including Protocol Specification (Confidential version), Docu. No. GPS.G6-SW-10019

[4] u-blox Package Information Guide, Docu. No GPS-X-11004

☞ For regular updates to u-blox documentation and to receive product change notifications please register on our homepage.

Revision history

Revision	Date	Name	Status / Comments
	31/08/2009	tgri	Initial Version
1	21/09/2009	tgri	update of section 1.3 GPS performance, section 1.4 block diagram, section 3.2 peak supply current
A	25/02/2010	tgri	Change of status to Advance Information. Addition of NEO-6G. Update of section 1.8.2, removed reference to Vddio – added USB driver certification. Update of section 3.2 table 11: average supply current, Added section 3.3-3.4: SPI & DDC timing, section 5.1: addition of table 12.
B	24/06/2010	dhur	Change of status to Preliminary. Update of section 1.2, 1.8.4, 1.10.4, 3.1, 3.2 and chapter 2 and 4. General clean-up and consistency check.
B1	11/08/2010	dhur	Replaced graphic in figure 2.
C	18/07/2011	dhur	Added chapter 1.6, update to FW7.03.
D	19/10/2011	dhur	Added NEO-6P and NEO-6V. Added chapter 1.7 and 1.8. Revised Chapter 6.
E	05/12/2011	dhur	Added NEO-6T. Added chapter 1.7 and 1.8. Added Accuracy for Timepulse signal in Table 2. Corrected Maximum Input power at RF_IN for NEO-6P in Table 9.

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SN74LV1T34 Single Power Supply Single Buffer GATE CMOS Logic Level Shifter

1 Features

- Single-Supply Voltage Translator at 5.0/3.3/2.5/1.8V V_{CC}
- Operating Range of 1.8V to 5.5V
- Up Translation
  - 1.2V(1) to 1.8V at 1.8V V_{CC}
  - 1.5V(1) to 2.5V at 2.5V V_{CC}
  - 1.8V(1) to 3.3V at 3.3V V_{CC}
  - 3.3V to 5.0V at 5.0V V_{CC}
- Down Translation
  - 3.3V to 1.8V at 1.8V V_{CC}
  - 3.3V to 2.5V at 2.5V V_{CC}
  - 5.0V to 3.3V at 3.3V V_{CC}
- Logic Output is Referenced to V_{CC}
- Output Drive
  - 8.0mA Output Drive at 5.0V
  - 7.0mA Output Drive at 3.3V
  - 3.0mA Output Drive at 1.8V
- Characterized up to 50MHz at 3.3V V_{CC}
- 5.0V Tolerance on Input Pins
- –40°C to 125°C Operating Temperature Range
- Latch-Up Performance Exceeds 250mA Per JESD 17
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Supports Standard Logic Pinouts
- CMOS Output B Compatible with AUP1G and LVC1G Families

(1) Refer to the V_{IH}/V_{IL} and output drive for lower V_{CC} condition

2 Applications

- Industrial controllers
- Telecom
- Portable applications
- Servers
- PC and notebooks
- Automotive

3 Description

SN74LV1T34 is a low voltage CMOS gate logic that operates at a wider voltage range for industrial, portable, telecom, and automotive applications. The output level is referenced to the supply voltage and is able to support 1.8V/2.5V/3.3V/5V CMOS levels.

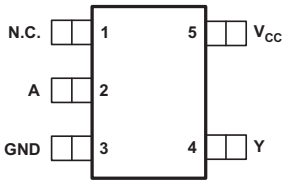
The input is designed with a lower threshold circuit to match 1.8V input logic at V_{CC} = 3.3V and can be used in 1.8V to 3.3V level up translation. In addition, the 5V tolerant input pins enable down translation (e.g. 3.3V to 2.5V output at V_{CC} = 2.5V). The wide V_{CC} range of 1.8V to 5.5V allows generation of desired output levels to connect to controllers or processors.

The SN74LV1T34 is designed with current-drive capability of 8 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SN74LV1T34DBVR	SOT-23 (5)	2,90mm x 1,60mm
SN74LV1T34DCKR	SC70 (5)	2,00mm x 1,25mm

DCK or DBV PACKAGE
(TOP VIEW)



DPW PACKAGE
(TOP VIEW)

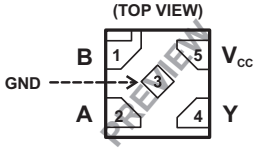


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

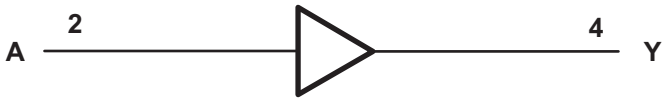
Changes from Original (December 2013) to Revision A	Page
• Updated document formatting.	1

Function Table

INPUT (Lower Level Input)	OUTPUT (V_{CC} CMOS)
A	Y
H	H
L	L

SUPPLY V_{CC} = 3.3V		
INPUT (Lower Level Input)		OUTPUT (V_{CC} CMOS)
A	B	Y
VIH(min) =1.35 V VIL(max) =0.8 V		VOH(min) = 2.9 V VOL(max)= 0.2 V

4.1 Logic Diagram



Switching Characteristics at 50 MHz

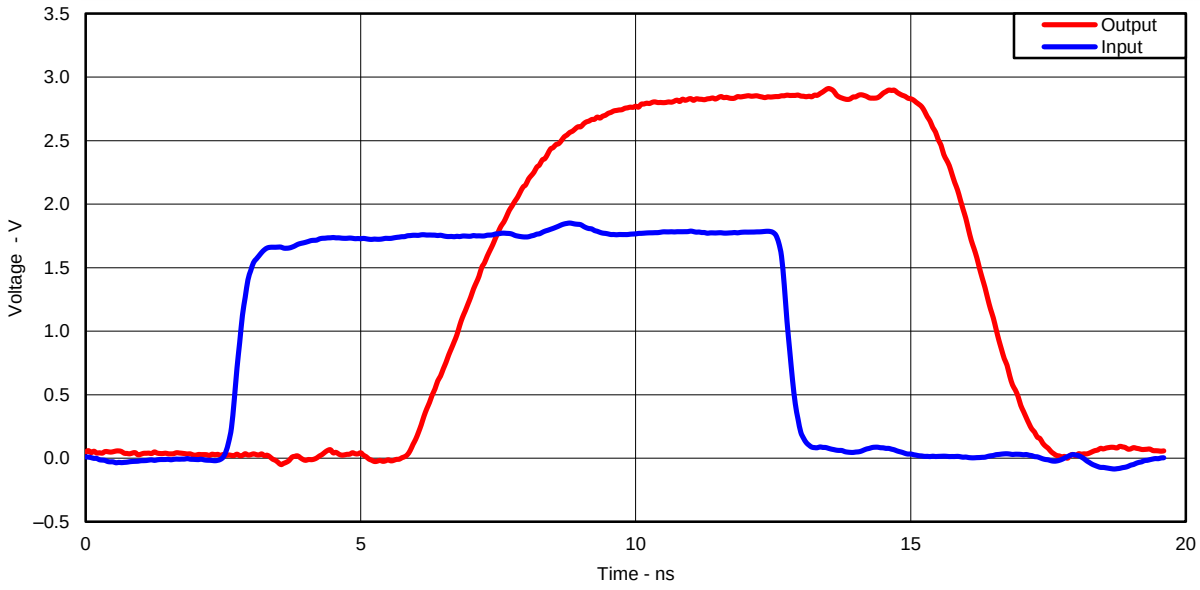


Figure 1. Excellent Signal Integrity (1.8V to 3.3V at 3.3V V_{CC})

Logic Diagram (continued)

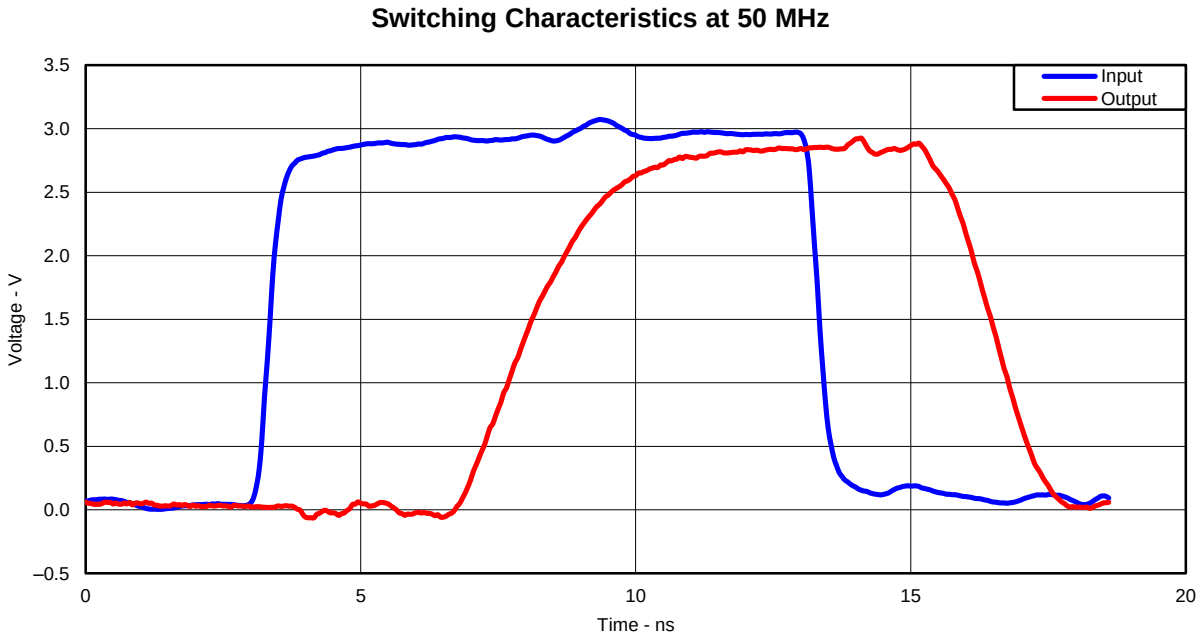


Figure 2. Excellent Signal Integrity (3.3V to 3.3V at 3.3V V_{CC})

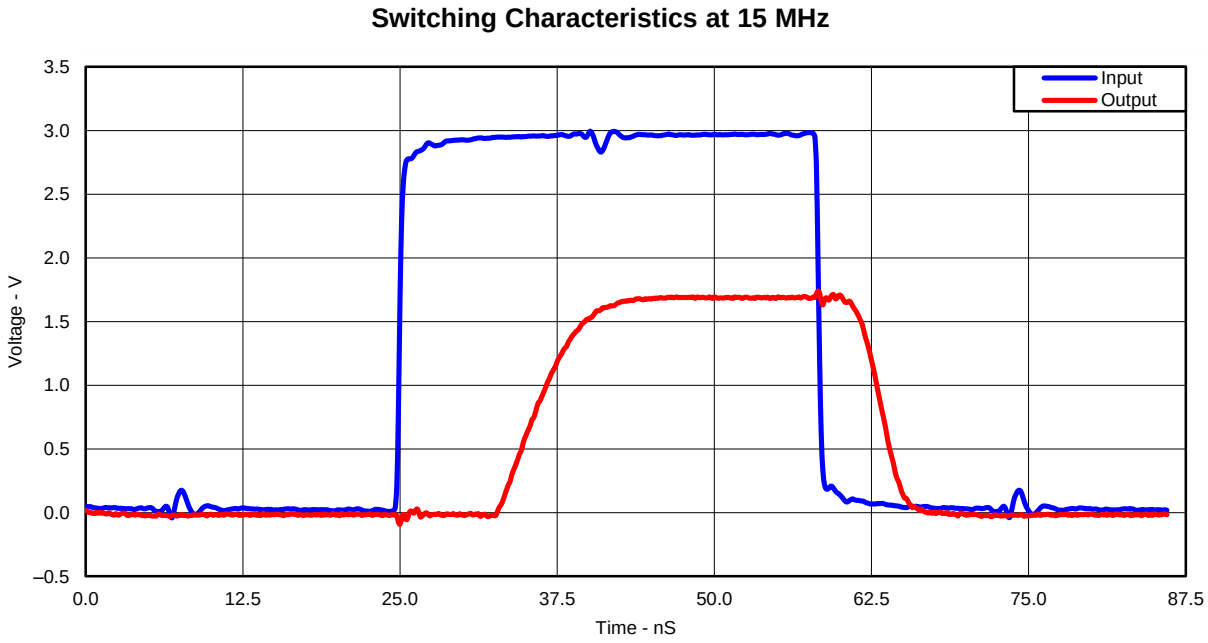


Figure 3. Excellent Signal Integrity (3.3V to 1.8V at 1.8V V_{CC})

4.2 Typical Design Examples

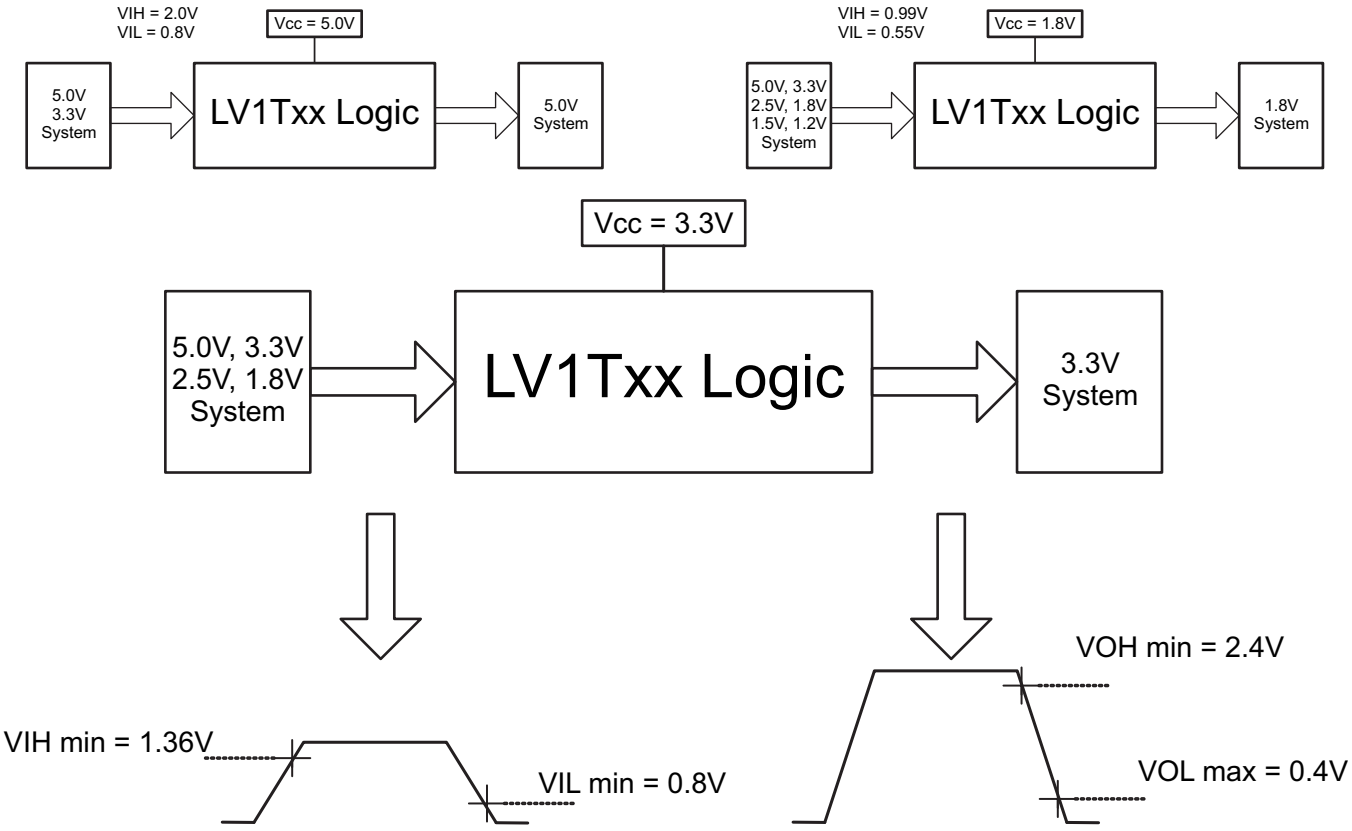


Figure 4. Switching Thresholds for 1.8-V to 3.3-V Translation

4.3 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7.0	V
V_I	Input voltage range(2)		–0.5	7.0	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	4.6	V
	Voltage range applied to any output in the high or low state(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current			±25	mA
	Continuous current through VCC or GND			±50	mA
θ_{JA}	Package thermal impedance(3)	DBV package		206	°C/W
		DCK package		252	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

4.4 Recommended Operating Conditions(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.6	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	Vcc	V
I_{OH}	High-level output current	V_{CC} = 1.8 V		–3.0	mA
		V_{CC} = 2.5 V		–5.0	
		V_{CC} = 3.3 V		–7.0	
		V_{CC} = 5.0 V		–8.0	
I_{OL}	Low-level output current	V_{CC} = 1.8 V		3.0	mA
		V_{CC} = 2.5 V		5.0	
		V_{CC} = 3.3 V		7.0	
		V_{CC} = 5.0 V		8.0	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.8 V		20	ns/V
		V_{CC} = 3.3 V or 2.5 V		20	
		V_{CC} = 5.0 V		20	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{IH}	High-level input voltage		V_{CC} = 1.65 V to 1.8 V	0.95			1.0		V
			V_{CC} = 2.0 V	0.99			1.03		
			V_{CC} = 2.25 V to 2.5 V	1.145			1.18		
			V_{CC} = 2.75 V	1.22			1.25		
			$_{VCC}$ = 3.0 V to 3.3 V	1.37			1.39		
			V_{CC} = 3.6 V	1.47			1.48		
			V_{CC} = 4.5 V to 5.0 V	2.02			2.03		
			V_{CC} = 5.5 V	2.1			2.11		
V_{IL}	Low-level input voltage		V_{CC} = 1.65 V to 2.0 V			0.57		0.55	V
			V_{CC} = 2.25 V to 2.75 V			0.75		0.71	
			V_{CC} = 3.0 V to 3.6 V			0.8		0.65	
			V_{CC} = 4.5 V to 5.5 V			0.8		0.8	
V_{OH}		I_{OH} = –20 µA	1.65 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1		V
		I_{OH} = –2.0 mA	1.65 V	1.28			1.21		
			1.8 V	1.5			1.45		
		I_{OH} = –3.0 mA	2.3 V	2.0			1.93		
		I_{OH} = –3.0 mA	2.5 V	2.25			2.15		
		I_{OH} = –3.0 mA	3.0 V	2.78			2.7		V
		I_{OH} = –5.5 mA		2.6			2.49		
		I_{OH} = –5.5 mA	3.3 V	2.9			2.8		
		I_{OH} = –4.0 mA	4.5 V	4.2			4.1		
		I_{OH} = –8.0 mA		4.1			3.95		
		I_{OH} = –8.0 mA	5.0 V	4.6			4.5		
V_{OL}		I_{OL} = 20 µA	1.65 V to 5.5 V			0.1		0.1	V
		I_{OL} = 2.0 mA	1.65 V			0.2		0.25	
		I_{OH} = 3.0 mA	2.3 V			0.15		0.2	
		I_{OL} = 3.0 mA	3.0 V			0.11		0.15	
		I_{OL} = 5.5 mA				0.21		0.252	
		I_{OL} = 4.0 mA	4.5 V			0.15		0.2	
		I_{OL} = 8.0 mA				0.3		0.35	
I_I	A input	V_I = 0 V or V_{CC}	0 V, 1.8 V, 2.5 V, 3.3 V, 5.5 V			0.1		±1.0	µA
I_{CC}		V_I = 0 V or V_{CC}; I_O = 0; Open on loading	5.0 V			1.0		10.0	µA
			3.3 V			1.0		10.0	
			2.5 V			1.0		10.0	
			1.8 V			1.0		10.0	
ΔI_{CC}		One input at 0.3 V or 3.4 V Other inputs at 0 or V_{CC}, I_O = 0	5.5 V			1.35		1.5	mA
		One input at 0.3 V or 1.1 V Other inputs at 0 or V_{CC}, I_O = 0	1.8 V			10.0		10.0	µA
C_i		V_I = V_{CC} or GND	3.3 V		2.0	10.0	2.0	10.0	pF
C_o		V_O = V_{CC} or GND	3.3 V		2.5		2.5		pF

4.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

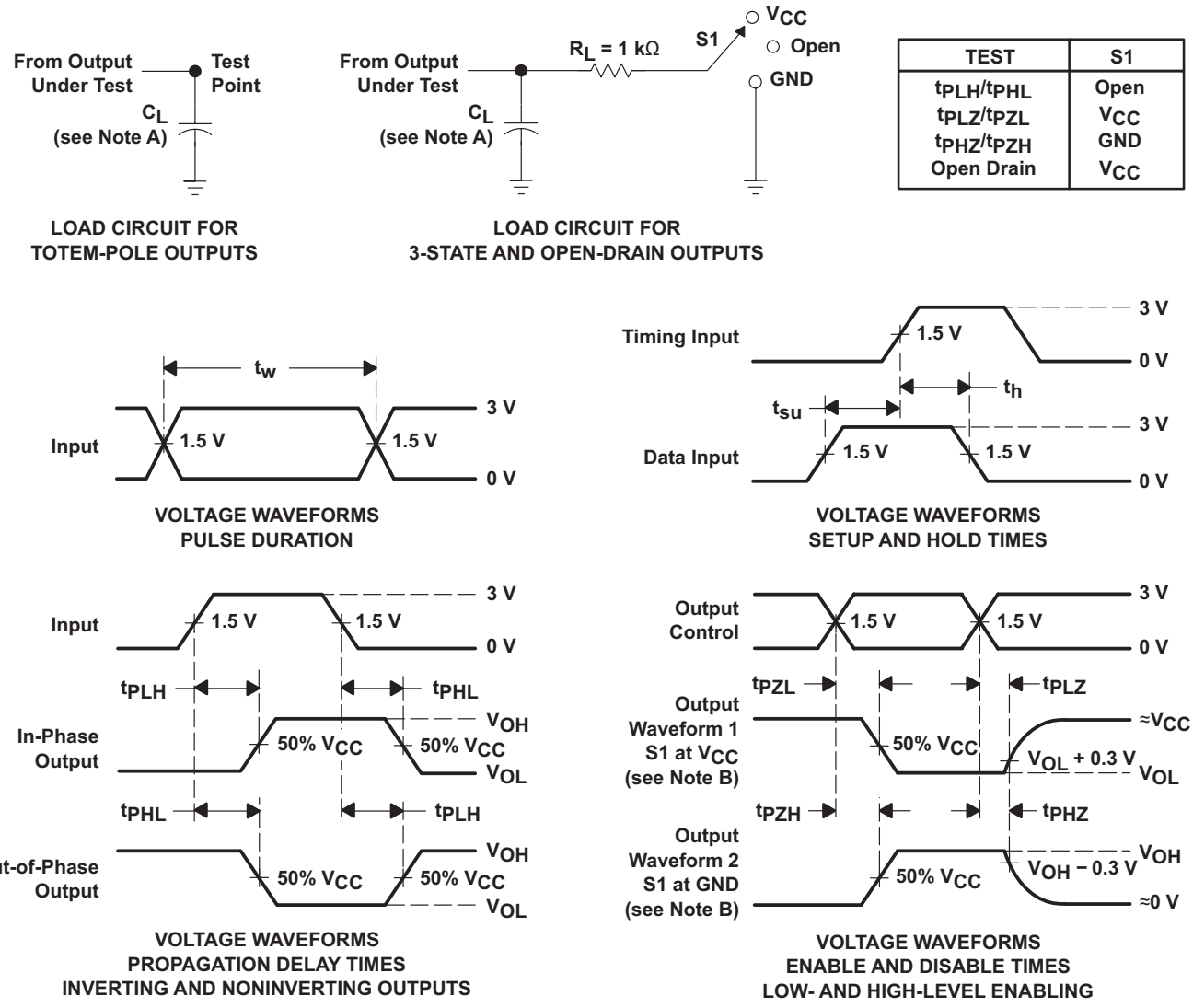
PARAMETER	FROM (INPUT)	TO (OUTPUT)	FREQUENCY (TYP)	V_{CC}	C_L	T_A = 25°C			T_A = –65°C to 125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Any In	Y	DC to 50MHz	5.0 V	15 pF		2.7	5.5		3.4	6.5	ns
					30 pF		3.0	6.5		4.1	7.5	
				3.3 V	15 pF		4.0	7.0		5.0	8.0	ns
					30 pF		4.9	8.0		6.0	9.0	
			DC to 25MHz	2.5 V	15 pF		5.8	8.5		6.8	9.5	ns
					30 pF		6.5	9.5		7.5	10.5	
			DC to 15MHz	1.8 V	15 pF		10.5	13.0		11.8	14.0	ns
					30 pF		12.0	14.5		12.0	15.5	

4.7 Operating Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 1 MHz and 10 MHz	1.8 V ± 0.15 V	14	pF
			2.5 V ± 0.2 V	14	
			3.3 V ± 0.3 V	14	
			5.0 V ± 0.5 V	14	

5 Parameter Measurement Information



NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

5.1 More Product Selection

DEVICE	PACKAGE	DESCRIPTION
SN74LV1T00	DCK, DBV	2-Input Positive-NAND Gate
SN74LV1T02	DCK, DBV	2-Input Positive-NOR Gate
SN74LV1T04	DCK, DBV	Inverter Gate
SN74LV1T08	DCK, DBV	2-Input Positive-AND Gate
SN74LV1T34	DCK, DBV, DPW	Single Buffer Gate
SN74LV1T14	DCK, DBV	Single Schmitt-Trigger Inverter Gate
SN74LV1T32	DCK, DBV	2-Input Positive-OR Gate
SN74LV1T86	DCK, DBV	Single 2-Input Exclusive-Or Gate
SN74LV1T125	DCK, DBV	Single Buffer Gate with 3-state Output
SN74LV1T126	DCK, DBV	Single Buffer Gate with 3-state Output
SN74LV4T125	RGY, PW	Quadruple Bus Buffer Gate With 3-State Outputs

6 Device and Documentation Support

6.1 Trademarks

All trademarks are the property of their respective owners.

6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

7 Mechanical, Packaging, and Orderable Information

The following packaging information and addendum reflect the most current data available for the designated devices. This data is subject to change without notice and revision of this document.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV1T34DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(NEJ3 ~ NEJS)	Samples
SN74LV1T34DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(WJ3 ~ WJS)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

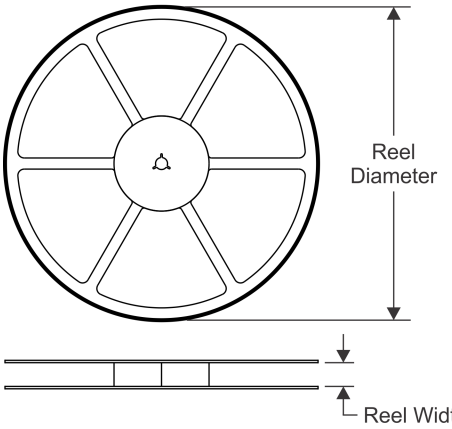
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

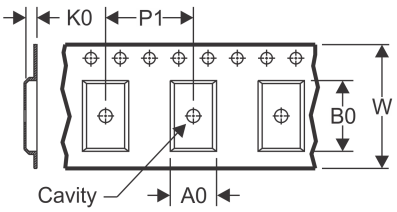
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

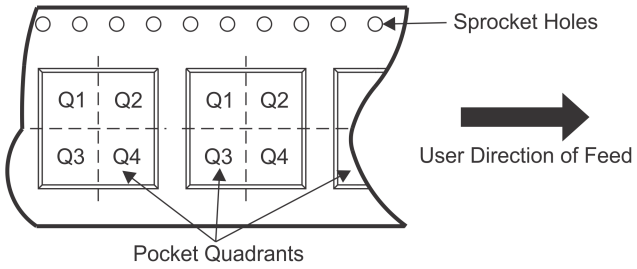


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

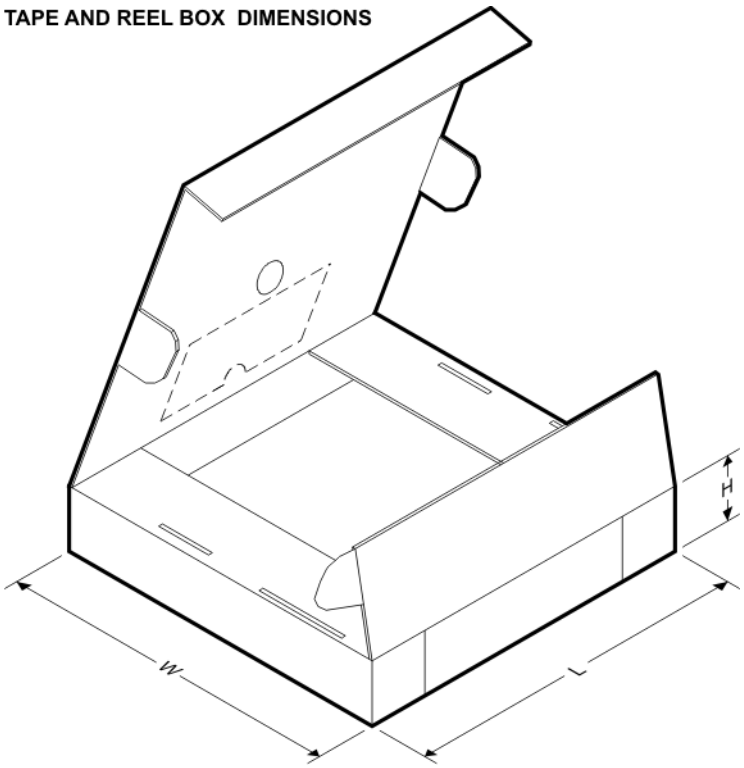
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV1T34DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LV1T34DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3

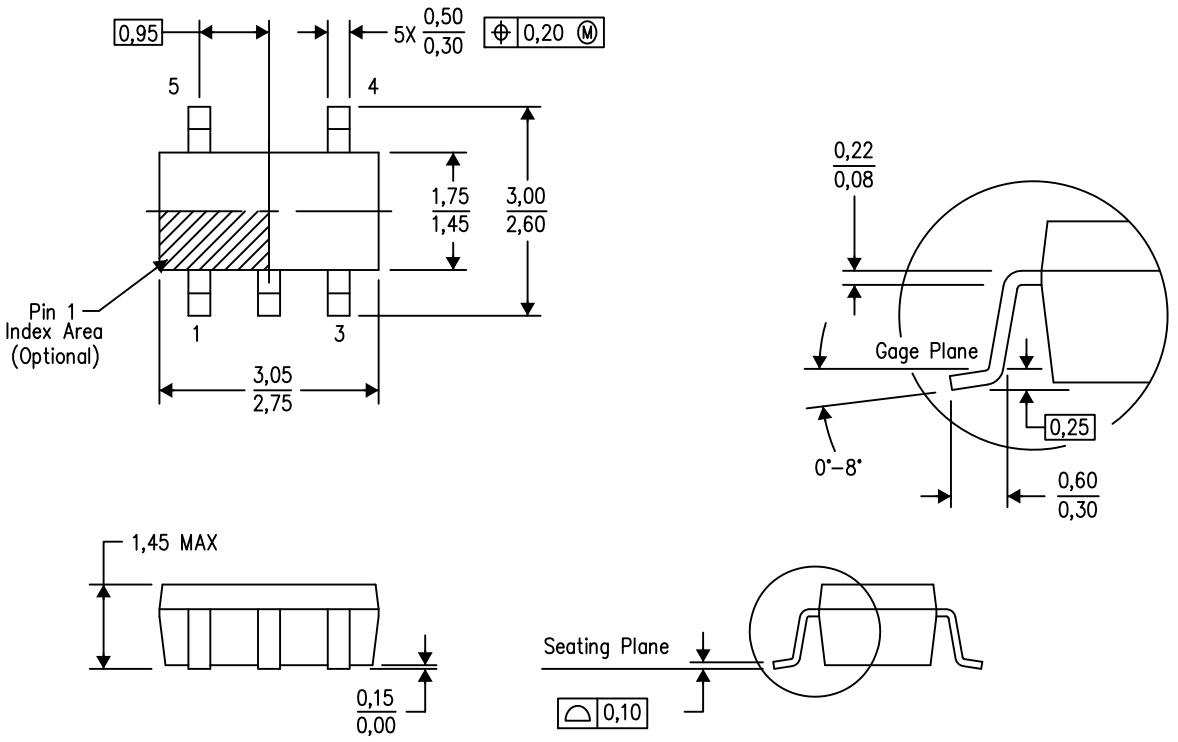
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

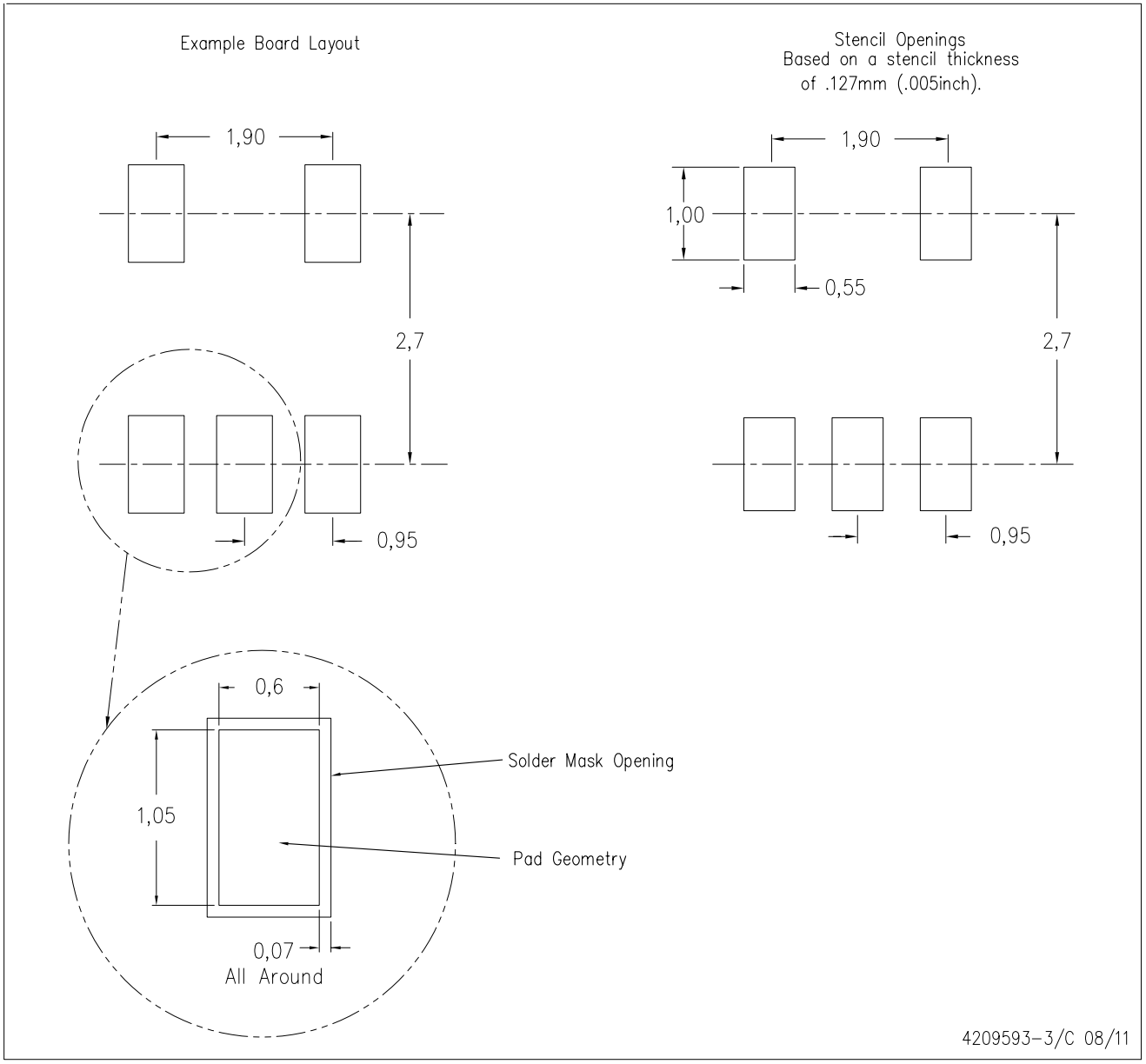
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV1T34DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74LV1T34DCKR	SC70	DCK	5	3000	180.0	180.0	18.0

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



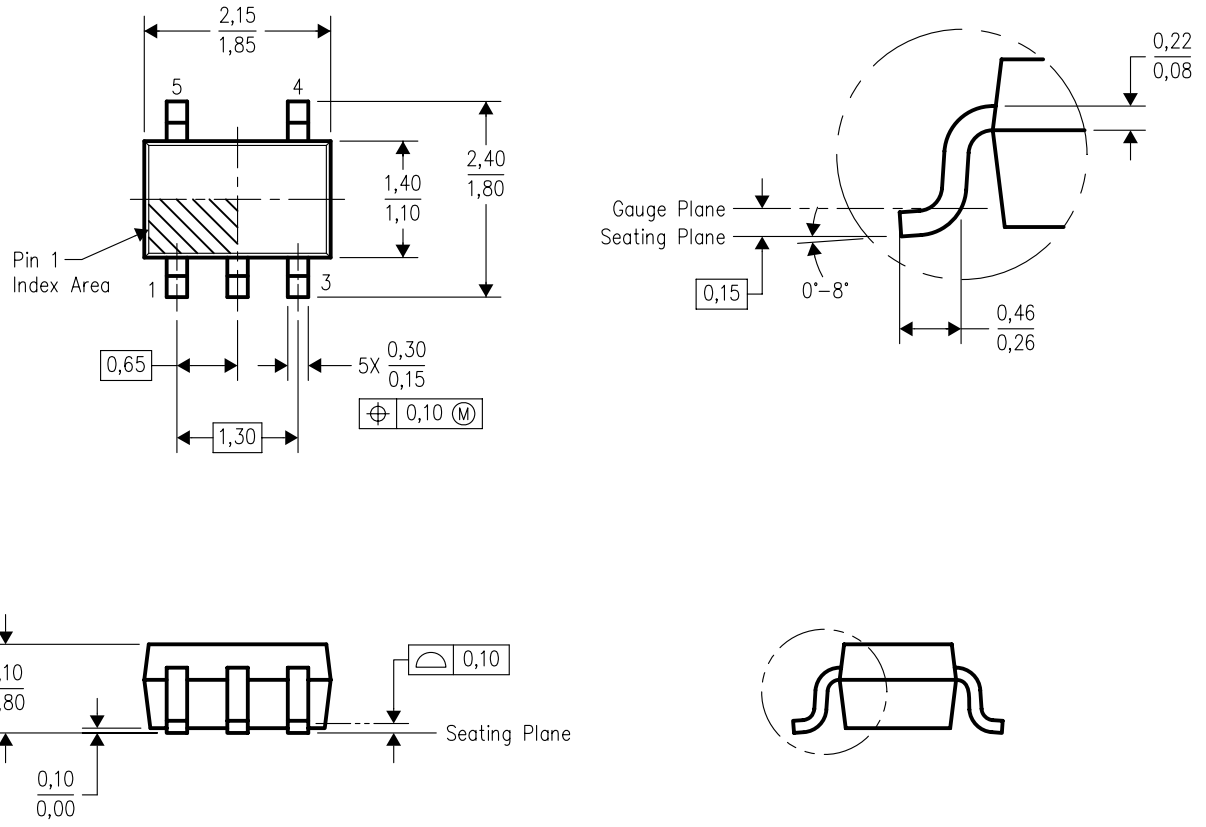
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

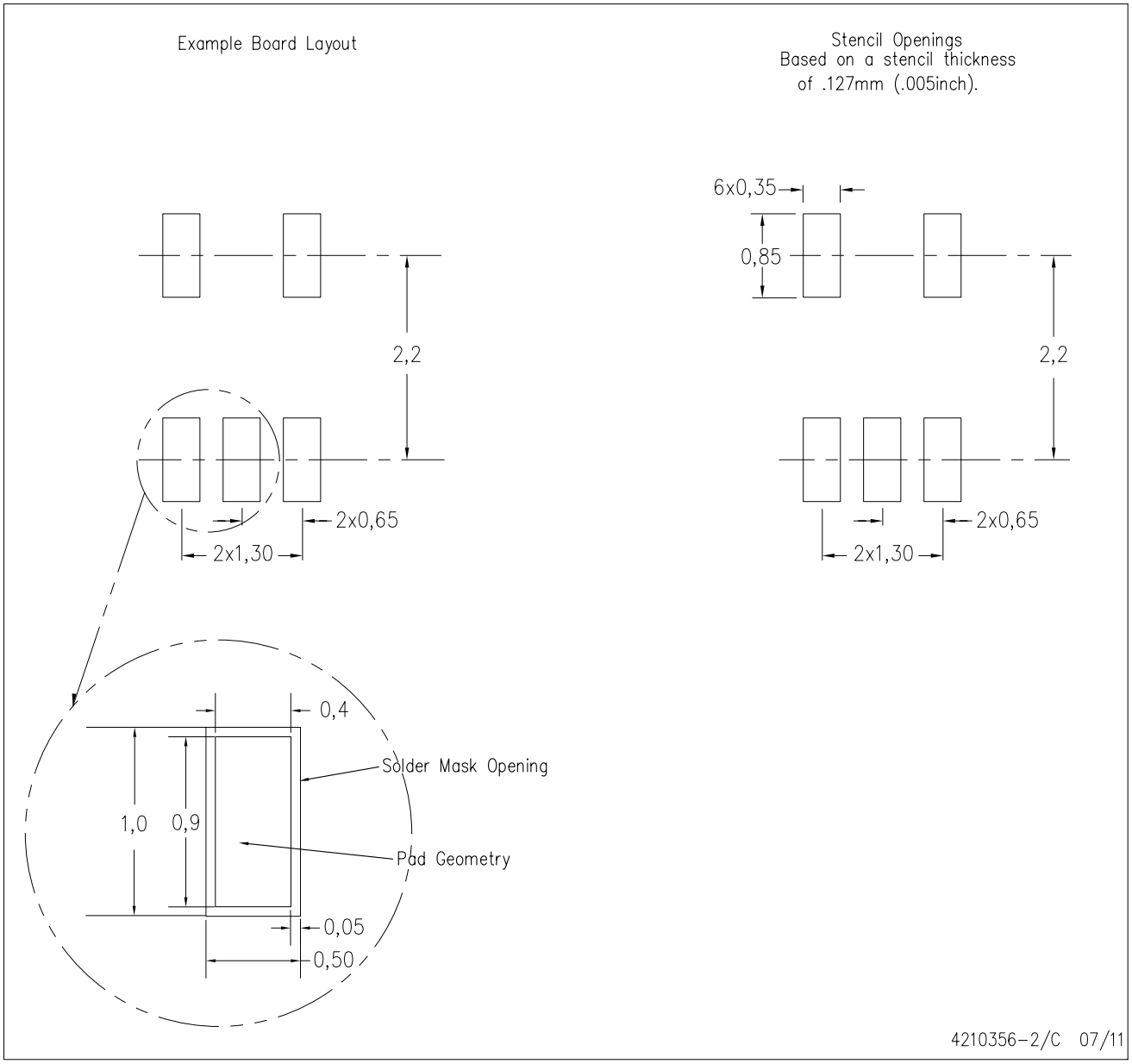
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



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D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

IMPORTANT NOTICE

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DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
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Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

SN series Manual

(V1.0 2015.03)

Thanks for purchasing our Electronic Speed Controller (ESC).The brushless system with high power for RC model can be very dangerous, so we strongly suggest you read this manual carefully. Any claims arising from the operating, failure or malfunctioning etc. will be denied. We assume no liability for personal injury, property damage or consequential damages resulting from our product or our workmanship. As far as is legally permitted, the obligation to compensation is limited to the invoice amount of the affected product. At the same time, We do not assume any liability arising from modifications due to unauthorized product. We reserve the right to change without notice about product design, appearance, performance and operational requirements.

Specification:

◆ Signal frequency:20-500Hz
◆ Outout PWM frequency:18KHz
◆ Application:SimonK/ BLheli firmware

Model	Continuous	Instant current	BEC	Battery	Weight	Size
SN16A	16A	18A	N/A	2~4S	7.6g	23x12x4.5mm
SN20A	20A	22A	N/A	2~4S	7.6g	23x12x4.5mm
HSN30A	30A	35A	N/A	2~6S	14.5g	45x16.6x5.5mm
HSN40A	40A	45A	N/A	2~6S	20.0g	60x17x7.2mm

Note: **The weight of SN16A/SN20A is only 2g without cable**.

◆ Specially for Multi-copter, throttle respond fast;
◆ Suit for throttle, which can compatible well with motor;
◆ Throttle signal is twisted pair cable, reduce the crosstalk while the signal transfer by the copper wire and flight more stable;
◆ The maximum refresh frequencyup to 500Hz throttle signal, compatible with all flight controls;
◆ Use new process ultra-low resistance MOSFET with miniaturization, and all flashes are N MOS with high withstanding current;
◆ Minaturization design, SN16/20A with high performance capacitor fliter on the board, weight reduce to 2g, also already thicken the PCB copper specially and low heat for small aircraft.

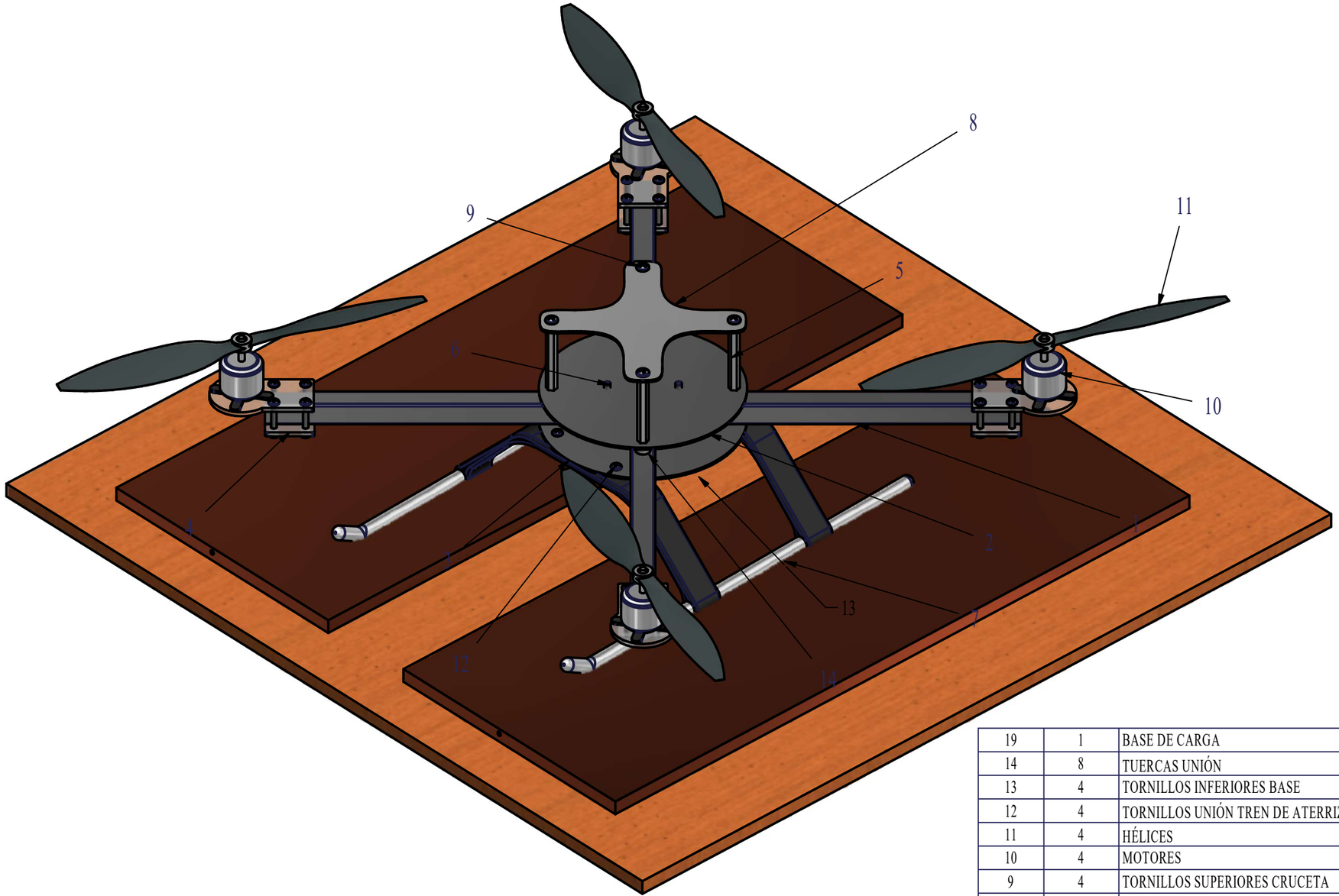
2. ANEXO 2 PLANOS

2.1. PLANOS MECÁNICOS

Plano general	CUADRICOPT.2016.1.01
Brazo del cuadricóptero	CUADRICOPT.2016.1.02
Base superior	CUADRICOPT.2016.1.03
Base inferior	CUADRICOPT.2016.1.04
Soporte motores	CUADRICOPT.2016.1.05
Tren de aterrizaje	CUADRICOPT.2016.1.06
Cruceta superior	CUADRICOPT.2016.1.07
Base de carga	CUADRICOPT.2016.1.08

2.2. PLANOS ELÉCTRÓNICOS

Circuito electrónico	CUADRICOPT.2016.1.09
Circuito electrónico PCB	CUADRICOPT.2016.1.10
Plano PCB	CUADRICOPT.2016.1.11



MARCA	CTDAD	DENOMINACIÓN Y CARACTERISTICAS	Nº PLANO / ABRE. NORMA	MATERIAL/OBSERVACIONES
19	1	BASE DE CARGA	CUADRICOPT.2016.1.08	MADERA
14	8	TUERCAS UNIÓN	ANSI B18.6.3	8-32 UNC-2B
13	4	TORNILLOS INFERIORES BASE	ANSI B18.6.3	6-32 UNC-2B
12	4	TORNILLOS UNIÓN TREN DE ATERRIZAJE	ANSI B18.6.3	6-32 UNC-2B
11	4	HÉLICES	GEMFAN 6030	
10	4	MOTORES	DYS BE 1806 2300 KV	
9	4	TORNILLOS SUPERIORES CRUCETA	ANSI B18.6.3	8-32 UNC-2B
8	1	CRUCETA SUPERIOR	CUADRICOPT.2016.1.07	ALUMINIO 6061
7	1	TREN DE ATERRIZAJE	CUADRICOPT.2016.1.06	ALUMINIO 6061
6	4	TORNILLOS UNIÓN BRAZOS	ANSI B18.6.3	8-32 UNC-2B
5	4	VARILLAS ROSCADAS	ANSI B18.6.3	ALUMINIO 6061
4	4	SOPORTE MOTORES	CUADRICOPT.2016.1.05	POLIETILENO ALTA DENSIDAD
3	1	BASE INFERIOR	CUADRICOPT.2016.1.04	ALUMINIO 6061
2	1	BASE SUPERIOR	CUADRICOPT.2016.1.03	ALUMINIO 6061
1	4	BRAZO CUADRICÓPTERO	CUADRICOPT.2016.1.02	ALUMINIO 6061

Observaciones Generales

Proyecto: CUADRICÓPTERO
Palabras clave:
Empresa: EUPLA
Estado del proyecto: En curso
Versión: V15

Observaciones de plano

Plano nº: 1 **de:** 1
Formato: A3
Coment:

	Fecha	Nombre
Dibujado	20/09/2016	M.URGEL
Comprobado		
Idem.s.normas		UNE-EN-ISO

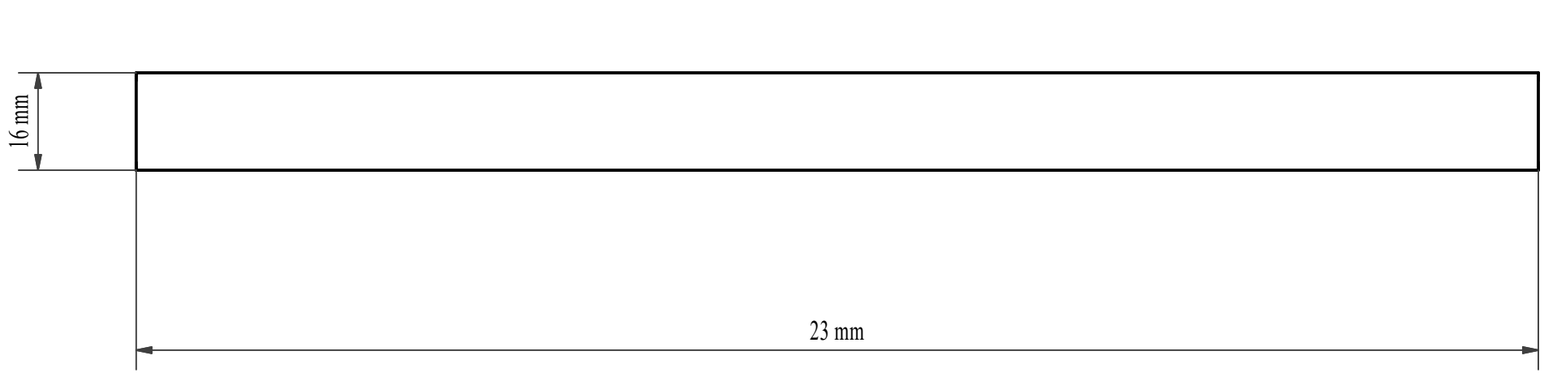
ESCALA 1:3

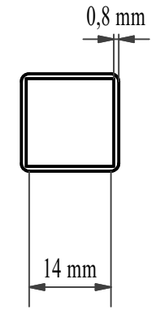
eupla
ESCUELA UNIVERSITARIA POLITECNICA
La Almunia de Dª Godina -ZARAGOZA-

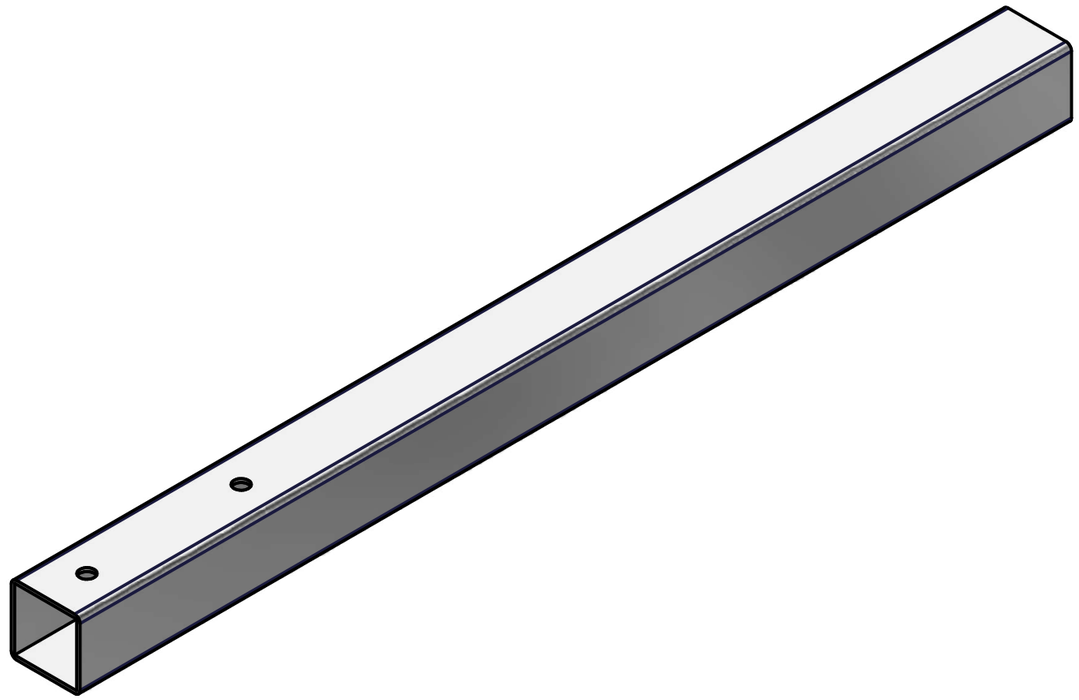
CUADRICÓPTERO

CUADRICÓPTERO
COMPONENTES

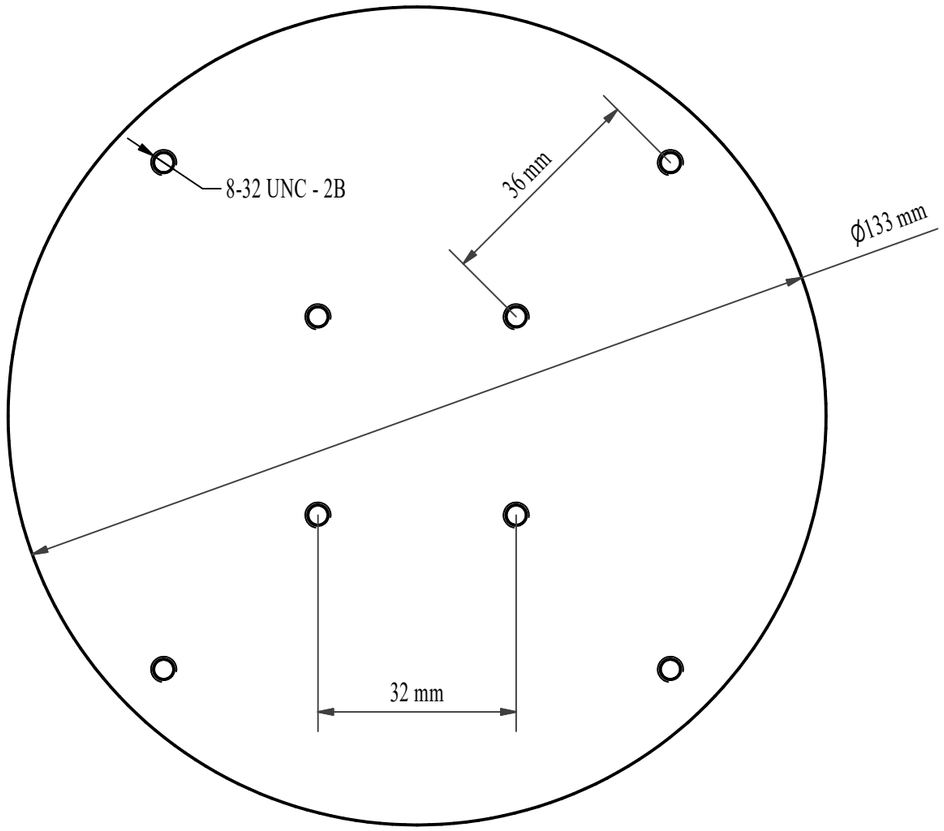
Nº P.: CUADRICOPT.2016.1.01
Nº O.: CUADRICOPT.2016.1.01
Nom.Ar.: Cuadricoptero lista.idw

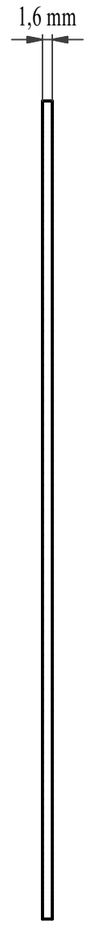


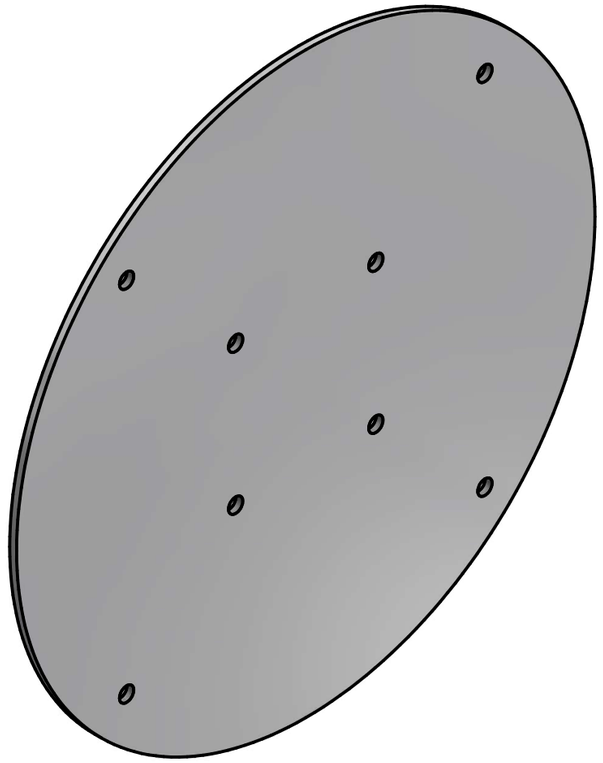




Observaciones Generales	Observaciones de plano		Fecha	Nombre		eupla
Proyecto: CUADRICOPTERO	**Plano nº:** 1 **de:** 1	**Dibujado**	20/09/2016	M.URGEL		ESCUELA UNIVERSITARIA POLITECNICA
Palabras clave:	**Formato:** A3	**Comprobado**				La Almunia de Dª Godina -ZARAGOZA-
Empresa: EUPLA	**Coment:**	**Idem.s.normas**		UNE-EN-ISO		
Estado del proyecto: En curso		**ESCALA** 1:1	**CUADRICÓPTERO** CUADRICÓPTERO BRAZO			**Nº P.:** CUADRICOPT.2016.1.02
Versión: V4						**Nº O.:** CUADRICOPT.2016.1.01
						Nom.Ar.: Brazo.idw







Observaciones Generales	Observaciones de plano		Fecha	Nombre		
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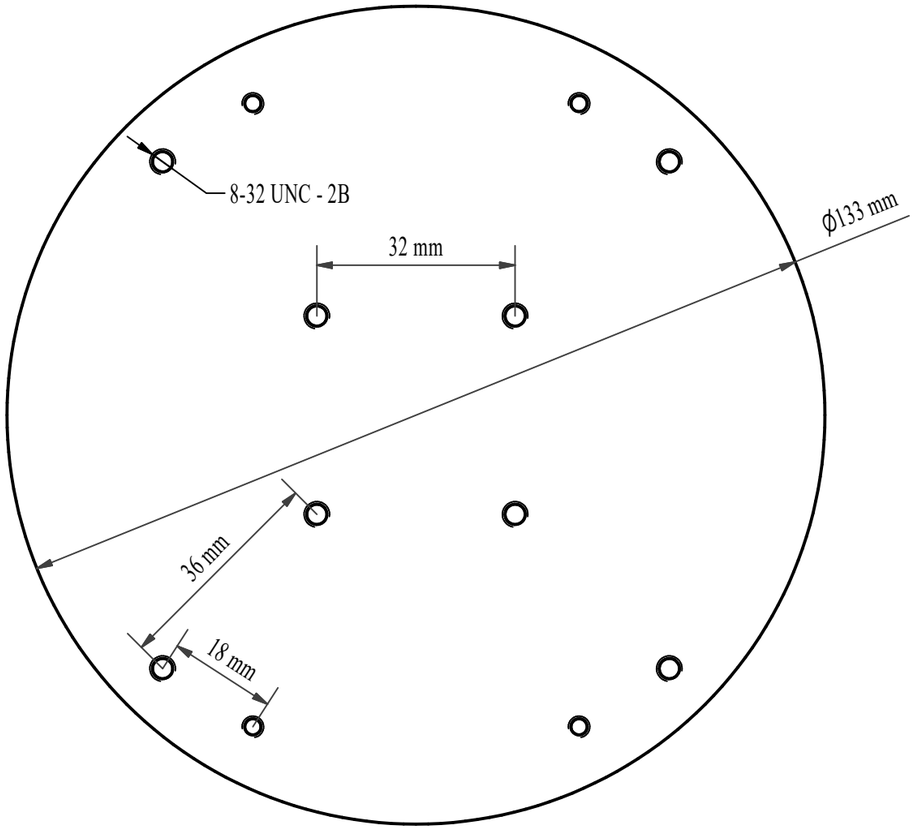
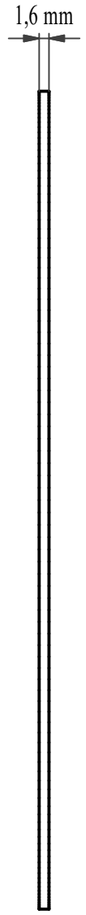
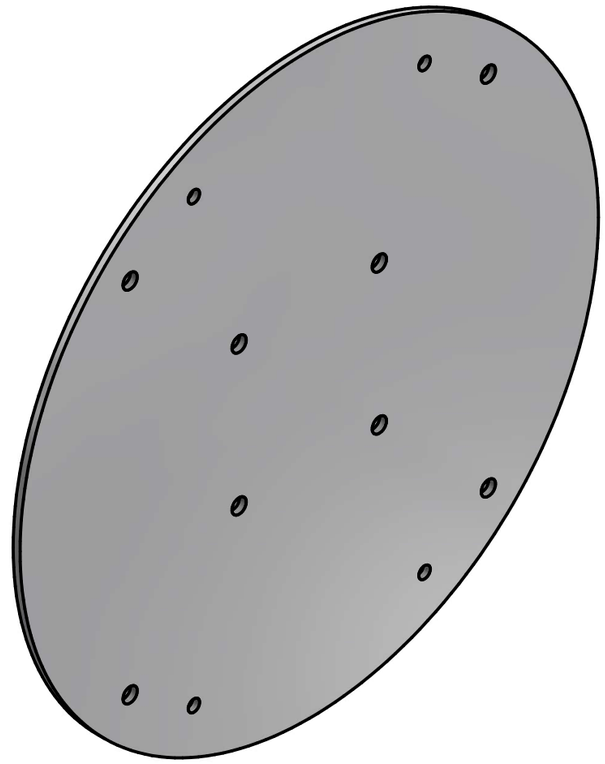
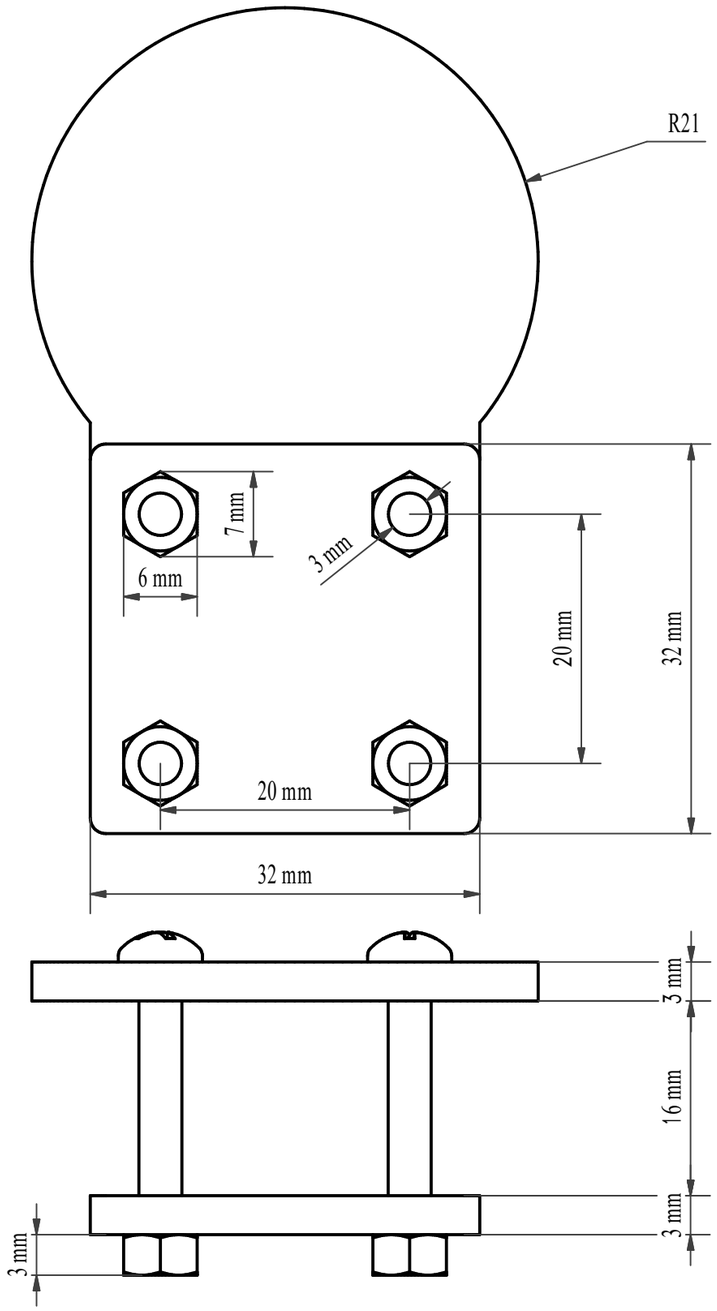
		Comprobado				
		Idem.s.normas		UNE-EN-ISO		
		ESCALA 1:1	**CUADRICÓPTERO** CUADRICÓPTERO BASE SUPERIOR		**Nº P.:** CUADRICOPT.2016.1.03 **Nº O.:** CUADRICOPT.2016.1.01 **Nom.Ar.:** BaseSuperior.idw	

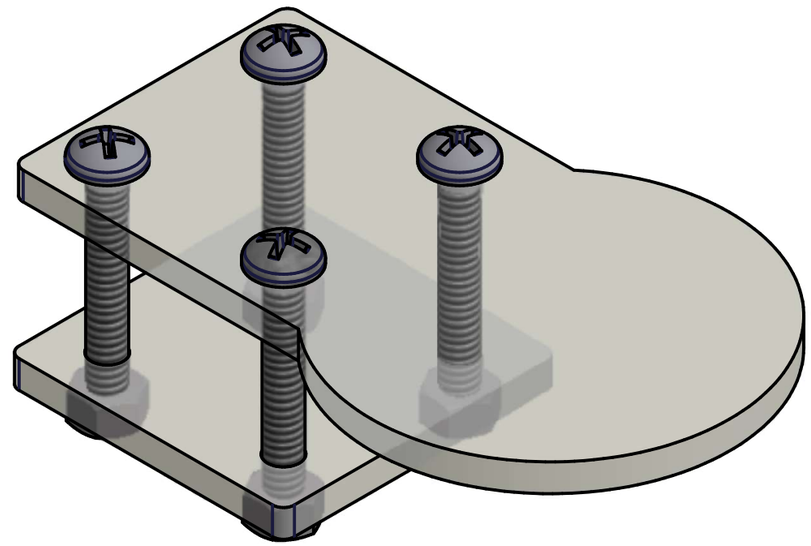




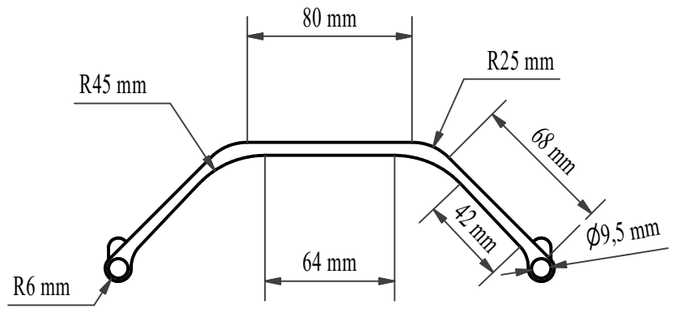


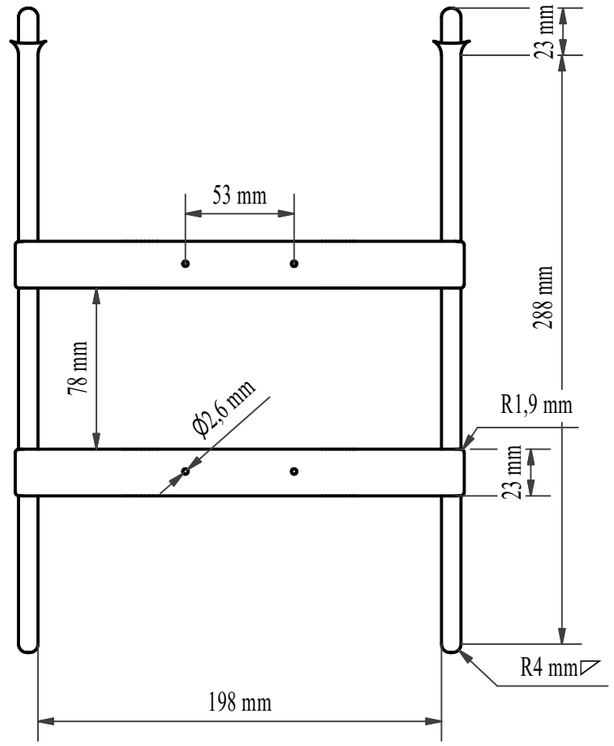
Observaciones Generales	Observaciones de plano		Fecha	Nombre		eupla
Proyecto: CUADRICÓPTERO	**Plano nº:** 1 **de:** 1	**Dibujado**	20/09/2016	M.URGEL		ESCUELA UNIVERSITARIA POLITECNICA
Palabras clave:	**Formato:** A3	**Comprobado**				La Almunia de Dª Godina -ZARAGOZA-
Empresa: EUPLA	**Coment:**	**Idem.s.normas**		UNE-EN-ISO		
Estado del proyecto: En curso		**ESCALA** 1:1	**CUADRICÓPTERO** CUADRICÓPTERO BASE INFERIOR			**Nº P.:** CUADRICOPT.2016.1.04
Versión: V3						**Nº O.:** CUADRICOPT.2016.1.01
						Nom.Ar.: BaseInferior.idw



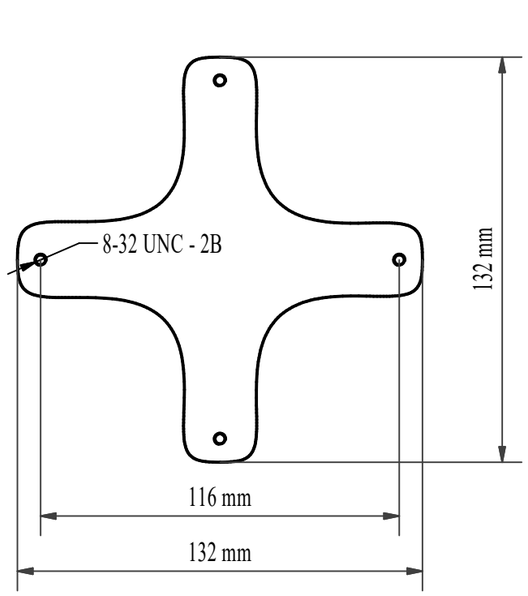


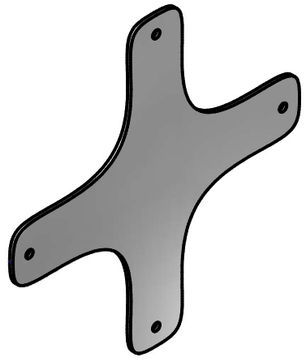
Observaciones Generales	Observaciones de plano		Fecha	Nombre		eupla
Proyecto: CUADRICÓPTERO **Palabras clave:** **Empresa:** EUPLA **Estado del proyecto:** En curso **Versión:** V6	**Plano nº:** 1 **de:** 1 **Formato:** A3 **Coment:**	**Dibujado**	20/09/2016	M.URGEL		ESCUELA UNIVERSITARIA POLITECNICA La Almunia de Dª Godina -ZARAGOZA-
		Comprobado				
		Idem.s.normas		UNE-EN-ISO		
		ESCALA 2:1	**CUADRICÓPTERO** CUADRICÓPTERO SOPORTE MOTORES		**Nº P.:** CUADRICOPT.2015.1.05 **Nº O.:** CUADRICOPT.2015.1.01 **Nom.Ar.:** SoporteMotores.idw	



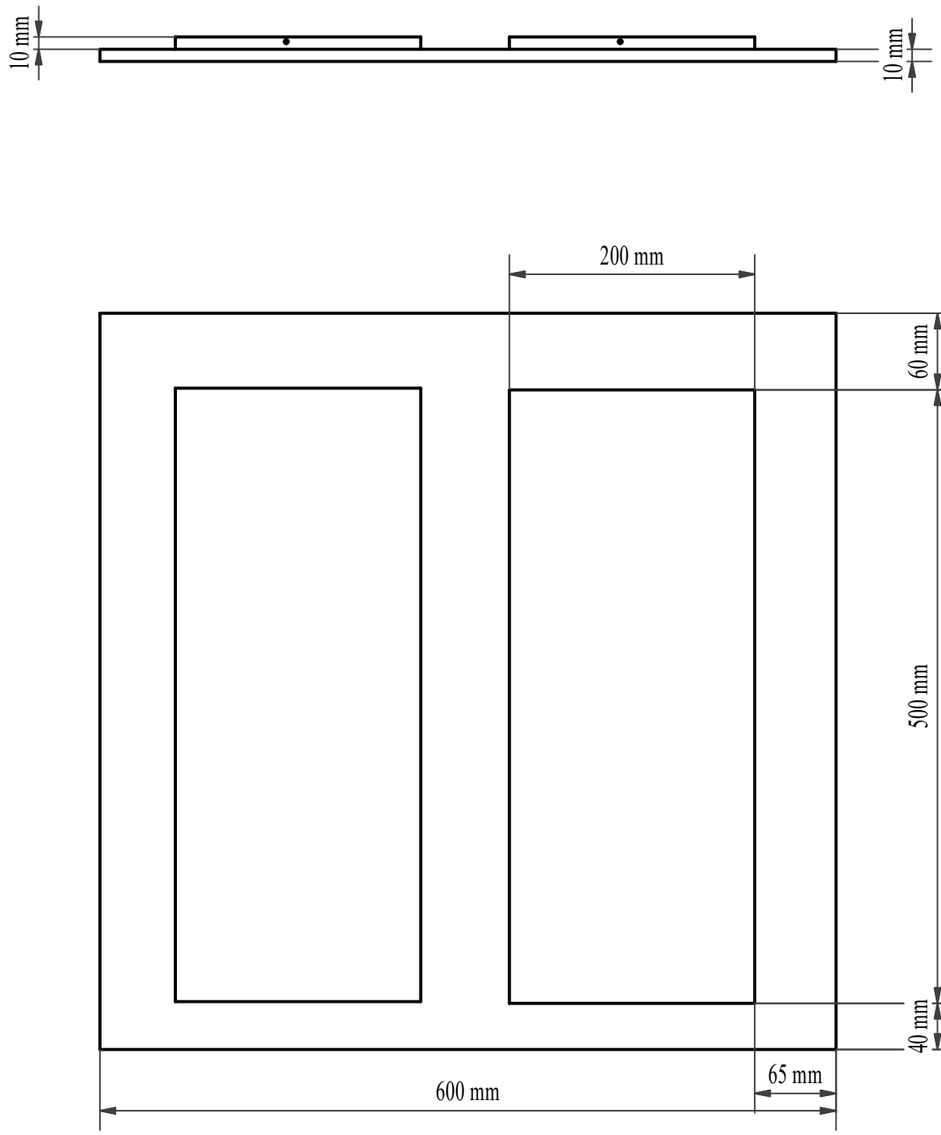


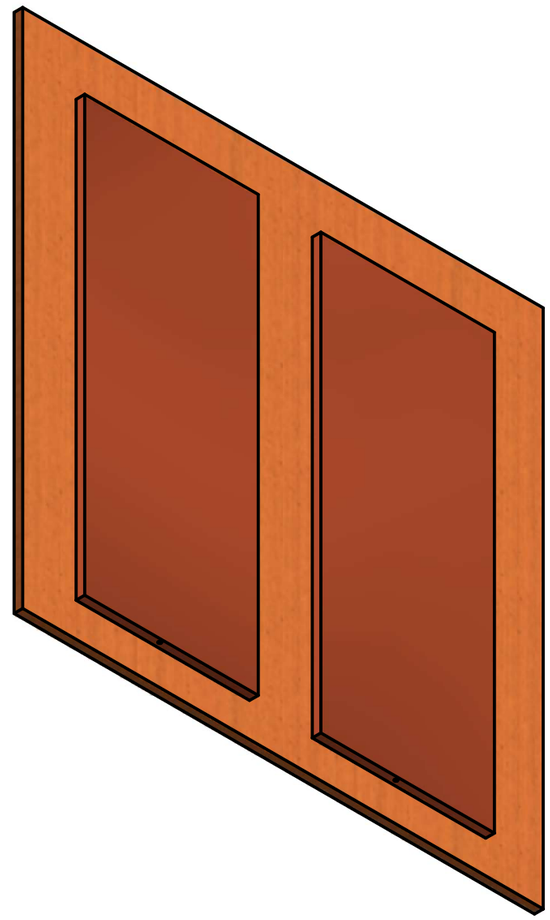
Observaciones Generales	Observaciones de plano		Fecha	Nombre		
Proyecto: CUADRICÓPTERO **Palabras clave:** **Empresa:** EUPLA **Estado del proyecto:** En curso **Versión:** V5	**Plano nº:** 1 **de:** 1 **Formato:** A3 **Coment:**	**Dibujado**	20/09/2016	M.URGEL	eupla ESCUELA UNIVERSITARIA POLITECNICA La Almunia de Dª Godina -ZARAGOZA-	
		Comprobado				
		Idem.s.normas		UNE-EN-ISO		
		ESCALA 1:3	**CUADRICÓPTERO** CUADRICÓPTERO TREN DE ATERRIZAJE		**Nº P.:** CUADRICOPT.2016.1.06 **Nº O.:** CUADRICOPT.2016.1.01 **Nom.Ar.:** Tren de aterrizaje.idw	



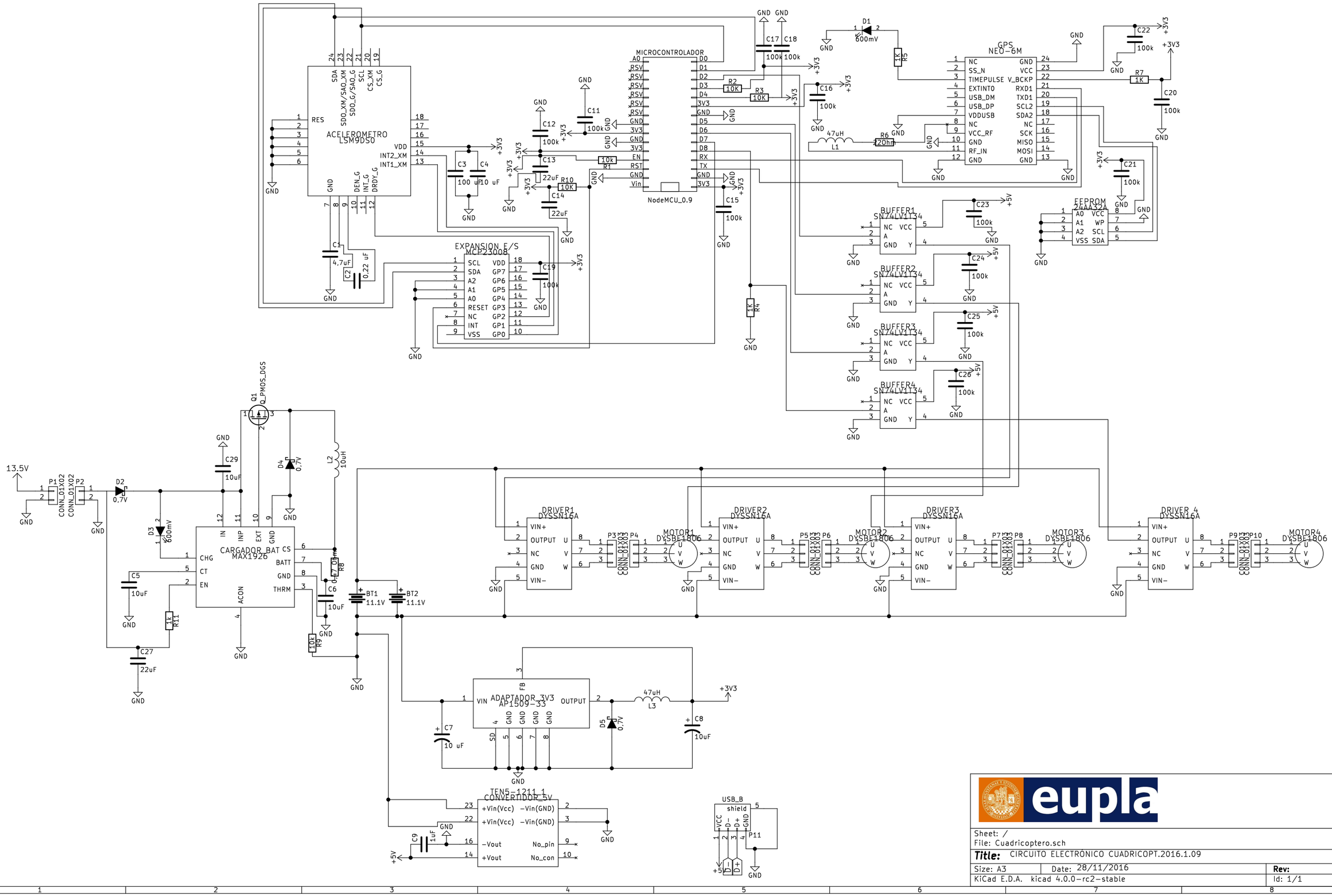


Observaciones Generales	Observaciones de plano		Fecha	Nombre		eupla
Proyecto: CUADRICÓPTERO **Palabras clave:** **Empresa:** EUPLA **Estado del proyecto:** En curso **Versión:** V5	**Plano nº:** 1 **de:** 1 **Formato:** A3 **Coment:**	**Dibujado**	20/09/2016	M.URGEL		ESCUELA UNIVERSITARIA POLITECNICA La Almunia de Dª Godina -ZARAGOZA-
		Comprobado				
		Idem.s.normas		UNE-EN-ISO		
		ESCALA 1:2	**CRUCETA SUPERIOR** CUADRICÓPTERO CRUCETA SUPERIOR		**Nº P.:** CUADRICOPT.2016.1.07 **Nº O.:** CUADRICOPT.2016.1.01 **Nom.Ar.:** Cruceta superior.idw	





Observaciones Generales	Observaciones de plano		Fecha	Nombre		
Proyecto: CUADRICÓPTERO	**Plano nº:** 1 **de:** 1	**Dibujado**	01/11/2016	M.URGEL	eupla	
Palabras clave:	**Formato:** A3	**Comprobado**			ESCUELA UNIVERSITARIA POLITECNICA	
Empresa: EUPLA	**Coment:**	**Idem.s.normas**		UNE-EN-ISO	La Almunia de Dª Godina -ZARAGOZA-	
Estado del proyecto: En curso		**ESCALA** 1:5	**CUADRICÓPTERO** CUADRICÓPTERO BASE DE CARGA		**Nº P.:** CUADRICOPT.2016.1.08	
Versión: V3					**Nº O.:** CUADRICOPT.2016.1.01	
					Nom.Ar.: Base de carga.idw	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LSM9DS0
MICROCONTROLADOR
NodeMCU_0.9
GPS
NEO-6M
EXPANSION E/S
MCP23008
EEPROM
24AA32A
BUFFER1
SN74LV1T34
BUFFER2
SN74LV1T34
BUFFER3
SN74LV1T34
BUFFER4
SN74LV1T34
CARGADOR_BAT
MAX1926
ADAPTADOR_3V3
AP1509-33
CONVERTIDOR_5V
TEN5-1211_1
DRIVER1
DYSSN16A
DRIVER2
DYSSN16A
DRIVER3
DYSSN16A
DRIVER 4
DYSSN16A
MOTOR1
DYSBF1806
MOTOR2
DYSBF1806
MOTOR3
DYSBF1806
MOTOR4
DYSBF1806
USB_B
13.5V
GND
+3V3
+5V
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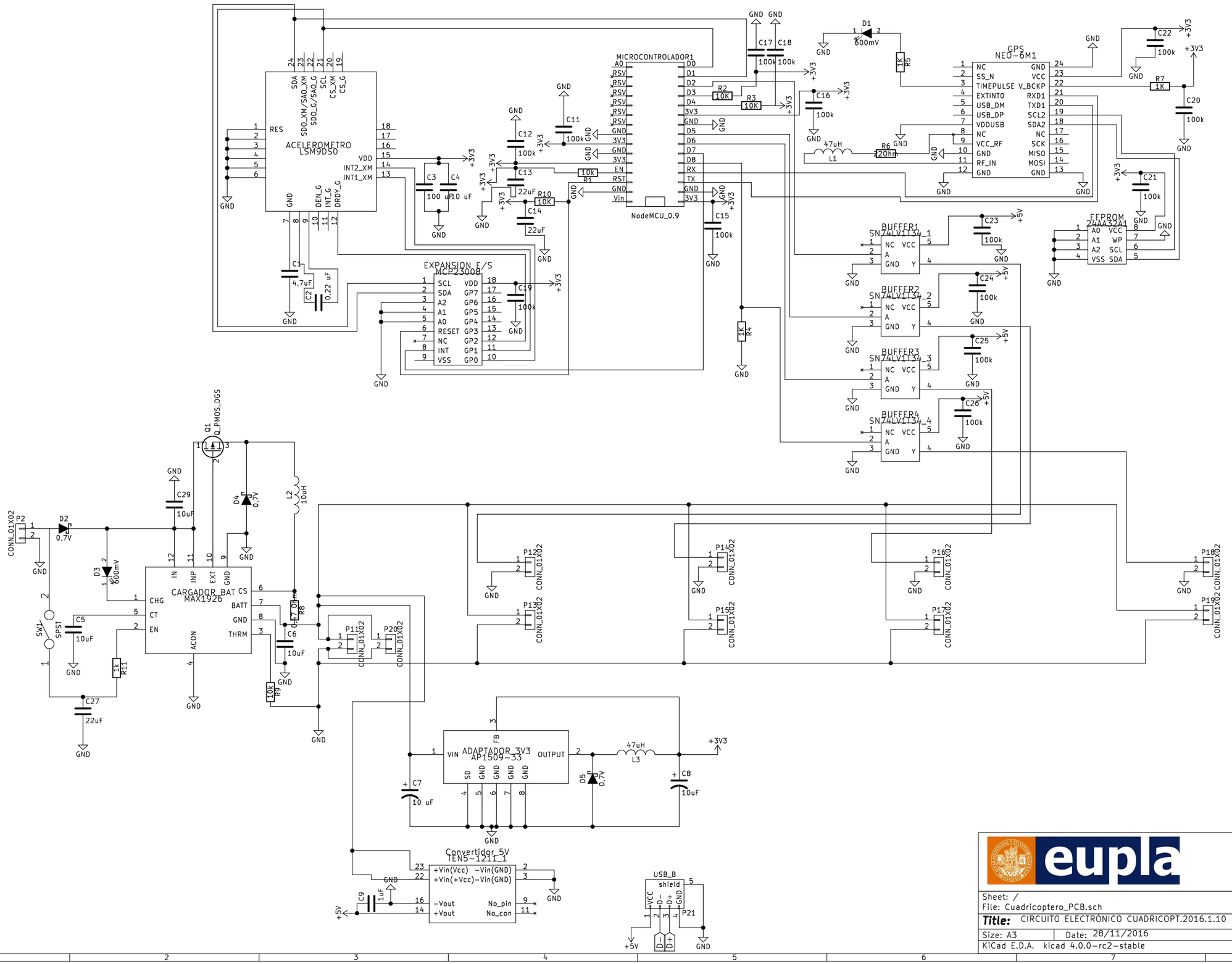
Size: A3
Date: 28/11/2016
KiCad E.D.A. kicad 4.0.0-rc2-stable
Rev:
Id: 1/1



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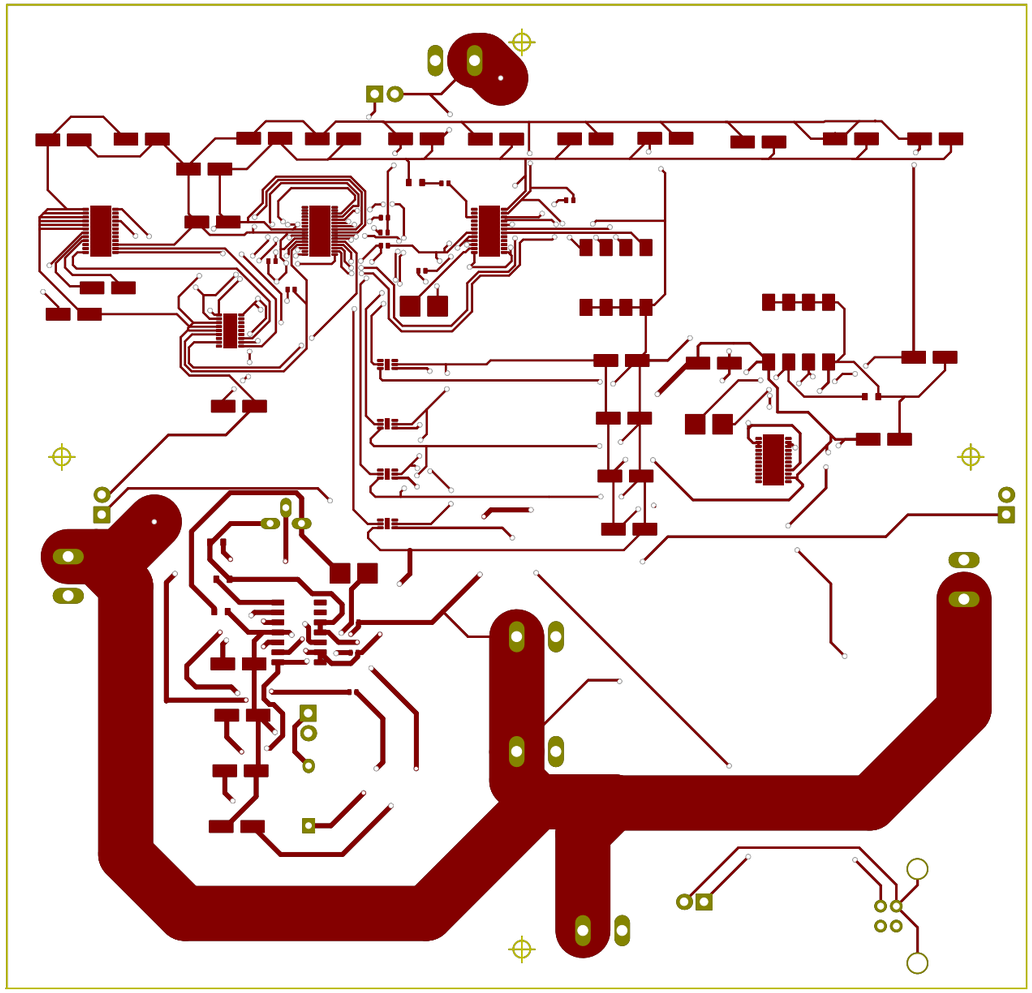

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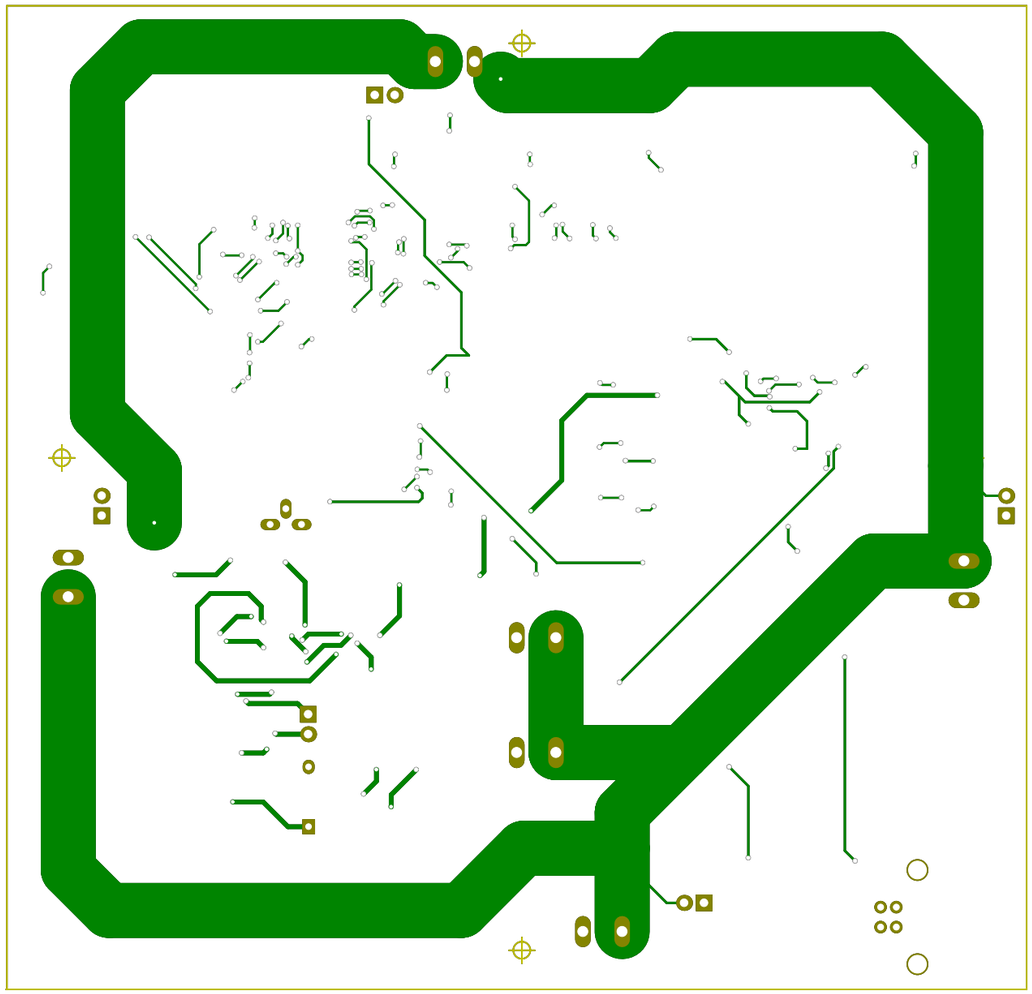

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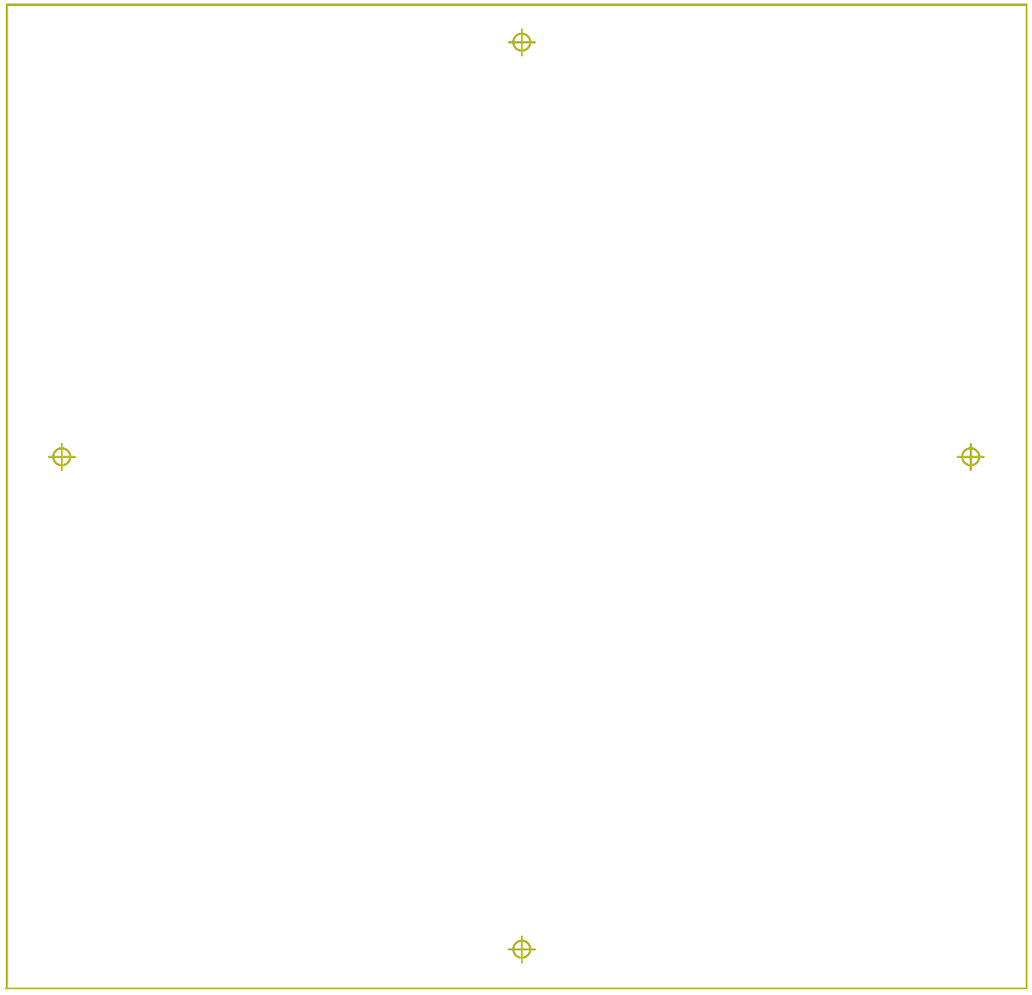

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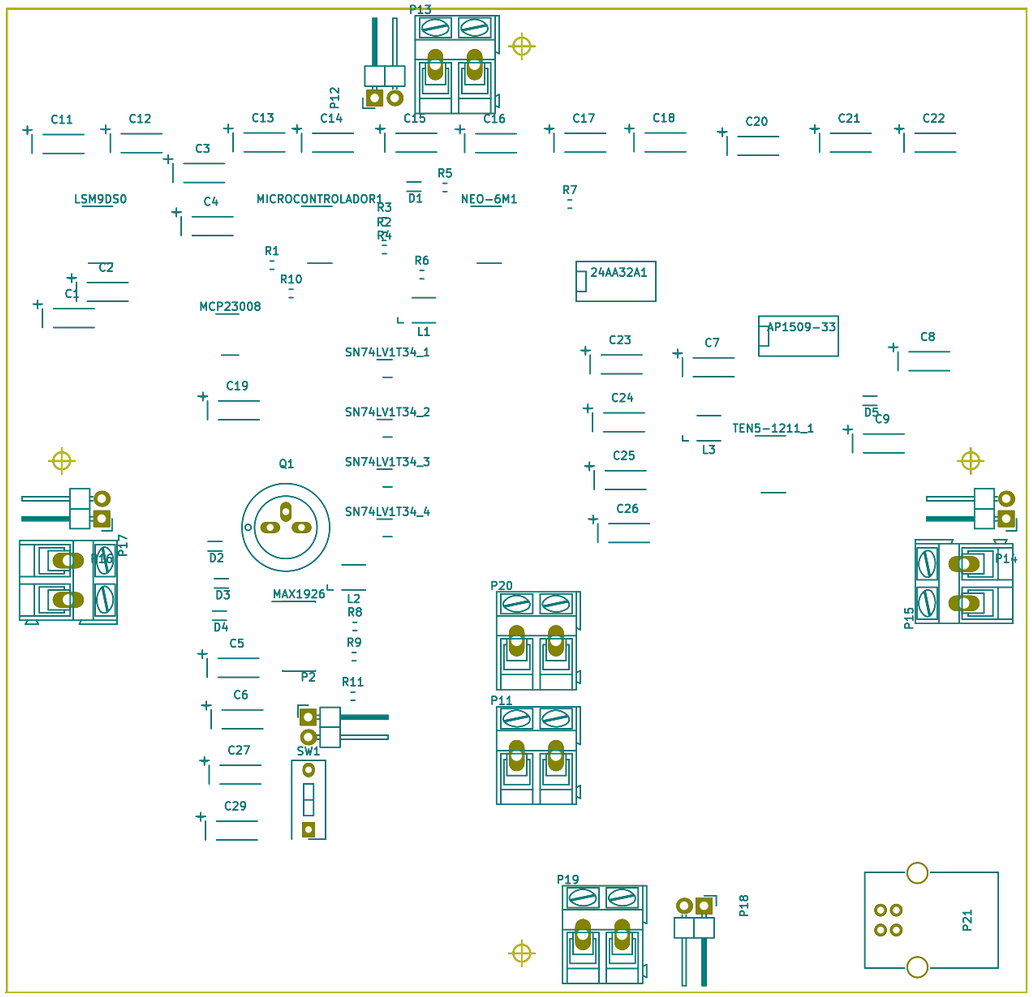

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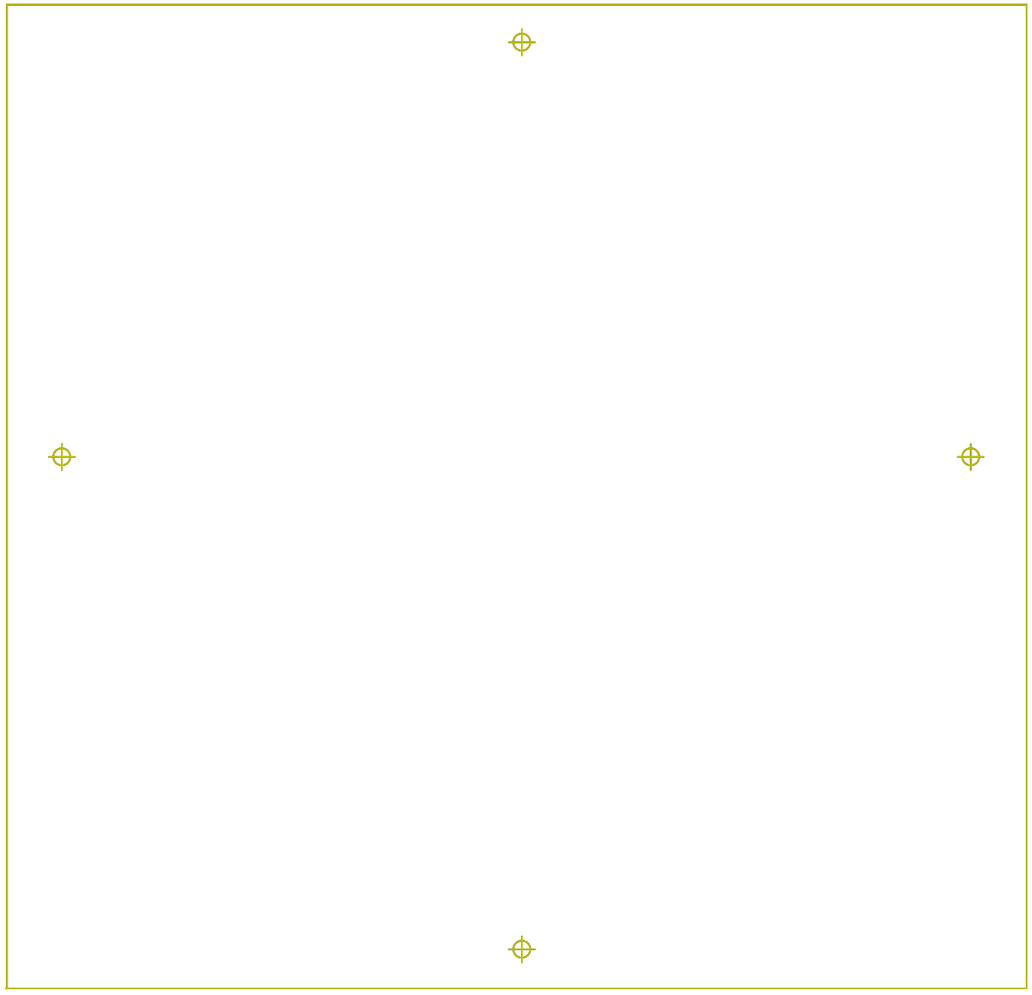

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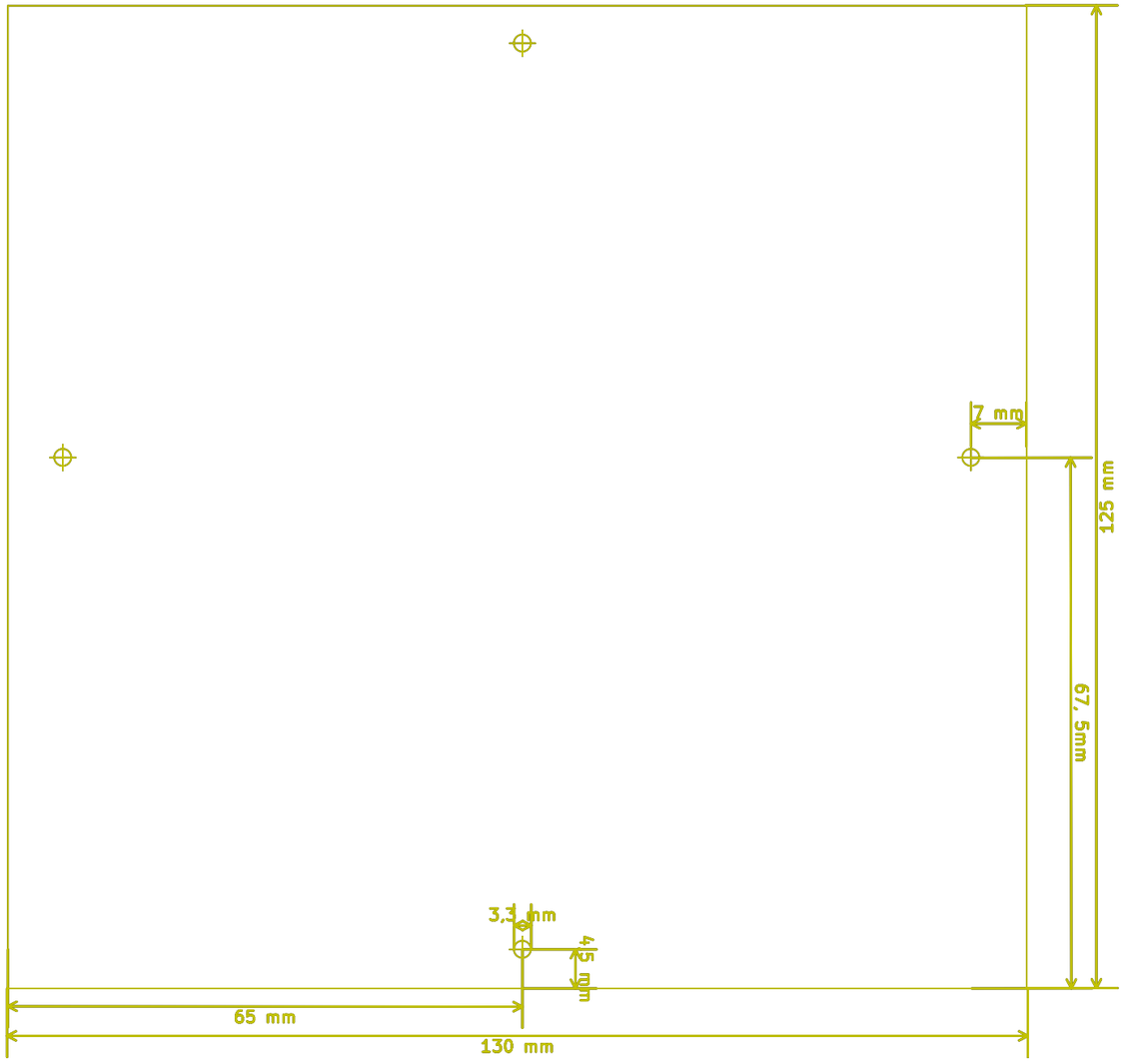

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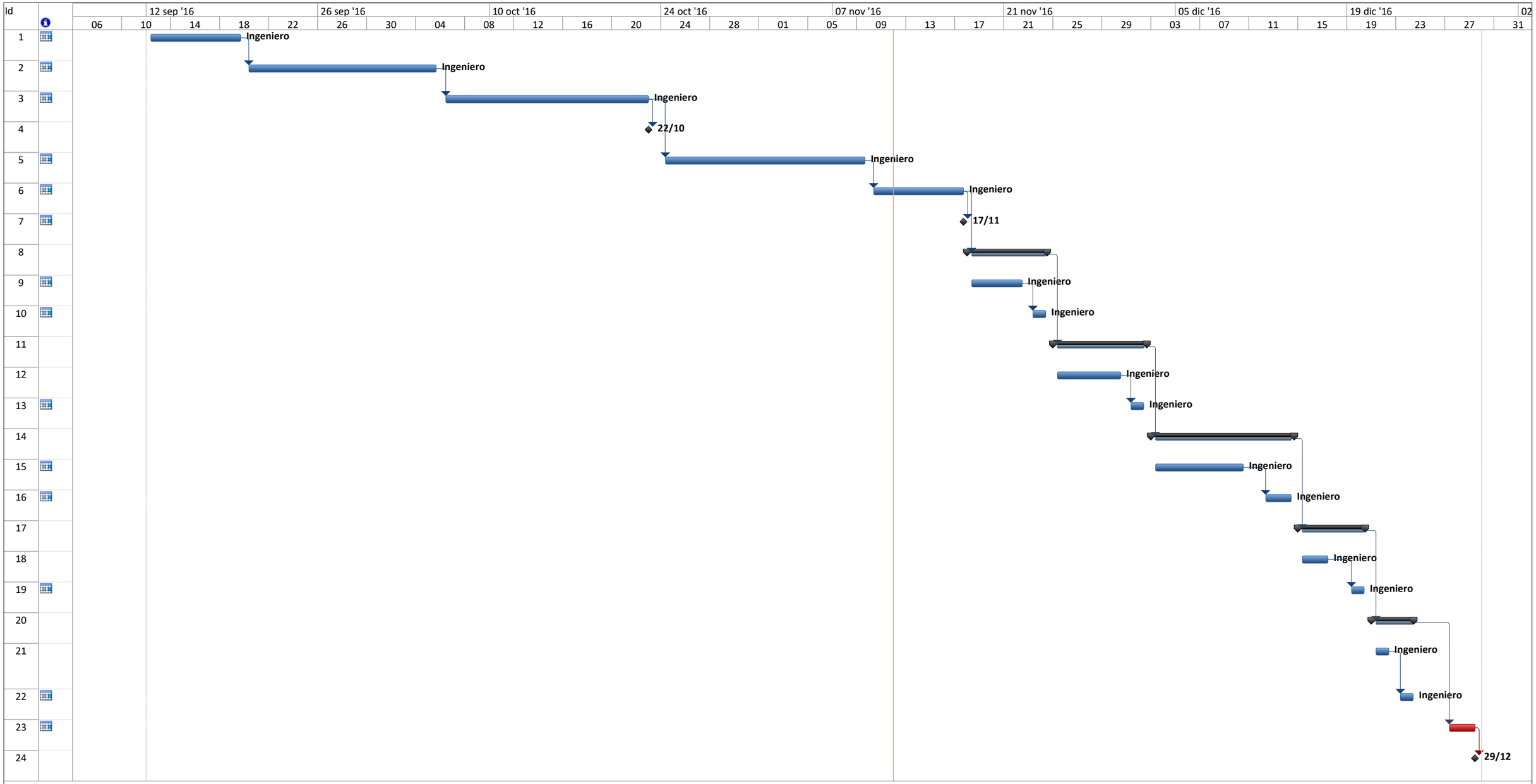
3. ANEXO 3 PLANIFICACIÓN

En este anexo se va a exponer la planificación llevada a cabo para la realización del proyecto.

3.1. ÍNDICE ANEXOS

1. Lista de tareas e hitos
2. Diagrama de Gantt
3. Informe de costes

Id	Modo de tarea	Nombre de tarea	Duración	Comienzo	Fin	Predecesoras
1		Introducción	1 sem	lun 12/09/16	lun 19/09/16	
2		Marco teórico	2 sem.	mar 20/09/16	mié 05/10/16	1
3		Diseño mecánico	2 sem.	jue 06/10/16	sáb 22/10/16	2
4		Hito 1	0 días	sáb 22/10/16	sáb 22/10/16	3
5		Diseño electrónico PCB	2 sem.	lun 24/10/16	mié 09/11/16	3
6		Diseño de software de control	1 sem	jue 10/11/16	jue 17/11/16	5
7		Hito 2	0 días	jue 17/11/16	jue 17/11/16	6
8		**Finalización del diseño**	**5 días**	**vie 18/11/16**	**jue 24/11/16**	**6**
9		Documentación	3 días	vie 18/11/16	mar 22/11/16	
10		Presentación	1 día	mié 23/11/16	jue 24/11/16	9
11		**Construcción de la estructura**	**6 días**	**vie 25/11/16**	**vie 02/12/16**	**8**
12		Fabricación estructura	4 días	vie 25/11/16	mié 30/11/16	
13		Test de la estructura	1 día	jue 01/12/16	vie 02/12/16	12
14		**Construcción de la PCB**	**7 días**	**sáb 03/12/16**	**mié 14/12/16**	**11**
15		Fabricación PCB	4 días	sáb 03/12/16	sáb 10/12/16	
16		Test PCB	2 días	lun 12/12/16	mié 14/12/16	15
17		**Implementación de motores**	**4 días**	**jue 15/12/16**	**mar 20/12/16**	**14**
18		Montaje motores	2 días	jue 15/12/16	sáb 17/12/16	
19		Test motores	1 día	lun 19/12/16	mar 20/12/16	18
20		**Montaje componentes electrónicos**	**3 días**	**mié 21/12/16**	**sáb 24/12/16**	**17**
21		Montaje componentes electrónicos	1 día	mié 21/12/16	jue 22/12/16	
22		Test componentes electrónicos	1 día	vie 23/12/16	sáb 24/12/16	21
23		Implementación software control	2 días	mar 27/12/16	jue 29/12/16	20
24		Final del proyecto	0 días	jue 29/12/16	jue 29/12/16	23



Proyecto: Gantt.mpp
Fecha: sáb 12/11/16

Tarea	Resumen del proyecto	Hito inactivo		Informe de resumen manual		Fecha límite	
División	Tareas externas	Resumen inactivo		Resumen manual		Tareas críticas	
Hito	Hito externo	Tarea manual		Sólo el comienzo		División crítica	
Resumen	Tarea inactiva	Sólo duración		Sólo fin		Progreso	

Informe presupuestario el sáb 12/11/16
Gantt.mpp

Id	Nombre de tarea	Costo fijo	Acumulación de costos fijos	Costo total	Previsto	Variación	Real	Restante
2	Marco teórico	0,00 €	Prorrateo	1.440,00 €	0,00 €	1.440,00 €	0,00 €	1.440,00 €
3	Diseño mecánico	0,00 €	Prorrateo	1.440,00 €	0,00 €	1.440,00 €	0,00 €	1.440,00 €
5	Diseño electrónico PCB	0,00 €	Prorrateo	1.440,00 €	0,00 €	1.440,00 €	0,00 €	1.440,00 €
1	Introducción	0,00 €	Prorrateo	720,00 €	0,00 €	720,00 €	0,00 €	720,00 €
6	Diseño de software de control	0,00 €	Prorrateo	720,00 €	0,00 €	720,00 €	0,00 €	720,00 €
12	Fabricación estructura	0,00 €	Prorrateo	480,00 €	0,00 €	480,00 €	0,00 €	480,00 €
15	Fabricación PCB	0,00 €	Prorrateo	480,00 €	0,00 €	480,00 €	0,00 €	480,00 €
9	Documentación	0,00 €	Prorrateo	360,00 €	0,00 €	360,00 €	0,00 €	360,00 €
16	Test PCB	0,00 €	Prorrateo	240,00 €	0,00 €	240,00 €	0,00 €	240,00 €
18	Montaje motores	0,00 €	Prorrateo	240,00 €	0,00 €	240,00 €	0,00 €	240,00 €
23	Implementación software control	0,00 €	Prorrateo	240,00 €	0,00 €	240,00 €	0,00 €	240,00 €
10	Presentación	0,00 €	Prorrateo	120,00 €	0,00 €	120,00 €	0,00 €	120,00 €
13	Test de la estructura	0,00 €	Prorrateo	120,00 €	0,00 €	120,00 €	0,00 €	120,00 €
19	Test motores	0,00 €	Prorrateo	120,00 €	0,00 €	120,00 €	0,00 €	120,00 €
21	Montaje componentes electrónic	0,00 €	Prorrateo	120,00 €	0,00 €	120,00 €	0,00 €	120,00 €
22	Test componentes electrónicos	0,00 €	Prorrateo	120,00 €	0,00 €	120,00 €	0,00 €	120,00 €
4	Hito 1	0,00 €	Prorrateo	0,00 €	0,00 €	0,00 €	0,00 €	0,00 €
7	Hito 2	0,00 €	Prorrateo	0,00 €	0,00 €	0,00 €	0,00 €	0,00 €
24	Final del proyecto	0,00 €	Prorrateo	0,00 €	0,00 €	0,00 €	0,00 €	0,00 €
		0,00 €		8.400,00 €	0,00 €	8.400,00 €	0,00 €	8.400,00 €

4. ANEXO 4 PRESUPUESTO

4.1. COMPONENTES MECÁNICOS

Unidades	Artículo	Precio/Unidad(€)	Precio(€)
4	Motor DYS BE1806 2300Kv	7,33 €	29,32 €
4	Hélices Gemfan 6030 paso 3 6"	1,97 €	7,86 €
1	Perfil cuadrado aluminio 14x16 50cm	2,50 €	2,50 €
1	Lámina aluminio 1,6mm	8,81 €	8,81 €
1	Polietileno alta densidad granulado 200g	2,47 €	2,47 €
1	Caja 100 tornillos 8-32	3,95 €	3,95 €
1	Caja 20 tuercas 8-32	2,60 €	2,60 €
1	Plancha aluminio 1000mmx1000mm 10mm espesor	6,54 €	6,54 €
		TOTAL	64,05 €

4.2. COMPONENTES ELECTRÓNICOS

Unidades	Artículo	Precio/Unidad(€)	Precio(€)
1	Microcontrolador NodeMCU	6,67 €	6,67 €
1	GPS Neo-6M	16,67 €	16,67 €
1	Acelerómetro, giroscopio, magnetómetro LSM9DS0	23,23 €	23,23 €
1	EEPROM 24AA32A1	17,42 €	17,42 €
1	Cámara Xiaomi YiCam	67,17 €	67,17 €
4	Buffer Texas SN74LV1T34	1,89 €	7,56 €
4	Drivers DYS SN36A	4,13 €	16,51 €
1	Expansor E/S MCP23008	1,16 €	1,16 €
1	Placa virgen PCB 200x200mm	2,20 €	2,20 €
1	Plancha cobre PCB 100x100mm	3,53 €	3,53 €
1	10 Resistencias 0,47 Ohmios	0,20 €	0,20 €
1	10 Resistencias 220 Ohmios	0,20 €	0,20 €
1	10 Resistencias 1K	0,20 €	0,20 €
1	10 Resistencias 10K	0,20 €	0,20 €
5	Condensador 10uF	0,25 €	1,25 €
1	Condensador 1uF	0,25 €	0,25 €
14	Condensador 100K	0,22 €	3,08 €
2	Diodos 600mV	0,38 €	0,76 €
3	Diodos 0,7V	0,37 €	1,11 €
3	Inductor 47uH	0,64 €	1,92 €
1	Condensador 4,7uF	0,24 €	0,24 €
3	Condensador 22uF	0,19 €	0,57 €
1	Transistor MOSFET 6,2A 600V	1,91 €	1,91 €
1	Cable Cobre 4m 1,5 mm diámetro	9,95 €	9,95 €
		TOTAL	183,96 €

Autor: Mario Urgel García
424.16.31

4.3. POTENCIA DEL CIRCUITO

Unidades	Artículo	Precio/Unidad(€)	Precio(€)
1	Cargador baterías MAX1926	20,86 €	20,86 €
1	Convertidor 3V3 LP2980	0,33 €	0,33 €
1	Convertidor 5V Tracopower TEN5-1211	2,20 €	2,20 €
1	Fuente de alimentación Meanwell P5-35-13,5	16,67 €	16,67 €
2	Baterías Zippy Flightmax 8000mAh	43,61 €	87,22 €
1	Tablero Pino 600x600mm 10mm espesor	4,95 €	4,95 €
2	Lámina cobre 200x500mm 10mm espesor	16,18 €	32,36 €
		TOTAL	164,59 €

4.4. PRESUPUESTO GENERAL

Sección	Precio(€)
Componentes Mecánicos	64,05 €
Componentes Electrónicos	183,96 €
Potencia Circuito	164,59 €
Mano de obra	8.400,00 €
IVA 21%	1.850,65 €
TOTAL	10.663,25 €

De este modo, el presupuesto del proyecto total asciende a diez mil seiscientos sesenta y tres euros con veinticinco céntimos.

5. ANEXO 5 PLIEGO DE CONDICIONES

Este documento contiene las condiciones legales que guiarán la realización, en este proyecto, de un dron cuadricóptero de videovigilancia. En lo que sigue, se supondrá que el proyecto ha sido encargado por una empresa cliente a una empresa consultora con la finalidad de realizar dicho sistema. Dicha empresa ha debido desarrollar una línea de investigación con objeto de elaborar el proyecto. Esta línea de investigación está amparada por las condiciones particulares del siguiente pliego:

5.1. CONDICIONES GENERALES

1. El montaje y fabricación de los elementos que intervengan será realizado totalmente por la empresa licitadora.

2. En la oferta, se hará constar el precio total por el que se compromete a realizar el proyecto.

3. El proyecto se realizará bajo la supervisión de un Ingeniero Técnico para el desarrollo de la misma.

4. El contratista tiene derecho a sacar copias a su costa de los planos, pliego de condiciones y presupuestos. El Ingeniero autor del proyecto autorizará con su firma las copias solicitadas por el contratista después de confrontarlas.

5. Tanto en las certificaciones de obras como en la liquidación final, se abonarán los trabajos realizados por el contratista a los precios de ejecución de material que figuran en el presupuesto para cada unidad de obra.

6. Concluida la ejecución del proyecto, será reconocido por el Ingeniero Técnico que a tal efecto designe la empresa.

7. La garantía total será del 4% del presupuesto y la parcial del 2%.

8. La garantía parcial cubre desperfectos de fábrica y fallos de funcionamiento, mientras que la total cubre además averías. Ambos tipos no soportan roturas accidentales o desperfectos por causas que no sean su uso normal.

9. La garantía será de dos años una vez disponga la empresa cliente del sistema completamente instalado.

10. La forma de pago será en un único pago abarcando el coste total del presupuesto o dividido en mensualidades durante un año con un interés del 3% sobre el presupuesto total.

11. El tiempo transcurrido desde que la empresa cliente pide la máquina hasta su disposición es de 3 semanas.

11. El cuadricóptero será enviado a la sede de la empresa cliente asumiendo los gastos de transporte el propio cliente.

12. La empresa cliente dispondrá de un servicio de garantía de dos años una vez disponga de la máquina completamente instalada.

13. En caso de averías no soportadas por la garantía o fuera del plazo establecido se ofrecerá un servicio de reparación a un precio de mano de obra de 25 €/hora incluyendo el coste de las piezas necesarias en caso de cambiarlas y el coste del transporte por parte de la empresa cliente.

5.2. CONDICIONES PARTICULARES

La empresa consultora, que ha desarrollado el presente proyecto, lo entregará a la empresa cliente bajo las condiciones generales ya formuladas, debiendo añadirse las siguientes condiciones particulares:

1. La propiedad intelectual de los procesos descritos y analizados en el presente trabajo, pertenece por entero a la empresa consultora representada por el Ingeniero Director del Proyecto.

2. En la autorización se ha de hacer constar la aplicación a que se destinan sus reproducciones así como su cantidad.

3. En todas las reproducciones se indicará su procedencia, explicitando el nombre del proyecto, nombre del Ingeniero Director y de la empresa consultora.

4. Si la modificación se acepta, la empresa consultora se hará responsable al mismo nivel que el proyecto inicial del que resulta el añadirla.

5. Si la modificación no es aceptada, por el contrario, la empresa consultora declinará toda responsabilidad que se derive de la aplicación o influencia de la misma.

Relación de documentos

(_) Memoria ..... 99 páginas

(X) Anexos .....283 páginas

La Almunia, a 29 de 11 de 2016

Firmado: Mario Urgel García